

'89.

GS High-Speed CMOS LOGIC DATA BOOK

- GD54/74HC Series
- GD54/74HCT Series



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MANUFACTURERS' AGENTS**

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GoldStar

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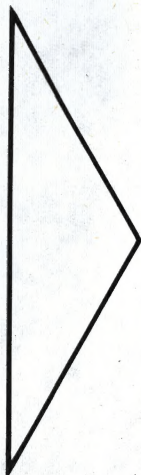
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INTRODUCTION

Family Description

GS High Speed CMOS Logic family, GD54/74HC, GD54/74HCT series, are based on Advanced Isoplanar Process, fully implanted CMOS technology with 2.5 μ m design rules and high performance double metal process to achieve the high speed operation superior to LS TTL while retaining the advantages of CMOS technology, the low power dissipation and high noise immunity. Also they are given special attention and design technique for Latch-Up free.

An extensive product range of functions from basic gates to bus compatible devices and the aforementioned performance will help you to improve system performance and reliability. That's the reason why so many logic designers are calling GoldStar.

Family Features

- Functionally and pin compatible with industry 54 and 74 LSTTL-series and GD4000B-series types.
- CMOS outputs for maximum noise margins.
- Fan-out (over temperature):
Standard Outputs-10 LSTTL loads
Bus-Driver Outputs-15 LSTTL loads
- Wide operating temperature range:
GD74HC/HCT/HCU: -40 to +85°C
GD54HC/HCT/HCU: -55 to +125°C
- Balanced propagation and transition times.
- Significant power reduction compared to LSTTL logic.

Series Features

GD54/74HC Series

- 2 to 6V operation.
- High noise immunity $NM_L=20\%$, $NM_H=30\%$ at $V_{CC}=4.5V$

GD54/74HCT Series

- 4.5 to 5.5V operation.
- Direct LSTTL input logic compatibility
 $V_{IL}=0.8V(max)$, $V_{IH}=2.0V(min)$
- CMOS input compatibility
 $I_{IL}, I_{IH} \leq 1\mu A$ at V_{OL}, V_{OH}

Table 1 compares significant operating characteristics of the HC/HCT vs. LSTTL logic families.

Table 1. Quantitative Comparison of High Performance CMOS and LSTTL Logic Types

Characteristic	74HC/HCT	74LS
1. Quiescent Power		
-per Gate	0.025 mW	6.0 mW
-per FF	0.11 mW	22 mW
-4 Stage Counter	0.44 mW	175 mW
-per Transceiver/Buffer	0.10 mW	65 mW

2. Operating Power

	Frequency			Frequency	
	0.1MHz	1MHz	10MHz	0.1 to 1MHz	10MHz
-per Gate	0.2mW	2mW	20mW	5.5mW	20mW
-per FF	0.15mW	1.5mW	15mW	10mW	15mW
-4 Stage Counter	0.24mW	2.4mW	24mW	95mW	120mW
-per Buffer/ Transceiver	0.25mW	2.5mW	25mW	60mW	90mW

3. Operating (HCT) Supply Voltage	4.5V to 5.5V	4.75V to 5.25V
(HC)	2V to 6V	

4. Operating Temperature Range

	-40°C to +85°C	0°C to +70°C
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5. Noise Margin @ 4.5V

LS to LS	—	0.7V/0.4V
HC to HC (HI/LOW)	1.25V/0.8V	—
HCT to HCT	2.4V/0.7V	—

6. Input Switching

Voltage Variation with Temp.	$V_{th} \pm 60 mV$	$V_{th} \pm 200 mV$
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7. Output Drive Current

a) Source Current at $V_{OH}=2.4, C_L=15pF$	-8mA	-400uA
b) Sink Current: Std. Logic (V_{OL}) BUS Logic (V_{OL}) $V_{OL}=0.5V$	4mA(0.33V) 6mA(0.33V) 12mA	4mA(0.4V) 12mA(0.4V) 24mA

8. Typ. Output

Transition Time		
t_{TLH}	6nS	15nS
t_{THL}	6nS	6nS

9. Typical Gate Propagation Delay*

t_{PHL}/t_{PLH}	8nS/8nS	8nS/11nS
$C_L=15pF$		

10. Typical FF Propagation Delay:

$C_L=15pF$		
t_{PLH}	14nS	15nS
t_{PHL}	14nS	22nS

11. Typ. Clock Rate of a FF

	50MHz	33MHz
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12. Input Current

I_{IL}	-1uA	-0.4 to -0.8mA
I_{IH}	1uA	40uA

13. 3-State Output Leakage Current

	$\pm 5uA$	$\pm 20uA$
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$V_{CC}=5V$, unless stated otherwise; $C_L=50pF$

INPUT

Switching Characteristics

A basic knowledge of input and output structures is essential to the High performance CMOS designer. Following section deals with the various input characteristic and application rules regarding their use.

The inputs of High performance CMOS devices are voltage-level sensitive, and do not require current, except for input leakage. The definitive switching characteristics for the HC and HCT versions are illustrated in Fig. 1.

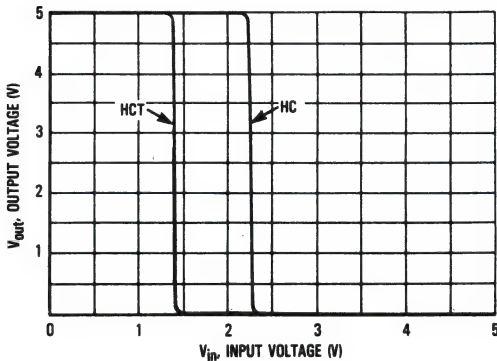


Fig. 1. Typical Transfer Characteristic for Buffered Devices

System designers require the actual MIN/MAX range of expected input switching voltage over the temperature range of -55°C to $+125^{\circ}\text{C}$. This vital information is contained in the curves of Fig. 2 and 3 for the HC and HCT families, respectively.

The unbuffered HCU04 hex inverter has one stage of active inverting logic from input to output and therefore, is a special case for input switching voltage as shown in Fig. 4.

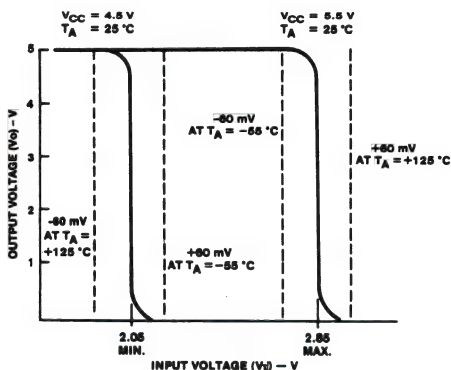


Fig. 2. Actual Min/Max switching characteristics of HC series types

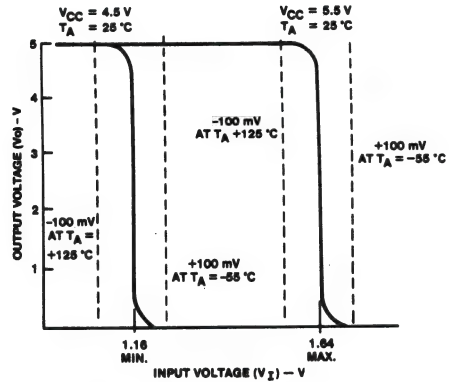


Fig. 3. Actual Min/Max switching characteristic of HCT series types

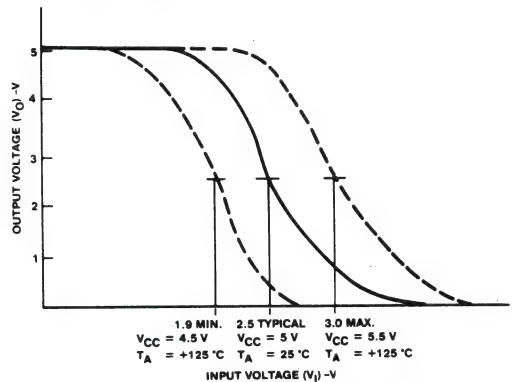


Fig. 4. Actual Min/Max and typical switching characteristics of the HCU04 Unbuffered Hex Inverter

Input Current

Fig. 5 shows the typical input leakage current of a High performance CMOS device as a function of ambient temperature for a V_{CC} of 6V. Over the full operation temperature range, the input leakage current is well below the rating specified in the JEDEC standard (100 nA between -55°C and $+25^{\circ}\text{C}$ and $1\mu\text{A}$ at $+85^{\circ}\text{C}$ and $+125^{\circ}\text{C}$).

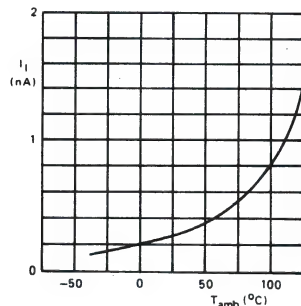


Fig. 5. Typical High performance CMOS input leakage current I_{IN} as a function of ambient temperature T_{amb} .

Termination of Unused Inputs

When CMOS inputs are left open-circuited, the inputs may be biased at or near the typical CMOS switchpoint of 0.45 V_{CC} for HC devices or 1.3 V for HCT devices. At this switchpoint, both the P-channel and the N-channel transistors are conducting, causing excess current drain. Due to the high gain of the buffered devices the device can go into oscillation from any noise in the system, resulting in even higher current drain. For these reasons, all unused HC/HCT inputs should be connected either to V_{CC} or GND.

For the bidirectional (transceiver) logic devices in the family have common I/O pins. When defined as inputs, they should be connected via a 10k Ω resistor to V_{CC} or GND.

Max Input Transition Time

Figure 6 shows the results of exceeding the maximum rise and fall times recommended by Goldstar or contained in JEDEC Standard No. 7A. The reason for the oscillation on the output is that as the voltage passes through the switching threshold region with a slow rise time, any noise that is on the input line is amplified, and is passed through to the output. This oscillation may have a low enough frequency to cause succeeding stages to switch, giving unexpected results. If input rise or fall times are expected to exceed the maximum specified rise or fall times, Schmitt-triggered devices such as GS HC/HCT14 and HC/HCT132 are recommended.

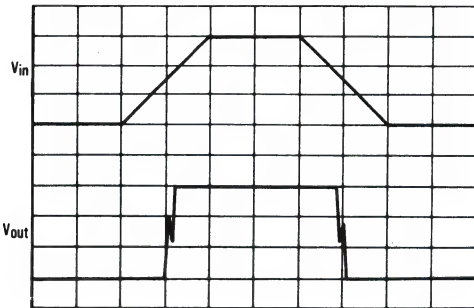


Fig. 6. Maximum Rise Time Violation.

Input-Voltage Considerations and Maximum Forward-Diode Input Current Limits

As a general rule, CMOS logic devices employing input clamp diodes (Fig. 7) to minimize ESD effects should be operated between the power supply rails. If the input series polysilicon resistor shown in Fig. 7 is not considered, then the rule is:

$$-0.5V \leq V_{IN} \leq (V_{CC} + 0.5V)$$

This rule is the industry standard (JEDEC Std. No. 7) and is intended to keep users from damaging devices because the devices of some HC/HCT device manufacturers do not

have the built-in input series polysilicon resistor. Data sheets continue to show the conservative rating established by JEDEC. However, GS High performance CMOS device inputs are capable of meeting the following rating:

$$-1.5V \leq V_{IN} \leq V_{CC} + 1.5V$$

Furthermore, except for special cases such as transceivers and analog switches or multiplexer signal inputs, can reliably operate with the $\pm 1.5V$ rule without logic errors. Beyond $\pm 1.5V$, maximum forward current poses a second limitation with respect to the V_{CC} and GND rail. This High performance CMOS and JEDEC rating is $\pm 20mA$ of transient current maximum forced into inputs or outputs.

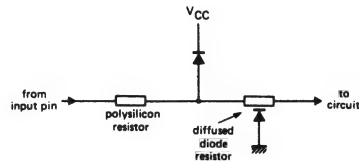


Fig. 7. Standard input protection of HC/HCT/HCU inputs against electrostatic discharge.

Noise Immunity and Noise margin

The noise margin characteristic of logic devices can be defined as amount of noise that a system can tolerate and still maintain collect logic operation or difference between the output logic Low (or High) of one gate and the input logic Low (or High) of the gate the given device is driving. The static noise immunity can be divided into two categories.

- $V_{NML} = V_{IL(max)}$ of the driven — $V_{OL(max)}$ of the driver
- $V_{NMH} = V_{OH(min)}$ of the driver — $V_{IH(min)}$ of the driven

Table 2. Noise Immunity and Noise margin at $V_{CC} = 4.5V$

		HC	HCT	HCU	LS
V_{ILmax}	(V)	0.9	0.8	0.8	0.8
V_{IHmin}	(V)	3.15	2.0	3.60	2.0
V_{OLmax}	(V)	0.1	0.1	0.5	0.4
		0.33(*)	0.33(*)		
V_{OHmin}	(V)	4.4	4.4	4.0	2.0
		3.84(*)	3.84(*)		
V_{NML}	(V)	0.8	0.7	0.3	0.4
V_{NMH}	(V)	1.25	2.4	0.4	0.7

* 4mA load

The guaranteed static noise-immunity characteristics for LSTTL and HC/HCT/HCU are shown Table 2. This table shows considerable improvement in NM of HC compared with that of LSTTL, and Table 3 shows NM in a mixed-technology system with fully loaded HCT and LSTTL output, $T_{amb} = 0^{\circ}C \sim 70^{\circ}C$

Table 3. Noise margin in a mixed technology system.

NM	HC	HCT	LS	LS→HCT	HC→HCT	HCT→HC
Low	0.8	-0.33	0.8-0.4	0.8-0.1	0.9-0.1	
High	3.84-2.0	2.7-2.0	4.4-2.0	4.4-3.15		
Low/High	0.47/1.84	0.4/0.7	0.7/2.4	0.8/1.25		

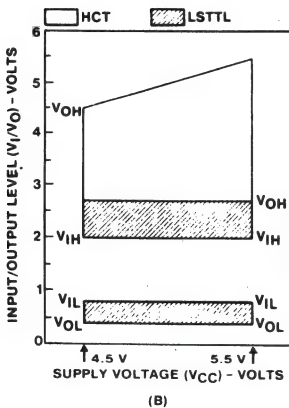
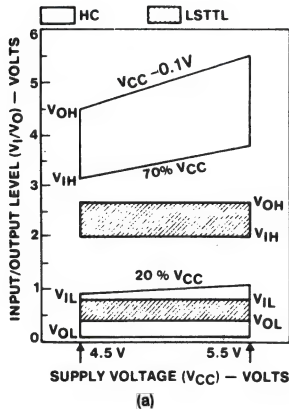


Fig. 8 Static noise margins for: (a) HC devices compared with LSTTL. and (b) HCT devices compared with LSTTL in a mixed technology system.

Whenever a HCT output drives either an LSTTL or a HCT input, the noise margin is better than when an LSTTL device drives an LSTTL or HCT input. This improvement is larger for V_{NMH} owing to the superior output sourcing current. The graph in Fig. 8 compares the static noise margins for HC devices with those for LSTTL. The graph illustrates that while HC circuits can drive LSTTL (as $V_{OH}(\min)$ for an HC device is greater than $V_{IH}(\min)$ for an LSTTL device), the

converse is not true since $V_{OH}(\min)$ for LSTTL is less than $V_{IH}(\min)$ for HC; there is no overlap in the noise-margin-high regions. Therefore, the noise-margin-high for LSTTL driving HC devices is said to be negative, which explains the reason for the problematical external pull-up resistor interfaced with LSTTL.

By the way, consider noise immunity for HC and HCT. HCT has a logic trip point at 1.4V, where the HC trips at 2.4V, thus HC's typical performance is twice that of HCT for ground noise; for V_{CC} noise, HCT is about 50% better. Therefore, in a normal system including CMOS systems, HC provides better noise immunity than HCT. The one case where HCT could prove more helpful is in systems that are designed with noiseless ground and dirty V_{CC} .

OUTPUT

Drive Capability

There are three different output configurations in the HCMOS family:

- push-pull
- three-state
- open-drain n-channel transistor.

Each is available with a standard output or a bus driver output, the latter having 50% more drive capability. All HC and HCT outputs are buffered for consistent current drives and a.c. characteristics throughout the family. Well-matched output N-channel and P-channel transistors give symmetrical output rise and fall times.

When comparing the output drive capabilities of High performance CMOS with those of LSTTL, note that LSTTL capability is usually expressed in unit loads (ULs) where the load is specified to be an input of the same family. Capability of High performance CMOS is expressed as the source or sink current at a specified output voltage. Since High performance CMOS requires virtually no input current, the unit load concept is not applicable. With a specified output drive of 4.0 mA at 0.4V, the High performance CMOS interface capability exceeds 4000 ULs, and with a 20uA/0.1V specification, the capability is 20ULs. Each standard output has a drive capability of 10 LSTTL loads and maintains a V_{OL} of 0.4V over the full temperature range. Bus driver outputs can drive 15 LSTTL loads under the same conditions. This high drive capability result from the decrease on gate length provided by silicon-gate process used. In addition, High performance CMOS offers symmetrical logic high and low currents as well.

Push-pull Outputs

A typical push-pull output stage is shown in Fig. 9. The bipolar parasitic transistor-drain diodes (D1 and D2) limit the output voltage V_O of all family in the case of externally-forced voltage such that $-0.5V \leq V_O \leq V_{CC} + 0.5V$. For voltages outside this range, the diodes and parasitic bipolar elements start to conduct. Although the diode current rating is 20 mA d.c., line ringing and power supply spikes in nor-

mal high-speed systems cause current-peaks that exceed this rating. Careful chip-layout and adequate aluminum traces ensure that the current peaks produced will not damage the diodes or degrade the internal circuitry. The maximum rated d.c. current for a standard output is 25 mA and that for a bus-driver output is 35 mA. These ratings are dictated by the current capability of on-chip metal traces and long-term aluminum migration, but it is expected that output currents during switching transients will, at times, exceed the maximum ratings.

A shorted output will also cause the maximum d.c. current rating to be exceeded. However, for logic testing, one output may be shorted for up to five seconds without damaging the device.

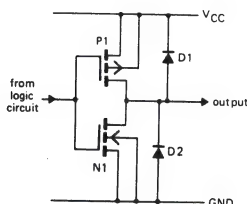


Fig. 9. Basic CMOS output stage.

3-State Outputs

Some HC/HCT devices have outputs that can be placed into a high-impedance state. These 3-state output devices are very useful for gang connecting to a common line or bus. When enabled, these output pins can be considered as ordinary output pins; as such, all specifications and precautions of standard output pins should be followed. When disabled, these output pins go into 3-state output. All I/O ports and transceivers have a three-state output. The I/O pin is defined as an input when the output is disabled, but this pin should be regarded as a real input and should not be left floating, because the input to an I/O port can cause V_{CC} current. If necessary, terminate the input with a 10k Ω resistor, see 'Termination of unused inputs'.

Open-drain Outputs

GS provides 3 open drain devices (03, 05 and 09) that are fabricated using only on N-ch transistor. The application of open drain device is for the wired-OR, driving LED or simply power-saving logic.

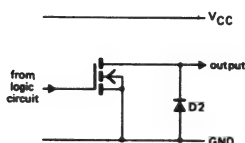


Fig. 10. Open-drain output circuit.

Increased drive capability of gates

For applications that require driving high capacitive loads where fast propagation delays are needed (e.g., driving power MOSFETs), devices within the same package may be paralleled. Paralleling devices in different packages may result in devices switching at different points on the input voltage waveform, creating output short circuits and yielding undesirable output voltage waveforms.

Protection

The outputs in a High performance CMOS devices are protected from ESD damage by diodes. Figure 11 shows these diodes. These intrinsic diodes are effective because of the large geometries (widths) of the output transistors. These diodes are the drain to n-substrate junction of the p device and the drain to p-well junction of the n device. This network provides protection to voltage levels typically greater than 3kV in all ESD discharge modes pertaining to the output.

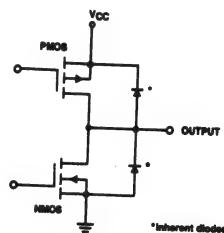


Fig. 11. Inherent diodes protecting output.

Output Curves

Output current derating versus temperature is shown in Fig. 12 and is valid for all types of output. As a design aid, output characteristic curves are given for both P-channel source and N-channel sink currents. The curves given include expected minimum curves for $T_A=25^\circ$, 85° , and 125°C , as well as typical values for $T_A=25^\circ\text{C}$. For temperatures $<25^\circ\text{C}$, use the 25°C curves. These curves, Figure 13 through 24 are intended as design aids, not as guarantees. Unused output pins should be open-circuited (floating).

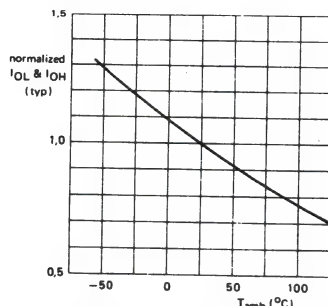


Fig. 12. Derating curve for output drive currents I_{OL} and I_{OH} .

STANDARD OUTPUT CHARACTERISTICS

N-CHANNEL SINK CURRENT

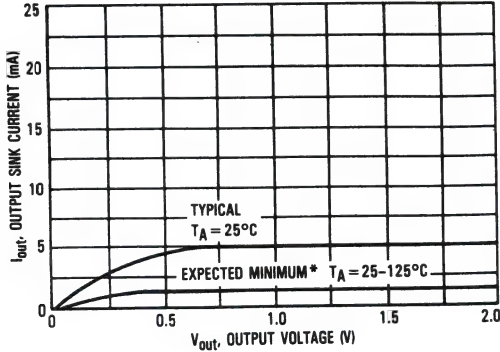


Fig. 13. $V_{CC}=2V$

P-CHANNEL SOURCE CURRENT

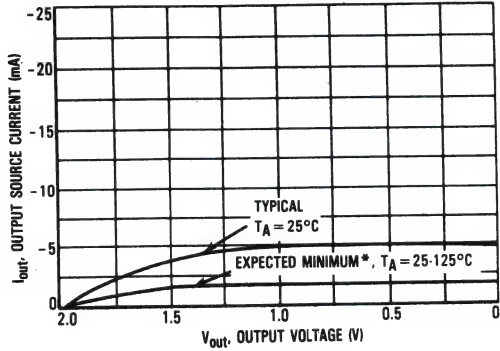


Fig. 14. $V_{CC}=2V$

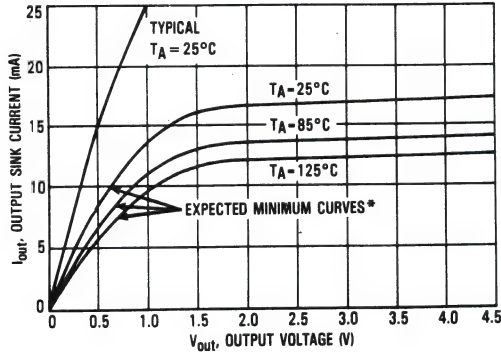


Fig. 15. $V_{CC}=4.5V$

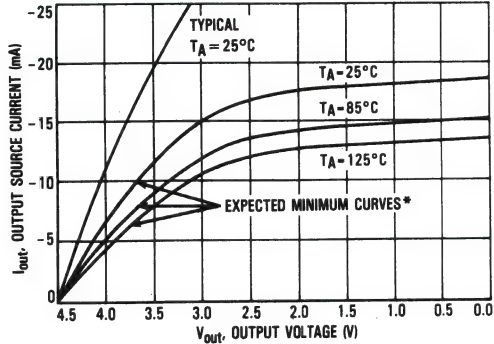


Fig. 16. $V_{CC}=4.5V$

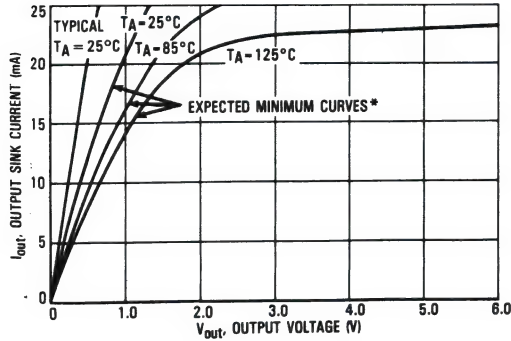


Fig. 17. $V_{CC}=6.0V$

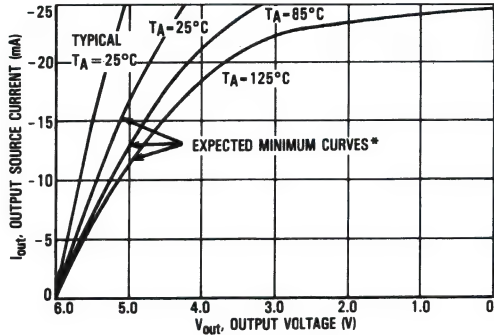


Fig. 18. $V_{CC}=6.0V$

*The expected minimum curves are not guarantees, but are design aids.

BUS-DRIVER OUTPUT CHARACTERISTICS

N-CHANNEL SINK CURRENT

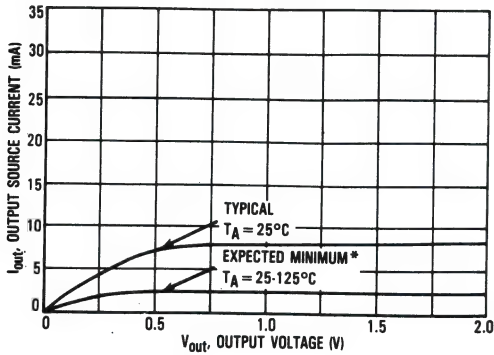


Fig. 19. $V_{CC}=2V$

P-CHANNEL SOURCE CURRENT

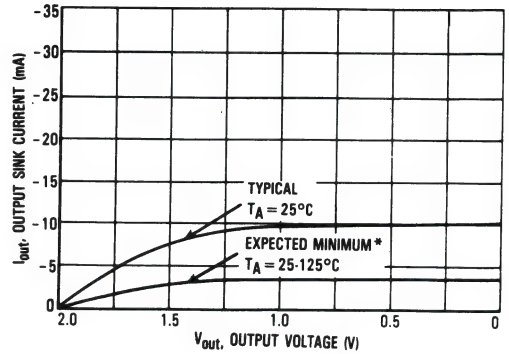


Fig. 20. $V_{CC}=2V$

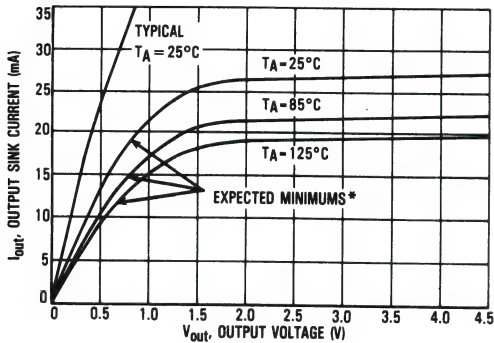


Fig. 21. $V_{CC} = 4.5 V$

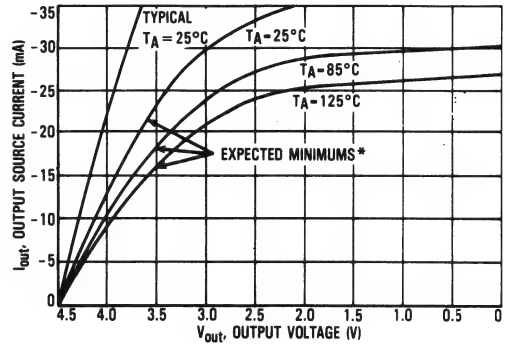


Fig. 22. $V_{CC}=4.5V$

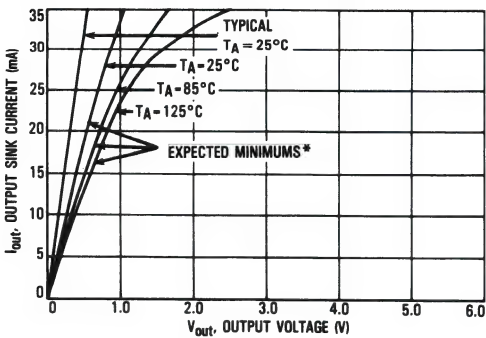


Fig. 23. $V_{CC}=6.0V$

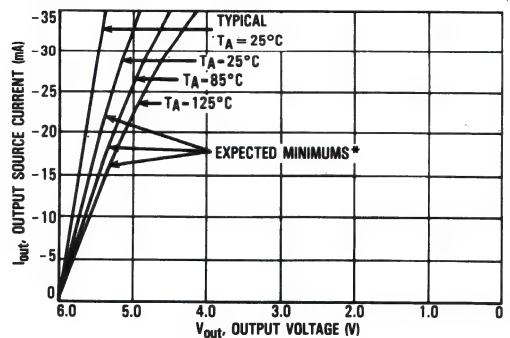


Fig. 24. $V_{CC}=6.0V$

*The expected minimum curves are not guarantees, but are design aids.

I/O PROTECTION

ESD

The gate input of a MOS transistor acts as a capacitor ($<1\text{pF}$) with very low leakage current ($<1\text{pA}$). Without protection, such an input could be electrostatically charged to a high voltage that would breakdown the dielectric and permanently damage the device. The integration process of the family allows polysilicon resistors to be formed at all inputs to slow down fast input transients caused by electrostatic discharge and to dissipate some of their energy. High performance CMOS device inputs have a resistor-diode protection network, shown in Fig. 7 that protects the gate oxide from electrostatic discharge (ESD) damage. The network provides protection to levels typically greater than 2kV. The 2kV figure was arrived at by testing devices in the ESD test circuit shown in Fig. 25 and Fig. 26 while conforming to the MIL-STD 883, test method 3015. Although all inputs and outputs are protected against electrostatic discharge, the standard CMOS handling precautions should be observed.

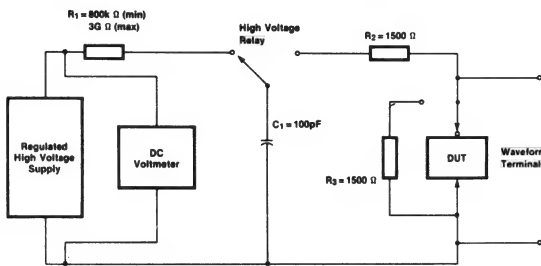


Fig. 25. ESD Test Circuit

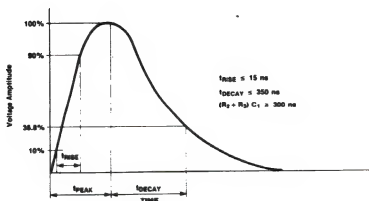


Fig. 26. ESD Pulse Waveform

Latch-Up

Typically, High performance CMOS devices do not latch up with currents of 75 mA forced into or out of the inputs or 300 mA for the outputs under worst case conditions ($T_A=125^\circ\text{C}$ and $V_{CC}=6\text{V}$). Under dc conditions for the inputs, the input protection network typically fails, due to grossly exceeding the maximum input voltage rating of -1.5 to $V_{CC}+1.5$ before latch-up currents are reached.

For most designs, latch up will not be a problem, but the designer should be aware of it, what causes it, and how it can be prevented.

Fig. 27 shows the parasitic bipolar devices that are formed. The circuit formed by the parasitic transistors and resistors is the basic configuration of a silicon controlled rectifier, or SCR. In the latch-up condition, transistors Q1 and Q2 are turned on, each providing the base current necessary for the other to remain in saturation, thereby latching the device on. Unlike a conventional SCR, where the device is turned on by applying a voltage to the base of the NPN transistor, the parasitic SCR is turned on by applying a voltage to the emitter of either transistor. The two emitters that trigger the SCR are the same point, the CMOS output. Therefore, to latch up the CMOS device, the output voltage must be greater than $V_{CC}+0.5\text{V}$ or less than -0.5V and have sufficient current to trigger the SCR. The latch-up mechanism is similar for the inputs.

Once a CMOS device is latched up, if the supply current is not limited, the device can be destroyed or its reliability can be degraded. Ways to prevent such an occurrence are listed below.

1. Ensure that inputs and outputs are limited to the maximum rated values.

$$-1.5 \leq V_{in} \leq V_{CC} + 1.5 \text{ V referenced to GND}$$

$$-0.5 \geq V_{out} \geq V_{CC} + 0.5 \text{ V referenced to GND}$$

$$|I_{IN}| \leq 20 \text{ mA}$$

$$|I_{OUT}| \leq 25 \text{ mA for standard outputs}$$

$$|I_{OUT}| \leq 35 \text{ mA for bus-driver outputs}$$

2. If voltage transients of sufficient energy to latch up the device are expected on the inputs or output, external protection diodes can be used to clamp the voltage. Another method of protection is to use a series resistor to limit the expected worst case current to the maximum ratings value.
3. Sequence power supplies so that the inputs or outputs of High performance CMOS devices are not active before the supply pins are powered up (e.g., recessed edge connectors and/or series resistors may be used in plug-in board applications).
4. Voltage regulating and filtering should be used in board design and layout to ensure that power supply lines are free of excessive noise.
5. Limit the available power supply current to the devices that are subject to latch-up conditions. This can be accomplished with the power-supply filtering network or with a current-limiting regulator.

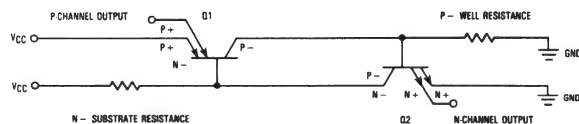


Fig. 27. Latch-Up Circuit Schematic

Supply Voltage

The HC and HCU versions have a power supply range of 2 to 6V; the absolute maximum voltage rating is 7V. The ability to use HC types with a 2V supply makes these devices particularly useful in battery-operated equipment, especially systems including memories that feature 2V standby operation. The absolute maximum supply or ground current, per pin, is $\pm 50\text{mA}$ for types with standard output drive, and $\pm 70\text{mA}$ for types with bus driver outputs. The operating supply-voltage range for GD74HCT types is 4.5V to 5.5V, $5\text{V} \pm 5\%$. These figures indicate that there is more tolerance in the regulation of the low-current CMOS system supply than is the case with other technologies. The maximum voltage indicated for HC and HCU versions also applies to HCT versions. The advantages of using High performance CMOS with its wider voltage supply range are illustrated in Fig. 28.

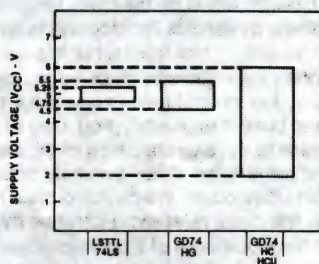


Fig. 28 Power-supply ranges for GD74HCT, GD74HC, and GD74HCU versions of the High performance CMOS family of devices and 74LS series types.

Decoupling Capacitors

The switching waveforms shown in Figures 29 and 30 show the current spikes introduced to the power supply and ground lines. This effect is shown for a load capacitance of less than 5 pF and for 50 pF. For ideal power supply lines with no series impedance, the spikes would pose no problem. However, actual power supply and ground lines do possess series impedance, giving rise to noise problems. For this reason, care should be taken in board layouts, ensuring low impedance paths to and from logic devices.

To absorb switching spikes, the following High performance CMOS devices should be bypassed with good quality 0.022 μF to 0.1 μF decoupling capacitors:

1. Bypass every device driving a bus with all outputs switching simultaneously.
2. Bypass all synchronous counters.
3. Bypass devices used as oscillator elements.
4. Bypass Schmitt-trigger devices with slow input rise and fall times. The slower the rise and fall time, the larger the bypass capacitor. Lab experimentation is suggested.

Bypass capacitors should be distributed over the circuit board. In addition, boards could be decoupled with a 1 μF capacitor.

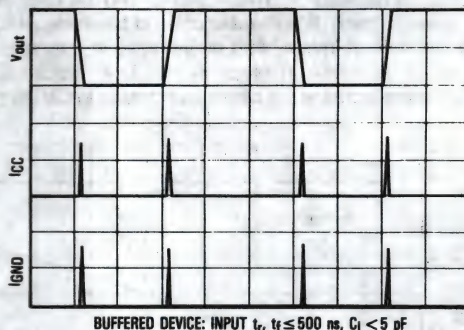


Fig. 29. Switching Currents for $C_L < 5\text{ pF}$

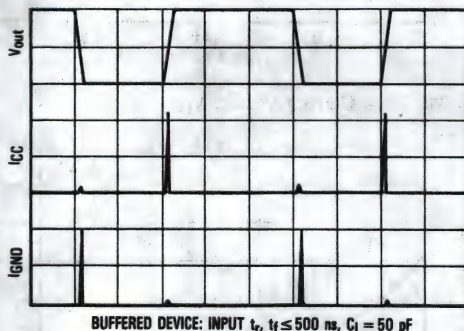


Fig. 30. Switching Currents for $C_L = 50\text{ pF}$

DYNAMIC CHARACTERISTICS

Propagation delay

The GS High performance CMOS family is designed to meet the dynamic switching speeds and operating frequency of low-power Schottky TTL. When compared to silicon-gate GD4000B series CMOS shows an improvement in ac performance. Values given in the data sheets are for the full operating temperature range and the supply voltages used are 2.0 V, 4.5 V and 6.0 V for HC devices, and 4.5 V for HCT devices. The published a.c. characteristics of the family are guaranteed for a capacitive test load of 50pF, a more realistic load than the 15 pF specified for LSTTL. The dynamic performance of a CMOS device is related to its drain characteristics. The drain characteristics are related to the thresholds and gate-to-source voltage potential, V_{GS} . The V_{GS} voltage at the input of the final stage of buffered devices is approximately the power supply voltage, V_{CC} or GND. Because $V_{GS} = V_{CC}$ or GND, the output drive current is proportional to the supply voltage. Therefore, a reduction in V_{CC} adversely affects the drain

characteristics which, in turn increases the propagation delays. An increase in V_{CC} decreases the propagation delays. Figure 31 and 32 show the typical variation of current drive and propagation delay, normalized to $V_{CC}=4.5$ V for $2.0 \leq V_{CC} \leq 6.0$ V. These curves may be used with the tables on each data sheet to arrive at parametric values over the voltage range. And an increase in temperature causes a decrease in electron and hole mobilities, a temperature increase will cause an increase in CMOS pro-

pagation delays. Correspondingly, ac performance improves with lower temperatures typically, speeds derate linearly from 25°C at about $-0.3\%/^\circ\text{C}$.

In addition to power supply and temperature effects, capacitive loading effect should be taken into account, for loads greater than 50pF, increase in propagation delay is expected.

Clock Pulse Requirements

All High performance CMOS flip-flops and counters contain master-slave devices with level-sensitive clock inputs. As the voltage at the clock input reaches the threshold level of the device, data in the master (input) section is transferred to the slave (output) section. The use of voltage threshold levels for clocking is an improvement over ac-coupled clock inputs, however, these levels make these devices somewhat sensitive to clock-edge rates. The threshold level is typically 50% of V_{CC} for HC devices, and 28% of V_{CC} for HCT devices (1.4V at $V_{CC}=5\text{V}$). Temperature has little effect on the clock threshold levels. The use of voltage thresholds for clocking is an improvement over a.c. coupled clock inputs, but it does not make the devices totally insensitive to clock-edge rates. When clocking occurs, the internal gates and output circuits of the device dump current to ground, producing a noise transient that is equal to the algebraic sum of the internal and external ground plane noise. When a number of loaded outputs change simultaneously, the device ground reference (and therefore the clock reference) can rise by as much as 500 mV. If the clock input of a positive-edge triggered device is at or near to its threshold during a noise transient, multiple triggering can occur. To prevent this, the rise and fall times of the clock inputs should be less than the published maximum (500 ns at $V_{CC}=4.5\text{V}$).

Maximum permissible input-clock pulse-frequency ratings on each clocked device-type data sheet requires a 50% duty cycle input clock. At these rated frequencies, the outputs will swing rail-to-rail, assuming no dc load on the outputs. This feature is a very conservative and highly reliable method of rating clock-input-frequency limits which for High performance CMOS devices, equal or exceed LSTTL ratings.

System clocking

In synchronously-clocked systems, spreads in the clock threshold levels of devices can cause logic errors if slow clock edges are used. For example, if data in one circuit changes before the clock threshold of the next sequential circuit is reached, a logic error will occur, see Fig. 33. To prevent this type of logic error, the maximum rise or fall time of the clock pulse should be less than twice the propagation delay of the flip-flop.

For a High performance CMOS device, the rise/fall time must be limited to 1000, 500 or 400 ns for $V_{CC}=2\text{V}$, 4.5V and 6V respectively. If these times are exceeded, noise on the input or power supply rails may cause the outputs to oscillate during transitions, causing logic errors and excessive power dissipation.

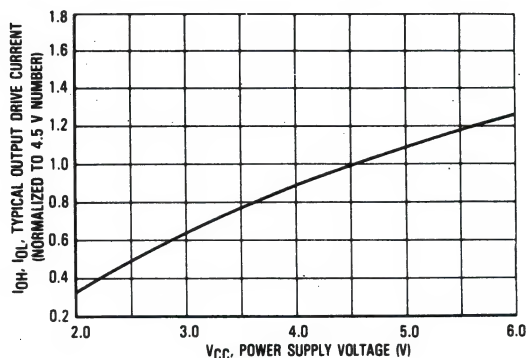


Fig. 31. Drive Current Versus V_{CC}

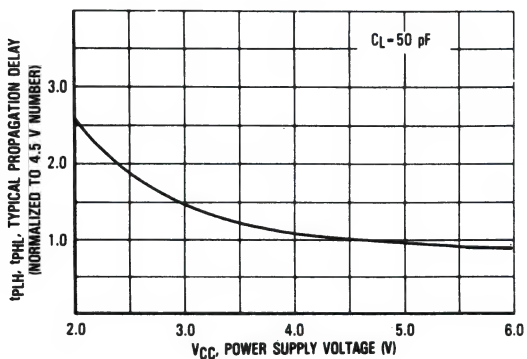


Fig. 32. Propagation Delay versus V_{CC}

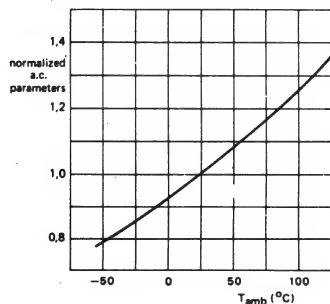


Fig. 33. Typical influence of temperature on a.c. parameters; $V_{CC}=5\text{V}$.

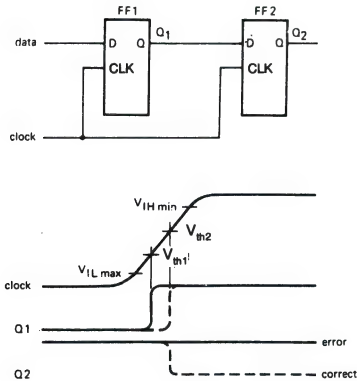


Fig. 33. In synchronously-clocked systems, changing the data in one device before the clock switching threshold of the next has been reached can cause logic errors. V_{th1} is the clock threshold of device 1; V_{th2} is the clock threshold of device 2.

POWER DISSIPATION

For LSTTL logic ICs operating below 10 MHz, the most significant part of the total power dissipation is the quiescent power dissipation due to the many bipolar transistors that continuously conduct. With High performance CMOS logic ICs however, the converse is true because quiescent power dissipation is only due to leakage currents through reverse-biased junctions and is so low that it is practically negligible compared with the frequency-dependent dynamic power dissipation.

Since the logic functions in most systems only change state during brief periods, the average system frequency is between one and two orders of magnitude lower than the system clock frequency. This means that replacing LSTTL ICs with equivalent HCT ICs, with their much lower quiescent power dissipation, results in a very significant reduction of overall system power dissipation without loss of operating speed.

Internal heat generation in CMOS can be divided into 2 categories; quiescent and dynamic power dissipations.

Quiescent Power Dissipation

When a CMOS is not switching, there should be no current path from V_{CC} to GND. And the device should not draw any supply current at all. In the quiescent state, either the PMOS or the NMOS transistor is fully off and, in theory, no direct MOS transistor channel path exists between V_{CC} and GND. In practice however, thermally generated minority charge-carriers, which are present in all reverse-biased diode junctions, allow a very small leakage current to flow between V_{CC} and GND. This current is defined as quiescent supply current (I_{CC}). Four factors affects the value of I_{CC} .

- Temperature
Increasing temperature causes I_{CC} to increase because the minority charge-carriers in the reverse-biased diode junctions are thermally generated.
- Device Complexity
MSI circuits dissipate more power than SSI circuits because they have a proportionally greater reverse-biased diode junction area.
- Supply voltage
The number of minority charge-carriers is linearly related to reverse junction voltage. The value of I_{CC} at $V_{CC}=2V$ is approximately one third the value at $V_{CC}=6V$.
- State-state input voltage levels
State-state input voltage levels which may slightly turn-on one of the input transistors and yet not fully turn-off the other. This causes a small additional quiescent supply current (ΔI_{CC}) to flow between V_{CC} and GND. In a system consisting entirely of HC ICs, the additional quiescent supply current ΔI_{CC} is so small that it can be omitted. This is because HC outputs swing from GND to V_{CC} . When these levels are applied to HC inputs they always turn one of the input transistors fully off. However, if HC input levels are held close to the switching threshold (typically $V_{CC}/2$). Fig. 34 shows that the additional quiescent supply current (ΔI_{CC}) becomes much greater than quiescent supply current I_{CC} .

Worst-case TTL V_{OL} of 0.5 V max. is close enough to GND to turn the input NMOS transistor fully off so that ΔI_{CC} is close to zero. However, a worst-case TTL V_{OH} of 2.4 V min. causes some ΔI_{CC} to flow. For this reason, 74HCT data sheets specify I_{CC} at the worst-case input voltage of $V_{CC}-2.1$ V.

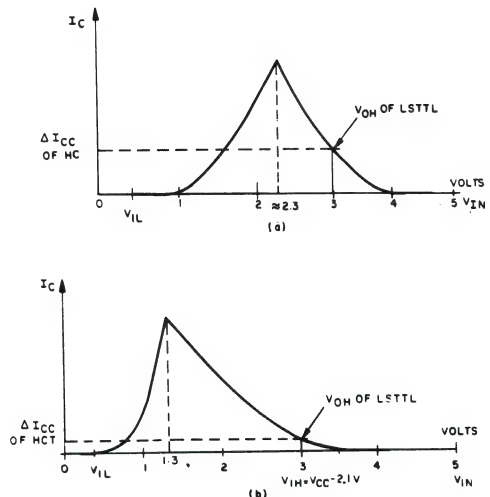


Fig. 34. (a) HC input, CMOS interface, (b) HCT input, TTL interface.

Therefore, following formula is used to compute quiescent power dissipation

$$\begin{aligned} \text{for HC } P_S &= I_{CC} \cdot V_{CC} \\ \text{for HCT } P_S &= I_{CC} \cdot V_{CC} + \Delta I_{CC} \cdot V_{CC} \cdot D \\ D: \quad &\text{Output switching duty factor} \\ &\Delta I_{CC} \text{ is calculated on a unit load basis} \end{aligned}$$

Dynamic Power Dissipation

Dynamic power dissipation is calculated in the same manner for both HC and HCT ICs. Three factors influence the dynamic power dissipation of High performance CMOS ICs. They are load capacitance, internal capacitance and switching transient currents.

— Load capacitance

The effect of load capacitance is caused by the charging and discharging of external capacitive loads. The energy dissipated in charging and discharging the capacitive load is

$$C_L \cdot V_{CC}^2 = P_{CL} \cdot t = P_{CL} \cdot \frac{1}{f_o}$$

therefore

$$P_{CL} = C_L \cdot V_{CC}^2 \cdot f_o$$

this equation is only applicable if all the outputs are switching the same load, if they are not, the equation becomes

$$P_{CL} = \Sigma(C_L \cdot V_{CC}^2 \cdot f_o)$$

For multiple output ICs, it is important to calculate with the appropriate output frequency.

— Internal capacitance

All MOS logic ICs have internal parasitic capacitance caused by diode junctions, MOS transistor structures, and the aluminium and polysilicon interconnections. It has the same effect as external capacitive loads, and its magnitude depends on the complexity of the circuit.

— Switching transient currents.

When the output of CMOS inverter, is switching states, wither from a logic 1 to a logic 0 or vice-versa, both transistors will be on for a short period of time. This condition creates a momentary low-resistance path between V_{CC} and ground. In this transient state, a momentary additional supply current (ΔI_{CC}) flows and power is consumed. This low-resistance path is obviously a function of the number of transitions the device makes as well as the input-signal rise and fall time. In other words, power loss resulting from internal device switching is proportional to the input frequency (as is power loss due to internal capacitance).

Although power dissipation due to switching and internal capacitance, increase linearly with increasing frequency. The power dissipation due to switching transient current is so small compared with internal capacitance. Therefore equation for dynamic dissipation is

$$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_i + \Sigma(C_L \cdot V_{CC}^2 \cdot f_o)$$

No-load Power Dissipation Capacitance.

For power dissipation calculation purposes, the total load caused by internal capacitances and by switching transient currents is defined as a single effective internal no-load power dissipation capacitance C_{PD} . It is defined on a 'per

Table 4. 54/74HC Family Characteristics

Symbol	Classification	V _{CC} (V)	Temperature (°C)						Units	Test Conditions
			54/74HC		74HC		54HC			
			+ 25		− 40 to 85		− 55 to 125			
			Min.	Max.	Min.	Max.	Min.	Max		
I _{CC}	SSI	6	—	2	—	20	—	40	μA	V _I =V _{CC} or GND I _O =0
	FF	6	—	4	—	40	—	80	μA	
	MSI	6	—	8	—	80	—	160	μA	

Table 5. Specification of ΔI_{CC} and unit load coefficient

Symbol	Parameter	T _{amb} (°C)								Unit	Test conditions		
		54/74HCT			74HCT		54HCT				V _{CC}	V _I	other
		+25			-40 to +85		-55 to +125						
		Min.	Typ.	Max.	Min.	Max.	Min.	Max.					
ΔI _{CC}	Additional quiescent supply current per input pin for unit load coefficient is 1		100	360		450		490	μA	4,5 to 5,5	V _{CC} -2,1V	Other inputs are V _{CC} or GND: I _O =0	

Note: To determine ΔI_{CC} per input, multiply this value by the unit load coefficient.
The unit load coefficient tables to be established at a later date.

function' basis and, where appropriate, it is also separately specified for each different logic function (e.g. gate or flip-flop) within the IC.

The worst-case operating conditions for C_{PD} are always chosen and the maximum number of internal and output circuits are toggled simultaneously. Devices which can be separated into independent sections are measured per section, the others are measured per device.

The recommended test frequency for determining C_{PD} is 1 MHz, but this is best increased to 10 MHz when I_{CC} is low and the device quiescent current influences I_{CC} .

Loading the switched outputs gives a more realistic value of C_{PD} , because it prevents transient 'through-currents' in the output stages. Furthermore, automatic testers often introduce about 30 pF to 40 pF on each device pin.

In order to determine the C_{PD} of a single section of a device (i.e., one of four gates, or one of two flip-flops in a package), GS uses the following procedures as defined by JEDEC.

Note: "biased" as used below means "tied to V_{CC} or GND."

Gates:	Switch one input while the remaining input(s) are biased so that the output(s) switch.
Latches:	Switch the enable and data inputs such that the latch toggles.
Flip-Flops:	Switch the clock pin while changing the data pin(s) such that the output(s) change with each clock cycle.
Decoders/ Demultiplexers:	Switch one address pin which changes two outputs.
Data Selectors/ Multiplexers:	Switch one address input with the corresponding data inputs at opposite logic levels so that the output switches.
Analog Switches:	Switch one address/select pin which changes two switches. The switch inputs/outputs should be left open. For digital applications where the switch inputs/outputs change between V_{CC} and GND, the respective switch capacitance should be added to the load capacitance.
Counters:	Switch the clock pin with the other inputs biased so that the device counts.
Shift Registers:	Switch the clock while alternating the input so that the device shifts alternating 1s and 0s through the register.
Transceivers:	Switch only one data input. place transceivers in a single direction.
Monostables:	The pulse obtained with a resistor and no external capacitor is repeatedly switched.
Parity Generators:	Switch one input.
Encoders:	Switch the lowest priority output.
Display Drivers:	Switch one inputs so that approximately one-half of the outputs change state.

ALUs/Adders: Switch the least significant bit. The remaining inputs are biased so that the device is alternately adding 0000 (binary) or 0001 (binary) to 1111 (binary)

Table 6. C_{PD} list

Equivalent Load (pF)	Codes
25	166, 173, 174, 259, 273, 373, 374, 377, 433, 534, 563, 564, 573, 574
47	93, 393
50	All unspecified codes
53	191
55	162
60	190, 192
100	42, 123, 137, 138, 139, 151, 154, 194, 221, 251, 280, 355, 423, 670
125	195
200	164
250	283, 299
#	05, 09, 34, 51, 76, 133, 148, 155, 298, 322, 386, 590

#: Value to be established at a later date

Power Dissipation Comparison

Figures 35 and 36 compare the dynamic power dissipation of SSI and MSI for HC, and LSTTL ICs. These graphs show that 74HC ICs maintain their power dissipation advantages for switching frequencies up to several MHz. This is because power is only dissipated during switching. The constant, frequency-independent power dissipation exhibited by LSTTL ICs is caused by the many bipolar transistors that continuously conduct.

Figures 35 and 36 also show that, as device complexity increases, the frequency at which High performance CMOS ICs dissipate the same amount of power as LSTTL ICs also increases. This is because, as LSTTL complexity increases, there are more resistive paths between V_{CC} and GND which carry more quiescent bias current and thus cause more quiescent power dissipation. High performance CMOS ICs also dissipate more quiescent power as their complexity increases, but the leakage currents which cause it are so small that it can be ignored.

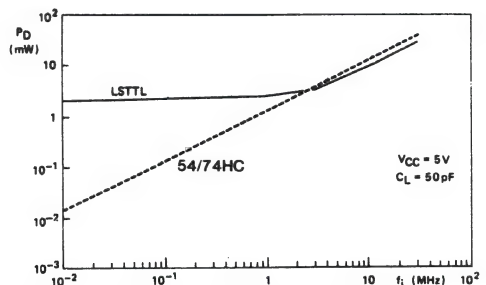


Fig. 35. Total power dissipation as a function of switching frequency for gates

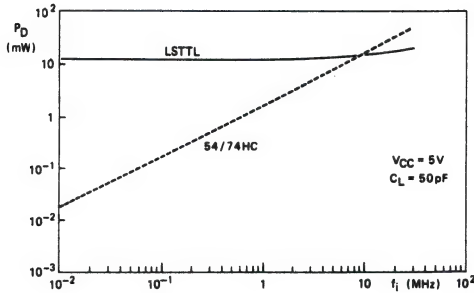


Fig. 36. Total power dissipation as a function of frequency for a dual flip-flop with one of the flip-flops toggling

INTERFACE

Interfacing

Because of the characteristics of the CMOS output, the High performance CMOS family is very versatile in interfacing between different logic families. The capability including the corresponding fanout is shown in Table 7. Note that the fanout to CMOS devices is limited only by the input rise and fall times, which are dependent on the capacitive loading, C_L . This dependence can be computed by the following relationship.

$$t_r, t_f = 2.2 RC_L$$

where R is the impedance of the output.

Table 7. High performance CMOS interfacing capability

Fanout From:	To Corresponding Logic Families:				
HC/HCT	TTL	LS	ALS	FAST	S/AS
Standard Types	2	10	20	6	2
Bus Drivers	3	15	30	10	3

HC types cannot be driven from any of the TTL families because the TTL output voltage high, $V_{OH}(\min)$, does not satisfy the HC input voltage high, $V_{IH}(\min)$ specification. The HCT types can be directly interfaced to the TTL families because the HCT input voltage high, $V_{IH}(\min)$ is less than the TTL output voltage high, $V_{OH}(\min)$. To meet minimum V_{IH} requirements, HC types can use a pull-up resistor as illustrated in Fig. 37.

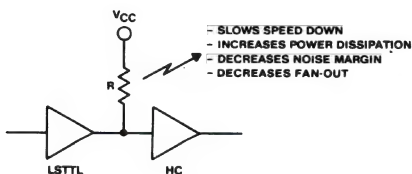


Fig. 37. Use of pull-up resistor to interface TTL and HC devices

However, the use of a pull-up resistor will not give optimum performance because as noted in Fig. 37, the resistor tends to slow down system speed, increase power dissipation, decrease noise margin, and decrease fan-out.

Logic-Level Conversion

The High performance CMOS family contains logic-level conversion types necessary to interface high-voltage logic levels (up to 15V common in control and automation systems) to low-voltage levels (down to 2V) as shown in Fig. 38.

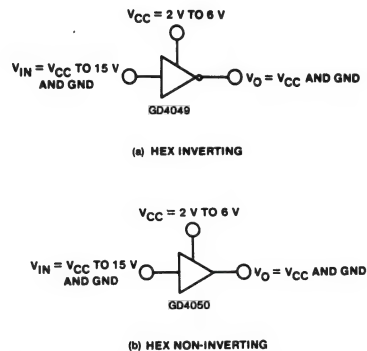


Fig. 38. High-to-low logic-level conversion

The High performance CMOS Quad open-drain NAND gate (HC/HCT03) is used to convert from HC (2V to 6V) or HCT (TTL or CMOS) logic levels up to 10V output logic levels as shown in Fig. 39. R_L can be a very wide range of values. For design of this output interface, use

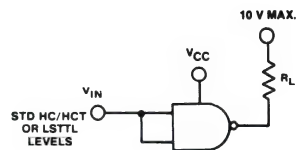


Fig. 39. Low-to-high logic-level conversion

the output N-MOS transistor characteristics of Fig. 15. The minimum value or R_L is that necessary to keep the output current below the 25mA family maximum rating. A large value of R_L will prolong the output rise time.

Bus Systems

CMOS is being used to an increasing extent in micro-processor bus systems following the introduction of versions of the popular NMOS processors.

There are several constraints imposed on microprocessor systems in industrial applications, such as electrically-noisy environments, battery-standby requirements and sealed, gas-tight enclosures. High performance CMOS bus systems, e.g. the CMOS Std. bus (a non-proprietary CMOS bus standard) provides a solution to all these problems. It offers superior noise immunity, equal operating speed, lower power dissipation, wider supply voltage range, extended temperature range, and enhanced reliability. For optimum results, use only HC devices in circuits which communicate directly with the bus. This allows a new bus termination to be introduced (see Fig. 48(b)) which, unlike the conventional TTL bus termination, draws no heavy d.c. current and is more suited to 48(b) outputs.

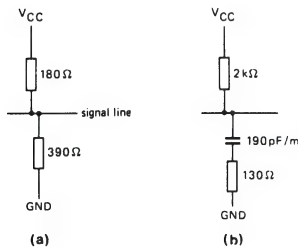


Fig. 40. Bus terminations. (a) Conventional termination for TTL buses. (b) Proposed termination for CMOS STD bus equivalents.

The wider supply voltage range of High performance CMOS together with its lower power dissipation virtually eliminates problems caused by voltage drops along power buses between cards in a system. It is possible for a circuit to pick up severe noise spikes or differential voltages via an edge connector. Such pick-up can exceed the CMOS maximum ratings if not limited by a $10\text{ k}\Omega$ series resistor in the High performance CMOS logic line. This will limit current to $\pm 20\text{ mA}$ for external voltages of up to $\pm 200\text{ V}$, however, for correct functioning, the d.c. input current should be kept below those values stated in 'Input/output protection'. The recommended board edge input protection is shown in Fig. 41.

In the circuit of Fig. 40, if the input diode current exceeds the maximum input current, a HIGH-to-LOW level shifter should be used (e.g. GD4049B or GD4050B).

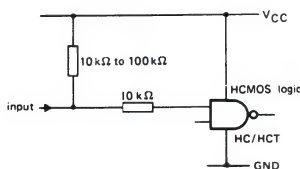


Fig. 41. Example of the board edge input protection circuit.



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GROSSANY OF TERMS. **f_{\max} Maximum Clock Frequency**

The maximum clocking frequency attainable with the following input and output conditions being met:

Input Conditions

HC & HCU: $t_r=t_f=6\text{ns}$, voltage swing from GND to V_{CC} with 50% duty cycle.

HCT : $t_r=t_f=6\text{ns}$, voltage swing from GND to 3.0 V with 50% duty cycle.

Output Conditions

Waveform must swing from 10% of $(V_{OH}-V_{OL})$ to 90% of $(V_{OH}-V_{OL})$ and be functionally correct under the given load condition: $C_L=50\text{ pF}$, all outputs.

 V_{CC} Supply Voltage

DC supply voltage (referenced to GND). The voltage range over which ICs are functional.

 V_{IH} HIGH Level Input Voltage

The worst case voltage that is recognized by a device as the HIGH state.

 V_{IL} LOW Level Input Voltage

The worst case voltage that is recognized by a device as the LOW state.

 V_{OH} HIGH Level Output Voltage

The worst case high-level voltage at an output for a given output current (I_{out}) and supply voltage (V_{CC}).

 V_{OL} LOW Level Output Voltage

The worst case low-level voltage at an output for a given output current (I_{out}) and supply voltage (V_{CC}).

 V_{T+} Positive-Going Input Threshold Voltage

The minimum input voltage of a device with hysteresis which is recognized as a high level. (Assumes ramp up from previous low level.)

 V_{T-} Negative-Going Input Threshold Voltage

The maximum input voltage of a device with hysteresis which is recognized as a low level. (Assumes ramp down from previous high level).

 V_H Hysteresis Voltage

The difference between V_{T+} and V_{T-} of a given device with hysteresis. A measure of noise rejection.

 I_{CC} IC Quiescent Supply Current

The current into the V_{CC} pin when the device inputs are static at V_{CC} or GND and outputs are not connected.

 ΔI_{CC} Additional Quiescent Supply Current

The current into the V_{CC} pin when one of the device inputs is at 2.4 V with respect to GND and the other inputs are static at V_{CC} or GND. The outputs are not connected.

 I_{IH} HIGH Level Input Current

The input current when the input voltage is forced to a high level.

 I_{IL} LOW Level Input Current

The input current when the input voltage is forced to a low level.

 I_{OH} HIGH Level Output Current

The output current when the output voltage is at a high level.

 I_{OL} LOW Level Output Current

The output current when the output voltage is at a low level.

 I_{OZ} Three-State Leakage Current

The current into or out of a three-state output in the high-impedance state with that respective output forced to V_{CC} or GND.

 I_{IN} Input Current

The current into an input pin with the respective input forced to V_{CC} or GND. A negative sign indicates current is flowing out of the pin (source). A positive sign or no sign indicates current is flowing into the pin (sink).

 I_{OUT} Output Current

The current out of an output pin. A negative sign indicates current is flowing out of the pin (source). A positive

sign or no sign indicates current is flowing into the pin (sink).

C_L Load Capacitance

The capacitor value which loads each output during testing and/or evaluation. This capacitance is assumed to be attached to each output in a system. This includes all wiring and stray capacitance.

C_{PD} Power Dissipation Capacitance

Used to determine device dynamic power dissipation.

t_{PLH} Low-to-High Propagation Delay

HC & HCU: The Time interval between the 0.5 V_{CC} level of the controlling input waveform and the 50% level of the output waveform, with the output changing from low level to high level.

HCT : The time interval between the 1.3 V level (with respect to GND) of the controlling input waveform and the 1.3 V level (with respect to GND) of the output waveform, with the output changing from low level to high level.

t_{PHL} High-to-Low Propagation Delay

HC & HCU: The time interval between the 0.5 V_{CC} level of the controlling input waveform and the 50% level of the output waveform, with the output changing from high level to low level.

HCT : The time interval between the 1.3 V level (with respect to GND) of the controlling input waveform and the 1.3 level (with respect to GND) of the output waveform, with the output changing from high level to low level.

t_{PLZ} 3-state Output Disable Time

HC & HCU: The time interval between the 0.5 V_{CC} level of the controlling input waveform and the 10% level of the output waveform, with the output changing from the low level to high-impedance (off) state.

HCT : The time interval between 1.3 V with respect to GND of the controlling input waveform and the 10% level of the output waveform, with the output changing from the low level to high-impedance (off) state.

t_{PHZ} 3-state Output Disable Time

HC & HCU: The time interval between the 0.5 V_{CC} level of the controlling input waveform and the 90% level of the output waveform, with the output changing from the high level to high-impedance (off) state.

HCT : The time interval between 1.3 V with respect to GND of the controlling input waveform and the 90% level of the output waveform, with the output changing from the high level to high-impedance (off) state.

t_{PZL} 3-state Output Enable Time

HC & HCU: The time interval between 0.5 V_{CC} level of the controlling input waveform and the 50% level of the output waveform, with the output changing from the high-impedance (off) state to a low level.

HCT : The time interval between 1.3 V level with respect to GND of the controlling input waveform and the 1.3 V level with respect to GND of the output waveforms, with the output changing from the high-impedance (off) state to a low level.

t_{PZH} 3-state Output Enable Time

HC & HCU: The time interval between the 0.5 V_{CC} level of the controlling input waveform and the 50% level of the output waveform, with the output changing from the high impedance (off) state to a high level.

HCT : The time interval between 1.3 V level with respect to GND of the controlling input waveform and the 1.3 V level with respect to GND of the output waveforms, with the output changing from the high-impedance (off) state to a low level.

t_{TLH} Output Transition Time

The time interval between the 10% and 90% voltage levels of the rising edge of a switching output, that is changing from LOW-to-HIGH.

t_{THL} Output Transition Time

The time interval between the 90% and 10% volage levels of the falling edge of a switching output, that is changing from HIGH-to-LOW.

t_w Pulse width

HC & HCU: The time interval between 50% levels of an input pulse required to guarantee proper operation of a logic device.

HCT : The time interval between 1.3 V levels (with respect to GND) of an input pulse required to guarantee proper operation of a logic device.

- t_{su} Setup Time**
The time interval immediately preceeding the active transition of a clock or latch enable input, during which the data to be recognized must be maintained (valid) at the input to ensure proper recognition. A negative setup time indicates that the data at the input may be applied sometime after the active clock or latch transition and still be recognized.
- HC & HCU:** The setup time is measured from the 50% level of the data waveform to the 50% level of the clock or latch input waveform.
- HCT** : The setup time is measured from the 1.3 level (with respect to GND) of the clock or latch input waveform.
- t_h Hold Time**
The time interval immediately following the active transition of a clock or latch enable input, during which the data to be recognized must be maintained (valid) at the input to ensure proper recognition. A negative hold time indicates that the data at the input may be changed prior to the active clock or latch transition and still be recognized.
- HC & HCU:** The hold time is measured from the 50% level of the clock or latch input waveform to the 50% level of the data waveform.
- HCT** : The hold time is measured from the 1.3 V level (with respect to GND) of the clock or latch input waveform to the 1.3 V level (with respect to GND) of the data waveform.
- t_{rec} Recovery Time**
HC & HCU: The time interval between the 50% level of the transition from active to inactive state of an asynchronous control input and the 50% level of the active clock or latch enable edge required to guarantee proper operation of a device.
- HCT** : The time interval between the 1.3 V level (with respect to GND) of the transition from active to inactive state of an asynchronous control input and the 1.3 V level (with respect to GND) of the active clock or latch edge required to guarantee proper operation of a logic device.
- t_r Input Rise Time**
HC & HCU: The time interval between the 10% and 90% voltage levels on the rising edge of an input signal.
- HCT** : The time interval between the 0.3 V level and 2.7 V level (with respect to GND) on the rising edge of an input signal.
- t_f Input Fall Time**
HC & HCU: The time interval between the 90% and 10% voltage levels on the falling edge of an input signal.
- HCT** : The time interval between the 2.7 V level and 0.3 V level (with respect to GND) on the falling edge of an input signal.



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GD54/74HC00, GD54/74HCT00

QUAD 2-INPUT NAND GATES

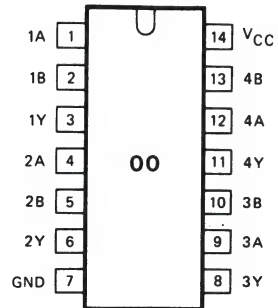
General Description

These devices are identical in pinout to the 54/74LS00. They contain four independent 2-input NAND gates. These devices are characterized for operation over wide temperature ranges to meet industry and military specifications.

Features

- Low Power consumption characteristic of CMOS devices
- Output drive capability: 10 LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts
for HCT 4.5 to 5.5 volts
- Low input current: $1\mu\text{A}$ Max.
- Low quiescent current: $20\mu\text{A}$ Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs

Pin Configuration



Suffix-Blank : Plastic Dual In Line Package
 Suffix-J : Ceramic Dual In Line Package
 Suffix-D : Small Outline Package

Logic Symbol and Logic Diagram

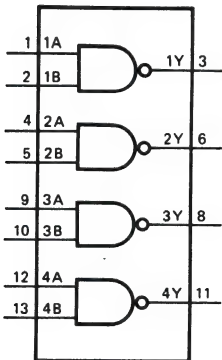


Fig. 1 Logic Symbol

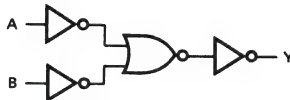


Fig. 2 Logic diagram (one gate)

Function Table

INPUTS		OUTPUT
nA	nB	nY
L	L	H
L	H	H
H	L	H
H	H	L

H=HIGH voltage level
 L=LOW voltage level

Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC Supply voltage		-0.5	+7	V
I_{IK}, I_{OK}	DC input or output diode current	for $V_I < -0.5$ or $V_I > V_{CC} + 0.5V$		20	mA
I_O	DC output source or sink current	for $-0.5V < V_O < V_{CC} + 0.5V$		25	mA
I_{CC}	DC V_{CC} or GND current			50	mA
T_{stg}	Storage temperature range		-65	150	°C
P_D	Power dissipation per package	above +70°C: derate linearly with 8mW/K		500	mW
T_L	Lead temperature	At distance $1/16 \pm 1/32$ in. from case for 60 sec(CERAMIC) 10 sec(PLASTIC)		300 260	°C

Recommended Operating Conditions

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range V_{CC} : GD54/74HC Types GD54/74HCT Types	2 4.5	6 5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A : GD74 Types GD54 Types	-40 -55	+85 +125	°C
Input Rise and Fall times t_r, t_f : GD54/74HC Types at 2V at 4.5V at 6V GD54/74HCT Types at 4.5V		1000 500 400 500	ns

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HC00		GD54HC00		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V_{IH}	HIGH level input voltage		2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2		1.5 3.15 4.2		V
V_{IL}	LOW level input voltage		2.0 4.5 6.0			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V
V_{OH}	HIGH level output voltage	$V_{IN}=V_{IH}$	$I_{OH}=-20\mu\text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9	V
			$I_{OH}=-4\text{mA}$	4.5 6.0	3.98 5.48	4.3 5.2		3.84 5.34		3.7 5.2	
		or V_{IL}	$I_{OH}=-20\mu\text{A}$	2.0 4.5 6.0			0.1 0.1 0.1		0.1 0.1 0.1	0.1 0.1 0.1	
			$I_{OH}=-4\text{mA}$	4.5 6.0		0.17 0.15	0.26 0.26		0.33 0.33	0.4 0.4	
V_{OL}	LOW level output voltage	$V_{IN}=V_{IH}$	$I_{OL}=20\mu\text{A}$	2.0 4.5 6.0			0.1 0.1 0.1		0.1 0.1 0.1	0.1 0.1 0.1	V
		or V_{IL}	$I_{OL}=4\text{mA}$	4.5 6.0		0.17 0.15	0.26 0.26		0.33 0.33	0.4 0.4	
$ I_{IN} $	Input leakage current	$V_{IN}=V_{CC}$ or GND	6.0			0.1		1.0		1.0	μA
I_{CC}	Quiescent supply current	$V_{IN}=V_{CC}$ or GND $I_{out}=0\mu\text{A}$	6.0			2		20		40	μA

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HCT00		GD54HCT00		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V_{IH}	HIGH level input voltage		4.5 to 5.5	2.0			2.0		2.0		V
V_{IL}	LOW level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V_{OH}	HIGH level output voltage	$V_{IN}=V_{IH}$	$I_{OH}=-20\mu\text{A}$	4.5	4.4	4.5		4.4		4.4	V
		or V_{IL}	$I_{OH}=-4\text{mA}$	4.5	3.98	4.3		3.84		3.7	
V_{OL}	LOW level output voltage	$V_{IN}=V_{IH}$	$I_{OL}=20\mu\text{A}$	4.5			0.1		0.1		V
		or V_{IL}	$I_{OL}=4\text{mA}$	4.5		0.17	0.26		0.33		
$ I_{IN} $	Input leakage current	$V_{IN}=V_{CC}$ or GND	5.5			0.1		1.0		1.0	μA
I_{CC}	Quiescent supply current	$V_{IN}=V_{CC}$ or GND $I_{out}=0\mu\text{A}$	5.5			2		20		40	μA

AC Characteristics for HC : $t_r=t_f=6\text{ns}$ $C_L=50\text{pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HC00		GD54HC00		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
$t_{PLH}/$ t_{PHL}	Propagation delay time nA, nB to nY	2.0 4.5 6.0		25 9 7	90 18 15		115 23 20		135 27 23	ns
$t_{TLH}/$ t_{THL}	Output transition time	2.0 4.5 6.0		18 7 6	72 14 13		95 19 16		110 22 19	ns

AC Characteristics for HCT : $t_r=t_f=6\text{ns}$ $C_L=50\text{pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HCT00		GD54HCT00		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
$t_{PLH}/$ t_{PHL}	Propagation delay time nA, nB, to nY	4.5		10	19		24		29	ns
$t_{TLH}/$ t_{THL}	Output transition time	4.5		7	15		19		22	ns

AC Waveform

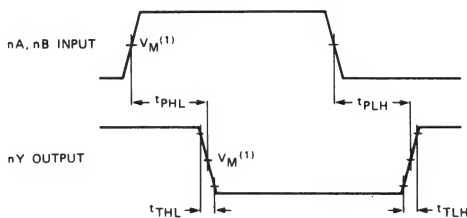


Fig. 3 Waveforms showing the input (nA, nB) to output (nY) propagation delays and the output transition times.

Note to AC waveform

- (1) HC : $V_M=50\%$, $V_I=GND$ to V_{CC}
HCT: $V_M=1.3V$; $V_I=GND$ to $3V$.

GD54/74HC02, GD54/74HCT02

QUAD 2-INPUT NOR GATES

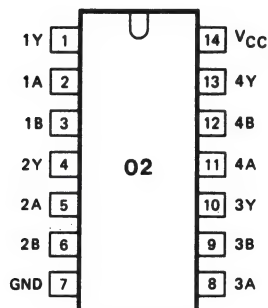
General Description

These devices are identical in pinout to the 54/74LS02. They contain four independent 2-input NOR gates. These devices are characterized for operation over wide temperature ranges to meet industry and military specifications.

Features

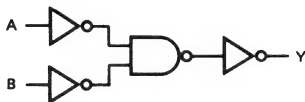
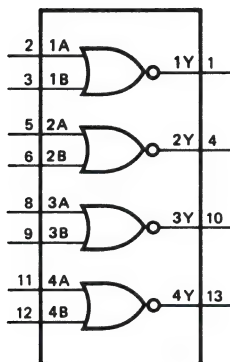
- Low Power consumption characteristic of CMOS devices
- Output drive capability: 10 LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts
for HCT 4.5 to 5.5 volts
- Low input current: $1\mu\text{A}$ Max.
- Low quiescent current: $20\mu\text{A}$ Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs

Pin Configuration



Suffix-Blank : Plastic Dual In Line Package
 Suffix-J : Ceramic Dual In Line Package
 Suffix-D : Small Outline Package

Logic Symbol and Logic Diagram



Function Table

INPUTS		OUTPUT
nA	nB	nY
L	L	H
L	H	L
H	L	L
H	H	L

H=HIGH voltage level
 L=LOW voltage level

Fig. 1 Logic Symbol

Fig. 2. Logic diagram (one gate)

Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC Supply voltage		-0.5	+7	V
I_{IK}, I_{OK}	DC input or output diode current	for $V_I < -0.5$ or $V_I > V_{CC} + 0.5V$		20	mA
I_O	DC output source or sink current	for $-0.5V < V_O < V_{CC} + 0.5V$		25	mA
I_{CC}	DC V_{CC} or GND current			50	mA
T_{stg}	Storage temperature range		-65	150	°C
P_D	Power dissipation per package	above +70°C: derate linearly with 8mW/K		500	mW
T_L	Lead temperature	At distance 1/16 ± 1/32 in. from case for 60 sec(CERAMIC) 10 sec(PLASTIC)		300 260	°C

Recommended Operating Conditions

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range V_{CC} : GD54/74HC Types GD54/74HCT Types	2 4.5	6 5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A : GD74 Types GD54 Types	-40 -55	+85 +125	°C
Input Rise and Fall times t_r, t_f : GD54/74HC Types at 2V at 4.5V at 6V GD54/74HCT Types at 4.5V		1000 500 400 500	ns

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HC02		GD54HC02		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2		1.5 3.15 4.2		V
V _{IL}	LOW level input voltage		2.0 4.5 6.0			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH}	I _{OH} =-20μA	2.0	1.9	2.0			1.9		V
				4.5	4.4	4.5			4.4		
		or V _{IL}	I _{OH} =-4mA I _{OH} =-5.2mA	6.0	5.9	6.0			5.9		
				4.5	3.98	4.3			3.84		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH}	I _{OL} =20μA	2.0			0.1	0.1		0.1	V
				4.5			0.1	0.1		0.1	
		or V _{IL}	I _{OL} =4mA I _{OL} =5.2mA	6.0			0.1	0.1		0.1	
				4.5		0.17	0.26	0.33		0.4	
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	6.0			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	6.0			2		20		40	μA

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HCT02		GD54HCT02		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		4.5 to 5.5	2.0			2.0		2.0		V
V _{IL}	LOW level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH}	I _{OH} =-20μA	4.5	4.4	4.5		4.4		4.4	V
		or V _{IL}	I _{OH} =-4mA	4.5	3.98	4.3		3.84		3.7	
V _{OL}	LOW level output voltage	V _{IN} =V _{IH}	I _{OL} =20μA	4.5			0.1	0.1		0.1	V
		or V _{IL}	I _{OL} =4mA	4.5		0.17	0.26	0.33		0.4	
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	5.5			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	5.5			2		20		40	μA

AC Characteristics for HC: $t_r=t_f=6\text{ns}$ $C_L=50\text{pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HC02		GD54HC02		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
$t_{PLH}/$ t_{PHL}	Propagation delay time nA, nB to nY	2.0 4.5 6.0		30 10 8	90 18 15		110 22 20		130 26 23	ns
$t_{TLH}/$ t_{THL}	Output transition time	2.0 4.5 6.0		25 8 7	70 15 13		85 18 16		100 22 19	ns

AC Characteristics for HCT: $t_r=t_f=6\text{ns}$ $C_L=50\text{pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HCT02		GD54HCT02		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
$t_{PLH}/$ t_{PHL}	Propagation delay time nA, nB, to nY	4.5		12 19			24		29	ns
$t_{TLH}/$ t_{THL}	Output transition time	4.5		8 15			19		22	ns

AC Waveform

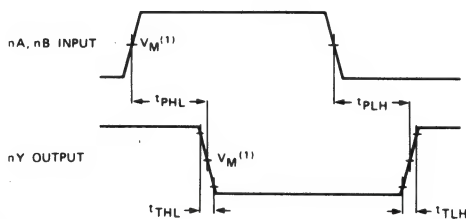


Fig. 3 Waveforms showing the input (nA, nB) to output (nY) propagation delays and the output transition times.

Note to AC waveform

- (1) HC : $V_M=50\%$, $V_I=\text{GND}$ to V_{CC}
HCT: $V_M=1.3\text{V}$; $V_I=\text{GND}$ to 3V

GD54/74HC03, GD54/74HCT03

QUAD 2-INPUT NAND GATES WITH OPEN-DRAIN OUTPUTS

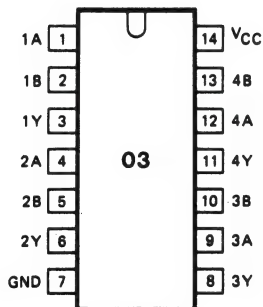
General Description

These devices are identical in pinout to the 54/74LS03. They contain four independent 2-Input NAND gates. The open-drain outputs require pull-up resistors to perform correctly. With suitable pull-up resistors, these devices can be used in active-low wired-OR or active-high wired-AND applications. These devices are characterized for operation over wide temperature ranges to meet industry and military specifications.

Features

- Low Power consumption characteristic of CMOS devices
- Output drive capability: 10 LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts
for HCT 4.5 to 5.5 volts
- Low input current: 1 μ A Max.
- Low quiescent current: 20 μ A Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs

Pin Configuration



Suffix-Blank : Plastic Dual In Line Package
 Suffix-J : Ceramic Dual In Line Package
 Suffix-D : Small Outline Package

Logic Symbol and Diagram

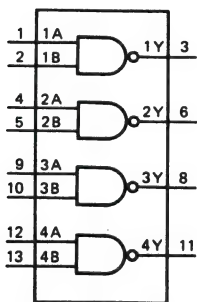


Fig. 1 Logic symbol

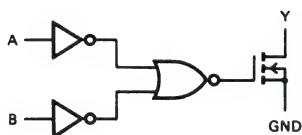


Fig. 2 Logic diagram (one gate)

Function Table

INPUTS		OUTPUT
nA	nB	nY
L	L	Z
L	H	Z
H	L	Z
H	H	L

H=HIGH voltage level
 L=LOW voltage level
 Z=high impedance OFF-state

Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC Supply voltage		-0.5	+7	V
I_{IK}, I_{OK}	DC input or output diode current	for $V_I < -0.5$ or $V_I > V_{CC} + 0.5V$		20	mA
I_O	DC output source or sink current	for $-0.5V < V_O < V_{CC} + 0.5V$		25	mA
I_{CC}	DC V_{CC} or GND current			50	mA
T_{stg}	Storage temperature range		-65	150	°C
P_D	Power dissipation per package	above +70°C: derate linearly with 8mW/K		500	mW
T_L	Lead temperature	At distance 1/16 ± 1/32 in. from case for 60 sec(CERAMIC) 10 sec(PLASTIC)		300 260	°C

Recommended Operating Conditions

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range V_{CC} : GD54/74HC Types GD54/74HCT Types	2 4.5	6 5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A : GD74 Types GD54 Types	-40 -55	+85 +125	°C
Input Rise and Fall times t_r, t_f : GD54/74HC Types at 2V at 4.5V at 6V GD54/74HCT Types at 4.5V		1000 500 400 500	ns

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HC03		GD54HC03		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2		1.5 3.15 4.2		V
V _{IL}	LOW level input voltage		2.0 4.5 6.0			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH}	I _{OH} =-20μA	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0	1.9 4.4 5.9		1.9 4.4 5.9		V
			I _{OH} =-4mA I _{OH} =-5.2mA	4.5 6.0	3.98 5.48	4.3 5.2	3.84 5.34		3.7 5.2		
		or V _{IL}	I _{OL} =20μA	2.0 4.5 6.0			0.1 0.1 0.1	0.1 0.1 0.1		0.1 0.1 0.1	V
			I _{OL} =4mA I _{OL} =5.2mA	4.5 6.0		0.17 0.15	0.26 0.26	0.33 0.33		0.4 0.4	
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	6.0			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	6.0			2		20		40	μA
I _{OH}	HIGH level output current	V _{IN} =V _{IH} or V _{IL} V _{out} =V _{CC}	6.0		0.01	0.5		5		10	μA

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HCT03		GD54HCT03		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		4.5 to 5.5	2.0			2.0		2.0		V
V _{IL}	LOW level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH} or V _{IL}	I _{OH} =-20μA	4.5	4.4	4.5	4.4		4.4		V
			I _{OH} =-4mA	4.5	3.98	4.3	3.84		3.7		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH} or V _{IL}	I _{OL} =20μA	4.5			0.1	0.1		0.1	V
			I _{OL} =4mA	4.5		0.17	0.26	0.33		0.4	
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	5.5			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	5.5			2		20		40	μA
I _{OH}	HIGH level output current	V _{IN} =V _{IH} or V _{IL} V _{out} =V _{CC}	4.5 to 5.5		0.01	0.5		5		10	μA

AC Characteristics for HC: $t_r=t_f=6\text{ns}$ $C_L=50\text{pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HC03		GD54HC03		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
$t_{PZL}/$ t_{PLZ}	Propagation delay time nA, nB to nY	2.0 4.5 6.0		25 9 8	90 18 15		110 22 20		130 26 23	ns
t_{THL}	Output transition time	2.0 4.5 6.0		25 8 7	70 15 13		85 18 16		100 22 19	ns

AC Characteristics for HCT: $t_r=t_f=6\text{ns}$ $C_L=50\text{pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HCT03		GD53HCT03		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
$t_{PZL}/$ t_{PLZ}	Propagation delay time nA, nB, to nY	4.5		12	20		24		28	ns
t_{THL}	Output transition time	4.5		8	15		19		22	ns

AC Waveform

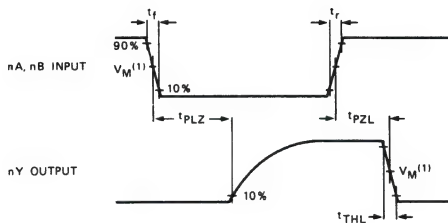


Fig. 3 Waveforms showing the input (nA, nB) to output (nY) propagation delays and the output transition times.

Note to AC waveform

- (1) HC : $V_M=50\%$, $V_I=\text{GND to } V_{CC}$
HCT: $V_M=1.3V$; $V_I=\text{GND to } 3V$.

GD54/74HC04, GD54/74HCT04

HEX INVERTERS

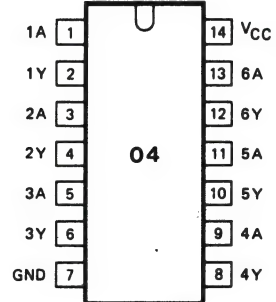
General Description

These devices are identical in pinout to the 54/74LS04. They contain six independent inverters. These devices are characterized for operation over wide temperature ranges to meet industry and military specifications.

Features

- Low Power consumption characteristic of CMOS devices
- Output drive capability: 10 LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts
for HCT 4.5 to 5.5 volts
- Low input current: 1 μ A Max.
- Low quiescent current: 20 μ A Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs

Pin Configuration



Suffix-Blank : Plastic Dual In Line Package
 Suffix-J : Ceramic Dual In Line Package
 Suffix-D : Small Outline Package

Logic Diagram

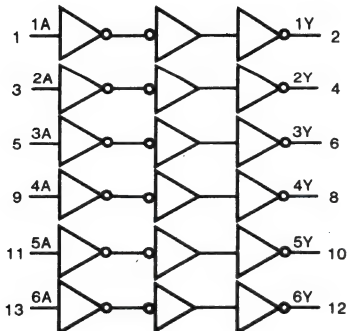


Fig. 1 Logic diagram

Function Table

INPUT	OUTPUT
nA	nY
L	H
H	L

H=HIGH Voltage level
 L=LOW Voltage level

Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC Supply voltage		-0.5	+7	V
I_{IK}, I_{OK}	DC input or output diode current	for $V_I < -0.5$ or $V_I > V_{CC} + 0.5V$		20	mA
I_O	DC output source or sink current	for $-0.5V < V_O < V_{CC} + 0.5V$		25	mA
I_{CC}	DC V_{CC} or GND current			50	mA
T_{stg}	Storage temperature range		-65	150	°C
P_D	Power dissipation per package	above +70°C: derate linearly with 8mW/K		500	mW
T_L	Lead temperature	At distance 1/16 ± 1/32 in. from case for 60 sec(CERAMIC) 10 sec(PLASTIC)		300 260	°C

Recommended Operating Conditions

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range V_{CC} : GD54/74HC Types	2	6	V
GD54/74HCT Types	4.5	5.5	
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A : GD74 Types	-40	+85	°C
GD54 Types	-55	+125	
Input Rise and Fall times t_r, t_f : GD54/74HC Types at 2V		1000	ns
at 4.5V		500	
at 6V		400	
GD54/74HCT Types at 4.5V		500	

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HC04		GD54HC04		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2		1.5 3.15 4.2		V
V _{IL}	LOW level input voltage		2.0 4.5 6.0			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH}	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V
		or V _{IL}									
			I _{OH} =-20μA I _{OH} =-4mA I _{OH} =-5.2mA	4.5 3.98 5.48	4.3 5.2		3.84 5.34		3.7 5.2		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH}	2.0 4.5 6.0			0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V
		or V _{IL}									
			I _{OL} =20μA I _{OL} =4mA I _{OL} =5.2mA	4.5 0.17 0.15	0.26 0.26		0.33 0.33		0.4 0.4		
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	6.0			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	6.0			2		20		40	μA

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HCT04		GD54HCT04		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		4.5 to 5.5	2.0			2.0		2.0		V
V _{IL}	LOW level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH}	4.5	4.4	4.5		4.4		4.4		V
		or V _{IL}	I _{OH} =-20μA I _{OH} =-4mA	4.5 3.98	4.3		3.84		3.7		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH}	4.5			0.1		0.1		0.1	V
		or V _{IL}	I _{OL} =20μA I _{OL} =4mA	4.5	0.17	0.26		0.33		0.4	
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	5.5			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	5.5			2		20		40	μA

AC Characteristics for HC: $t_r=t_f=6\text{ns}$ $C_L=50\text{pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HC04		GD54HC04		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
$t_{PLH}/$ t_{PHL}	Propagation delay time nA nY	2.0 4.5 6.0		25 8 7	80 16 14		105 21 18		125 26 23	ns
$t_{TLH}/$ t_{THL}	Output transition time	2.0 4.5 6.0		25 8 7	70 15 13		85 18 16		100 22 19	ns

AC Characteristics for HCT: $t_r=t_f=6\text{ns}$ $C_L=50\text{pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HCT04		GD54HCT04		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
$t_{PLH}/$ t_{PHL}	Propagation delay time nA to nY	4.5		10	20		24		29	ns
$t_{TLH}/$ t_{THL}	Output transition time	4.5		8	15		19		22	ns

AC Waveform

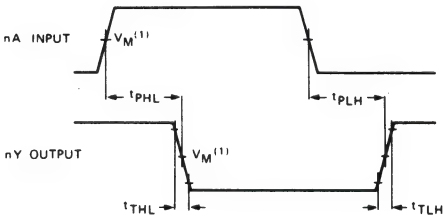


Fig. 2 Waveforms showing the input (nA) to output (nY) propagation delays and the output transition times.

Note to AC waveform

- (1) HC : $V_M=50\%$, $V_L=GND$ to V_{CC}
HCT: $V_M=1.3V$, $V_L=GND$ to $3V$.

GD54/74HCU04

HEX UNBUFFERED INVERTERS

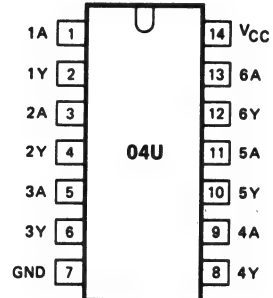
General Description

These devices are identical in pinout to the 54/74 LSO4. They contain six independent unbuffered inverters. These inverters are well suited for use as oscillators, pulse shapers and in many other applications requiring a high-input impedance amplifier. These devices are characterized for over wide temperature ranges to meet industry and ation over military specifications.

Features

- Low Power consumption characteristic of CMOS devices
- Output drive capability: 10 LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts
for HCT 4.5 to 5.5 volts
- Low input current: 1 μ A Max.
- Low quiescent current: 20 μ A Max. (74HCU)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs

Pin Configuration



Suffix-Blank : Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package
Suffix-D : Small Outline Package

Logic Diagram

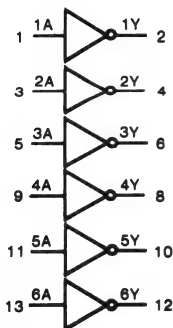


Fig. 1 Logic diagram

Function Table

INPUT	OUTPUT
nA	nY
L	H
H	L

H=HIGH Voltage level
L=LOW Voltage level

Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC Supply voltage		-0.5	+7	V
I_{IK}, I_{OK}	DC input or output diode current	for $V_I < -0.5$ or $V_I > V_{CC} + 0.5V$		20	mA
I_O	DC output source or sink current	for $-0.5V < V_O < V_{CC} + 0.5V$		25	mA
I_{CC}	DC V_{CC} or GND current			50	mA
T_{stg}	Storage temperature range		-65	150	°C
P_D	Power dissipation per package	above +70°C: derate linearly with 8mW/K		500	mW
T_L	Lead temperature	At distance 1/16 ± 1/32 in. from case for 60 sec(CERAMIC) 10 sec(PLASTIC)		300 260	°C

Recommended Operating Conditions

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range V_{CC} : GD54/74HC Types GD54/74HCT Types	2 4.5	6 5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A : GD74 Types GD54 Types	-40 -55	+85 +125	°C
Input Rise and Fall times t_r, t_f : GD54/74HC Types at 2V at 4.5V at 6V GD54/74HCT Types at 4.5 V		1000 500 400 500	ns

DC Electrical Characteristics for HCU: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER	TEST CONDITION	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HCU04		GD54HCU04		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V_{IH}	HIGH level input Voltage		2.0 4.5 6.0	1.7 3.6 4.8			1.7 3.6 4.8		1.7 3.6 4.8		V
V_{IL}	LOW level input voltage		2.0 4.5 6.0			0.3 0.8 1.1		0.3 0.8 1.1		0.3 0.8 1.1	V
V_{OH}	HIGH level output voltage	$V_{IN}=V_{IH}$	$I_{OH}=-20\mu\text{A}$	2.0 4.5 6.0	1.8 4.0 5.5		1.8 4.0 5.5		1.8 4.0 5.5		V
			$I_{OH}=-4\text{mA}$	4.5 6.0	3.98 5.48		3.84 5.34		3.7 5.2		
		or V_{IL}	$I_{OH}=-20\mu\text{A}$	2.0 4.5 6.0		0.2 0.5 0.5		0.2 0.5 0.5		0.2 0.5 0.5	
			$I_{OL}=4\text{mA}$ $I_{OL}=5.2\text{mA}$	4.5 6.0		0.26 0.26		0.33 0.33		0.4 0.4	
I_{IN}	Input leakage Current	$V_{IN}=V_{CC}$ or GND	6.0			0.1		1.0		1.0	μA
I_{CC}	Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{out}=0\mu\text{A}$	6.0			2		20		40	μA

AC Characteristics for HCU: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HCU04		GD54HCU04		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
$t_{PLH}/$ t_{PHL}	Propagation Delay Time nA to nY	2.0 4.5 6.0		23 7 6	75 15 13		95 19 16		110 22 19	ns
$t_{TLH}/$ t_{THL}	Output Transition Time	2.0 4.5 6.0		25 8 7	70 15 13		85 18 16		100 22 19	ns

AC Waveforms

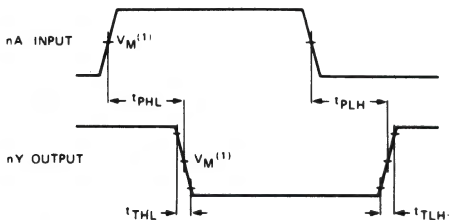


Fig. 2 Waveforms showing the input (nA) to output (nY) propagation delays and the output transition times.

Note to AC waveform

(1) HCU: $V_M=50\%$, $V_I=\text{GND}$ to V_{CC}

GD54/74HC05, GD54/74HCT05

HEX INVERTERS WITH OPEN-DRAIN OUTPUTS

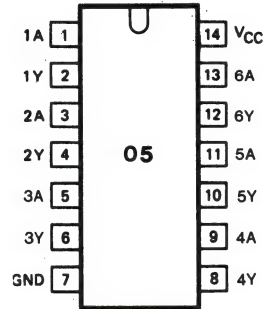
General Description

These devices are identical in pinout to the 54/74LS05. They contain six independent INVERTERS. The open-drain outputs require pull-up resistors to perform correctly. With suitable pull-up resistors, these devices can be used in active-low wired-OR or active-high wired-AND applications. These devices are characterized for operation over wide temperature ranges to meet industry and military specifications.

Features

- Low Power consumption characteristic of CMOS devices
- Output drive capability: 10 LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts
for HCT 4.5 to 5.5 volts
- Low input current: $1\mu\text{A}$ Max.
- Low quiescent current: $20\mu\text{A}$ Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs

Pin Configuration



Suffix-Blank : Plastic Dual In Line Package
 Suffix-J : Ceramic Dual In Line Package
 Suffix-D : Small Outline Package

Logic Diagram Typical Application

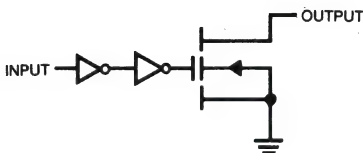


Fig. 1 Logic diagram (one gate)

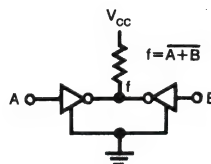


Fig. 2 Typical application

Function Table

INPUT	OUTPUT
nA	nY
H	L
L	Z

H= HIGH voltage level
 L= LOW voltage level
 Z= HIGH impedance OFF-state

Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC Supply voltage		-0.5	+7	V
I_{IK}, I_{OK}	DC input or output diode current	for $V_I < -0.5$ or $V_I > V_{CC} + 0.5V$		20	mA
I_O	DC output source or sink current	for $-0.5V < V_O < V_{CC} + 0.5V$		25	mA
I_{CC}	DC V_{CC} or GND current			50	mA
T_{sig}	Storage temperature range		-65	150	°C
P_D	Power dissipation per package	above +70°C: derate linearly with 8mW/K		500	mW
T_L	Lead temperature	At distance 1/16 ± 1/32 in. from case for 60 sec(CERAMIC) 10 sec(PLASTIC)		300 260	°C

Recommended Operating Conditions

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range V_{CC} : GD54/74HC Types GD54/74HCT Types	2 4.5	6 5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A : GD74 Types GD54 Types	-40 -55	+85 +125	°C
Input Rise and Fall times t_r, t_f : GD54/74HC Types at 2V at 4.5V at 6V GD54/74HCT Types at 4.5V		1000 500 400 500	ns

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HC05		GD54HC05		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2		1.5 3.15 4.2		V
V _{IL}	LOW level input voltage		2.0 4.5 6.0			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH}	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V
		or V _{IL}									
			I _{OH} =-20μA I _{OH} =-4mA I _{OH} =-5.2mA	4.5 3.98 6.0	4.3 5.2		3.84 5.34		3.7 5.2		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH}	2.0 4.5 6.0			0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V
		or V _{IL}									
			I _{OL} =20μA I _{OL} =4mA I _{OL} =5.2mA	4.5 6.0	0.17 0.15	0.26 0.26		0.33 0.33		0.4 0.4	
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	6.0			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	6.0			2		20		40	μA
I _{OH}	HIGH level output current	V _{IN} =V _{IH} or V _{IL} V _{out} =V _{CC}	6.0		0.01	0.5		5		10	μA

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HCT05		GD54HCT05		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		4.5 to 5.5	2.0			2.0		2.0		V
V _{IL}	LOW level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH}	4.5	4.4	4.5		4.4		4.4		V
		or V _{IL}	I _{OH} =-20μA I _{OH} =-4mA	4.5	3.98	4.3	3.84		3.7		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH}	4.5			0.1		0.1		0.1	V
		or V _{IL}	I _{OL} =20μA I _{OL} =4mA	4.5		0.17	0.26		0.33	0.4	
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	5.5			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	5.5			2		20		40	μA
I _{OH}	HIGH level output current	V _{IN} =V _{IH} or V _{IL} V _{out} =V _{CC}	4.5 to 5.5		0.01	0.5		5		10	μA

AC Characteristics for HC: $t_r = t_f = 6\text{ns}$ $C_L = 50\text{pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A = 25^\circ\text{C}$			GD74HC05		GD54HC05		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
$t_{PZL}/$ t_{PLZ}	Propagation delay time nA to nY	2.0 4.5 6.0		25 8 7	80 16 14		105 21 18		125 26 23	ns
t_{THL}	Output transition time	2.0 4.5 6.0		25 8 7	70 15 13		85 18 16		100 22 19	ns

AC Characteristics for HCT: $t_r = t_f = 6\text{ns}$ $C_L = 50\text{pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A = 25^\circ\text{C}$			GD74HCT05		GD54HCT05		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
$t_{PZL}/$ t_{PLZ}	Propagation delay time nA to nY	4.5		10	20		24		29	ns
t_{THL}	Output transition time	4.5		8	15		19		22	ns

AC Waveform

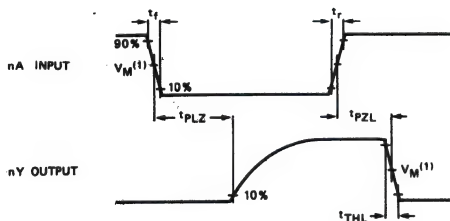


Fig. 3 Waveforms showing the input (nA) to output (nY) propagation delays and the output transition times.

Note to AC waveform

- (1) HC : $V_M = 50\%$, $V_I = \text{GND to } V_{CC}$
HCT: $V_M = 1.3\text{V}$, $V_I = \text{GND to } 3\text{V}$.

GD54/74HC08, GD54/74HCT08

QUAD 2-INPUT AND GATES

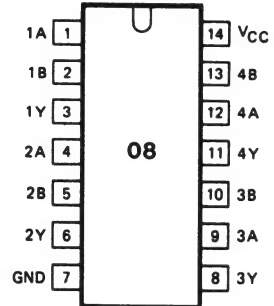
General Description

These devices are identical in pinout to the 54/74LS08. They contain four independent 2-input AND gates. These devices are characterized for operation over wide temperature ranges to meet industry and military specifications.

Features

- Low Power consumption characteristic of CMOS devices
- Output drive capability: 10 LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts
for HCT 4.5 to 5.5 volts
- Low input current: 1 μ A Max.
- Low quiescent current: 20 μ A Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs

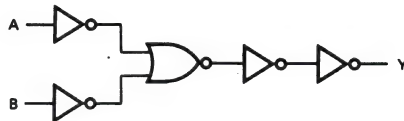
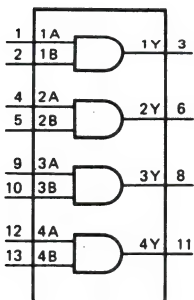
Pin Configuration



Suffix-Blank : Plastic Dual In Line Package
 Suffix-J : Ceramic Dual In Line Package
 Suffix-D : Small Outline Package

Logic Symbol and Logic Diagram

Function Table



INPUTS		OUTPUT
nA	nB	nY
L	L	L
L	H	L
H	L	L
H	H	H

H= HIGH voltage level
 L= LOW voltage level

Fig. 1 Logic symbol

Fig. 2 Logic diagram (one gate)

Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC Supply voltage		-0.5	+7	V
I_{IK}, I_{OK}	DC input or output diode current	for $V_I < -0.5$ or $V_I > V_{CC} + 0.5V$		20	mA
I_O	DC output source or sink current	for $-0.5V < V_O < V_{CC} + 0.5V$		25	mA
I_{CC}	DC V_{CC} or GND current			50	mA
T_{stg}	Storage temperature range		-65	150	°C
P_D	Power dissipation per package	above +70°C: derate linearly with 8mW/K		500	mW
T_L	Lead temperature	At distance 1/16 ± 1/32 in. from case for 60 sec(CERAMIC) 10 sec(PLASTIC)		300 260	°C

Recommended Operating Conditions

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range V_{CC} : GD54/74HC Types GD54/74HCT Types	2 4.5	6 5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A : GD74 Types GD54 Types	-40 -55	+85 +125	°C
Input Rise and Fall times t_r, t_f : GD54/74HC Types at 2V at 4.5V at 6V GD54/74HCT Types at 4.5V		1000 500 400 500	ns

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HC08		GD54HC08		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2		1.5 3.15 4.2		V
V _{IL}	LOW level input voltage		2.0 4.5 6.0			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH} or V _{IL}	I _{OH} =-20μA	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0	1.9 4.4 5.9		1.9 4.4 5.9		V
			I _{OH} =-4mA I _{OH} =-5.2mA	4.5 6.0	3.98 5.48	4.3 5.2	3.84 5.34		3.7 5.2		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH} or V _{IL}	I _{OL} =20μA	2.0 4.5 6.0			0.1 0.1 0.1	0.1 0.1 0.1		0.1 0.1 0.1	V
			I _{OL} =4mA I _{OL} =5.2mA	4.5 6.0		0.17 0.15	0.26 0.26	0.33 0.33		0.4 0.4	
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	6.0			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	6.0			2		20		40	μA

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HCT08		GD54HCT08		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		4.5 to 5.5	2.0			2.0		2.0		V
V _{IL}	LOW level Input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH} or V _{IL}	I _{OH} =-20μA	4.5	4.4	4.5	4.4		4.4		V
			I _{OH} =-4mA	4.5	3.98	4.3	3.84		3.7		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH} or V _{IL}	I _{OL} =20μA	4.5			0.1	0.1		0.1	V
			I _{OL} =4mA	4.5		0.17	0.26	0.33		0.4	
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	5.5			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	5.5			2		20		40	μA

AC Characteristics for HC: $t_r=t_f=6\text{ns}$ $C_L=50\text{pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HC08		GD54HC08		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
$t_{PLH}/$ t_{PHL}	Propagation delay time nA, nB to nY	2.0 4.5 6.0		25 9 7	90 18 15		115 23 20		135 27 23	ns
$t_{TLH}/$ t_{THL}	Output transition time	2.0 4.5 6.0		19 7 6	75 15 13		95 19 16		110 22 19	ns

AC Characteristics for HCT: $t_r=t_f=6\text{ns}$ $C_L=50\text{pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HCT08		GD54HCT08		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
$t_{PLH}/$ t_{PHL}	Propagation delay time nA, nB, to nY	4.5		14	24		30		36	ns
$t_{TLH}/$ t_{THL}	Output transition time	4.5		7	15		19		22	ns

AC Waveform

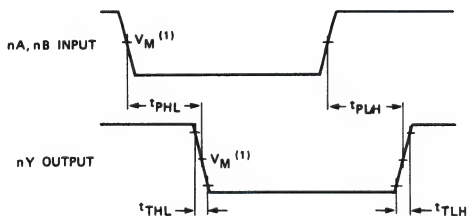


Fig. 3 Waveforms showing the input (nA, nB) to output (nY) propagation delays and the output transition times.

Note to AC waveform

- (1) HC : $V_M=50\%$, $V_I=\text{GND to } V_{CC}$
HCT: $V_M=1.3\text{V}$, $V_I=\text{GND to } 3\text{V}$.

GD54/74HC09, GD54/74HCT09

QUAD 2-INPUT AND GATES WITH OPEN-DRAIN OUTPUTS

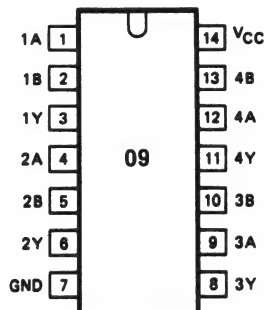
General Description

These devices are identical in pinout to the 54/74LS09. They contain four independent 2-Input AND gates. The open-drain outputs require pull-up resistors to perform correctly. With suitable pull-up resistors, these devices can be used in active-low wired-OR or active-high wired-AND applications. These devices are characterized for operation over wide temperature ranges to meet industry and military specifications.

Features

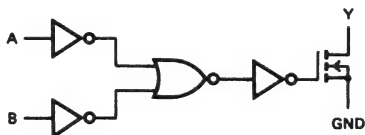
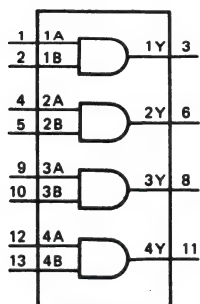
- Low Power consumption characteristic of CMOS devices
- Output drive capability: 10 LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts
for HCT 4.5 to 5.5 volts
- Low input current: 1 μ A Max.
- Low quiescent current: 20 μ A Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs

Pin Configuration



Suffix-Blank : Plastic Dual In Line Package
 Suffix-J : Ceramic Dual In Line Package
 Suffix-D : Small Outline Package

Logic Symbol and Diagram



Function Table

OUTPUTS		OUTPUT
nA	nB	nY
H	H	Z
L	X	L
X	L	L

H= HIGH voltage level
 L= LOW voltage level
 X= don't care

Fig. 1 Logic symbol

Fig. 2 Logic diagram (one gate)

Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC Supply voltage		-0.5	+7	V
I_{IK}, I_{OK}	DC input or output diode current	for $V_I < -0.5$ or $V_I > V_{CC} + 0.5V$		20	mA
I_O	DC output source or sink current	for $-0.5V < V_O < V_{CC} + 0.5V$		25	mA
I_{CC}	DC V_{CC} or GND current			50	mA
T_{sig}	Storage temperature range		-65	150	°C
P_D	Power dissipation per package	above +70°C: derate linearly with 8mW/K		500	mW
T_L	Lead temperature	At distance 1/16 ± 1/32 in. from case for 60 sec(CERAMIC) 10 sec(PLASTIC)		300 260	°C

Recommended Operating Conditions

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range V_{CC} : GD54/74HC Types GD54/74HCT Types	2 4.5	6 5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A : GD74 Types GD54 Types	-40 -55	+85 +125	°C
Input Rise and Fall times t_r, t_f : GD54/74HC Types at 2V at 4.5V at 6V GD54/74HCT Types at 4.5V		1000 500 400 500	ns

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A = 25 °C			GD74HC09		GD54HC09		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2		1.5 3.15 4.2		V
V _{IL}	LOW level input voltage		2.0 4.5 6.0			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V
V _{OH}	HIGH level output voltage	V _{IN} = V _{IH}	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V
		or V _{IL}									
			I _{OH} = -20 μA I _{OH} = -4 mA I _{OH} = -5.2 mA	4.5 3.98 5.48	4.3 5.2		3.84 5.34		3.7 5.2		
V _{OL}	LOW level output voltage	V _{IN} = V _{IH}	2.0 4.5 6.0			0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V
		or V _{IL}									
			I _{OL} = 20 μA I _{OL} = 4 mA I _{OL} = 5.2 mA	4.5 0.17 0.15	0.26 0.26		0.33 0.33		0.4 0.4		
I _{IN}	Input leakage Current	V _{IN} = V _{CC} or GND	6.0			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} = V _{CC} or GND I _{out} = 0 μA	6.0			2		20		40	μA
I _{OH}	HIGH level output current	V _{IN} = V _{IH} or V _{IL} V _{out} = V _{CC}	6.0		0.01	0.5		5		10	μA

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A = 25 °C			GD74HCT09		GD54HCT09		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		4.5 to 5.5	2.0			2.0		2.0		V
V _{IL}	LOW level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V _{OH}	HIGH level output voltage	V _{IN} = V _{IH}	4.5	4.4	4.5		4.4		4.4		V
		or V _{IL}									
			I _{OH} = -20 μA I _{OH} = -4 mA	4.5 3.98	4.3		3.84		3.7		
V _{OL}	LOW level output voltage	V _{IN} = V _{IH}	4.5			0.1		0.1		0.1	V
		or V _{IL}									
			I _{OL} = 20 μA I _{OL} = 4 mA	4.5 0.17	0.26		0.33		0.4		
I _{IN}	Input leakage Current	V _{IN} = V _{CC} or GND	5.5			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} = V _{CC} or GND I _{out} = 0 μA	5.5			2		20		40	μA
I _{OH}	HIGH level output current	V _{IN} = V _{IH} or V _{IL} V _{out} = V _{CC}	4.5 to 5.5		0.01	0.5		5		10	μA

AC Characteristics for HC: $t_r=t_f=6\text{ns}$ $C_L=50\text{pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HC09		GD54HC09		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
$t_{PZL}/$ t_{PLZ}	Propagation delay time nA, nB to nY	2.0 4.5 6.0		25 9 8	90 18 15		110 22 20		130 26 23	ns
t_{THL}	Output transition time	2.0 4.5 6.0		25 8 7	70 15 13		85 18 16		100 22 19	ns

AC Characteristics for HCT: $t_r=t_f=6\text{ns}$ $C_L=50\text{pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HCT09		GD54HCT09		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
$t_{PZL}/$ t_{PLZ}	Propagation delay time nA, nB, to nY	4.5		12	20		24		28	ns
t_{THL}	Output transition time	4.5		8	15		19		22	ns

AC Waveform

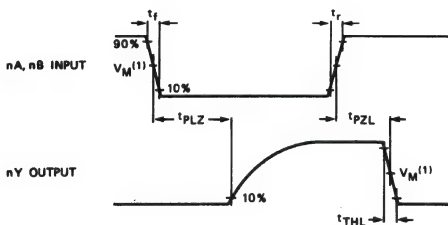


Fig. 3 Waveforms showing the input (nA, nB) to output (nY) propagation delays and the output transition times.

Note to AC waveform

- (1) HC : $V_M=50\%$, $V_I=\text{GND to } V_{CC}$
HCT: $V_M=1.3\text{V}$, $V_I=\text{GND to } 3\text{V}$.

GD54/74HC10, GD54/74HCT10

TRIPLE 3-INPUT NAND GATES

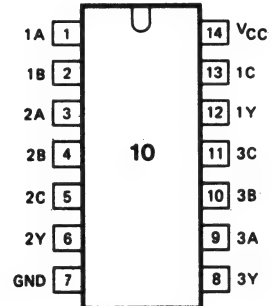
General Description

These devices are identical in pinout to the 54/74LS10. They contain three independent 3-input NAND gates. These devices are characterized for operation over wide temperature ranges to meet industry and military specifications.

Features

- Low Power consumption characteristic of CMOS devices
- Output drive capability: 10 LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts for HCT 4.5 to 5.5 volts
- Low input current: 1 μ A Max.
- Low quiescent current: 20 μ A Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs

Pin Configuration



Suffix-Blank : Plastic Dual In Line Package
 Suffix-J : Ceramic Dual In Line Package
 Suffix-D : Small Outline Package

Logic Symbol and Diagram

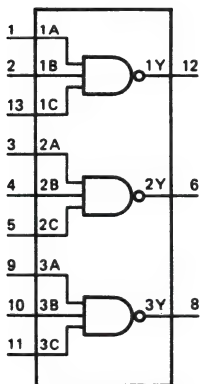


Fig. 1 Logic symbol

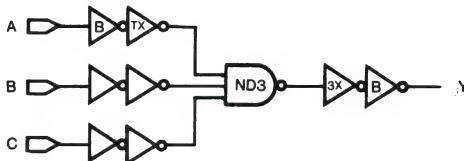


Fig. 2 Logic diagram (one gate)

Function Table

INPUT			OUTPUT
nA	nB	nC	nY
L	L	L	H
L	L	H	H
L	H	L	H
L	H	H	H
H	L	L	H
H	L	H	H
H	H	L	H
H	H	H	L

H=HIGH Voltage level
 L=LOW Voltage level

Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC Supply voltage		-0.5	+7	V
I_{IK}, I_{OK}	DC input or output diode current	for $V_I < -0.5$ or $V_I > V_{CC} + 0.5V$		20	mA
I_O	DC output source or sink current	for $-0.5V < V_O < V_{CC} + 0.5V$		25	mA
I_{CC}	DC V_{CC} or GND current			50	mA
T_{stg}	Storage temperature range		-65	150	°C
P_D	Power dissipation per package	above +70°C: derate linearly with 8mW/K		500	mW
T_L	Lead temperature	At distance 1/16 ± 1/32 in. from case for 60 sec(CERAMIC) 10 sec(PLASTIC)		300 260	°C

Recommended Operating Conditions

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range V_{CC} : GD54/74HC Types GD54/74HCT Types	2 4.5	6 5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A : GD74 Types GD54 Types	-40 -55	+85 +125	°C
Input Rise and Fall times t_r, t_f : GD54/74HC Types at 2V at 4.5V at 6V GD54/74HCT Types at 4.5V		1000 500 400 500	ns

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HC10		GD54HC10		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2		1.5 3.15 4.2		V
V _{IL}	LOW level input voltage		2.0 4.5 6.0			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH}	I _{OH} =-20μA	2.0	1.9	2.0	1.9		1.9		V
				4.5	4.4	4.5	4.4		4.4		
		or V _{IL}	I _{OH} =-4mA I _{OH} =-5.2mA	6.0	5.9	6.0	5.9		5.9		
				4.5	3.98	4.3	3.84		3.7		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH}	I _{OL} =20μA	2.0			0.1	0.1		0.1	V
				4.5			0.1	0.1		0.1	
		or V _{IL}	I _{OL} =4mA I _{OL} =5.2mA	6.0			0.1	0.1		0.1	
				4.5		0.17	0.26	0.33		0.4	
				6.0		0.15	0.26	0.33		0.4	
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	6.0			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	6.0			2		20		40	μA

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HCT10		GD54HCT10		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		4.5 to 5.5	2.0			2.0		2.0		V
V _{IL}	LOW level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH}	I _{OH} =-20μA	4.5	4.4	4.5	4.4		4.4		V
				4.5	3.98	4.3	3.84		3.7		
		or V _{IL}	I _{OH} =-4mA	4.5							
				4.5							
V _{OL}	LOW level output voltage	V _{IN} =V _{IH}	I _{OL} =20μA	4.5			0.1	0.1		0.1	V
				4.5							
		or V _{IL}	I _{OL} =4mA	4.5		0.17	0.26	0.33		0.4	
				4.5							
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	5.5			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	5.5			2		20		40	μA

AC Characteristics for HC: $t_r=t_f=6\text{ns}$ $C_L=50\text{pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HC10		GD54HC10		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
$t_{PLH}/$ t_{PHL}	Propagation delay time nA, nB, nC to nY	2.0 4.5 6.0		28 10 8	90 18 15		120 22 19		145 28 24	ns
$t_{TLH}/$ t_{THL}	Output transition time	2.0 4.5 6.0		19 7 6	75 15 13		95 19 16		110 22 19	ns

AC Characteristics for HCT: $t_r=t_f=6\text{ns}$ $C_L=50\text{pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HCT10		GD54HCT10		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
$t_{PLH}/$ t_{PHL}	Propagation delay time nA, nB, nC to nY	4.5		14	24		30		36	ns
$t_{TLH}/$ t_{THL}	Output transition time	4.5		7	15		19		22	ns

AC Waveform

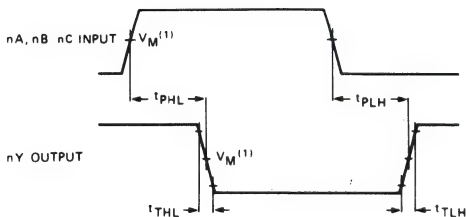


Fig. 3 Waveforms showing the input (nA, nB, nC) to output (nY) propagation delays and the output transition times.

Note to AC waveform

(1) HC : $V_M=50\%$, $V_I=GND$ to V_{CC}

HCT: $V_M=1.3V$, $V_I=GND$ to $3V$.

GD54/74HC11, GD54/74HCT11

TRIPLE 3-INPUT AND GATES

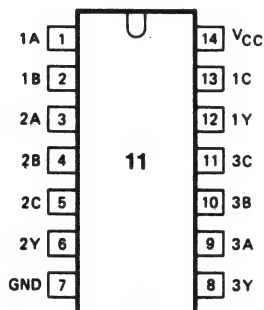
General Description

These devices are identical in pinout to the 54/74LS11. They contain three independent 3-input AND gates. These devices are characterized for operation over wide temperature ranges to meet industry and military specifications.

Features

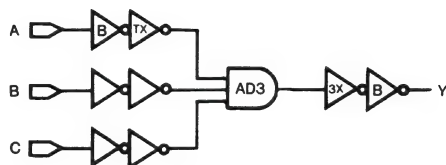
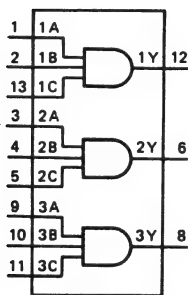
- Low Power consumption characteristic of CMOS devices
- Output drive capability: 10 LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts
for HCT 4.5 to 5.5 volts
- Low input current: 1 μ A Max.
- Low quiescent current: 20 μ A Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs

Pin Configuration



Suffix-Blank : Plastic Dual In Line Package
 Suffix-J : Ceramic Dual In Line Package
 Suffix-D : Small Outline Package

Logic Symbol and Diagram



Function Table

INPUT			OUTPUT
nA	nB	nC	nY
L	L	L	L
L	L	H	L
L	H	L	L
L	H	H	L
H	L	L	L
H	L	H	L
H	H	L	L
H	H	H	H

H=HIGH Voltage level
 L=LOW Voltage level

Fig. 1 Logic symbol

Fig. 2 Logic diagram (one gate)

Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC Supply voltage		-0.5	+7	V
I_{IK}, I_{OK}	DC input or output diode current	for $V_I < -0.5$ or $V_I > V_{CC} + 0.5V$		20	mA
I_O	DC output source or sink current	for $-0.5V < V_O < V_{CC} + 0.5V$		25	mA
I_{CC}	DC V_{CC} or GND current			50	mA
T_{stg}	Storage temperature range		-65	150	°C
P_D	Power dissipation per package	above +70°C: derate linearly with 8mW/K		500	mW
T_L	Lead temperature	At distance 1/16 ± 1/32 in. from case for 60 sec(CERAMIC) 10 sec(PLASTIC)		300 260	°C

Recommended Operating Conditions

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range V_{CC} : GD54/74HC Types GD54/74HCT Types	2 4.5	6 5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A : GD74 Types GD54 Types	-40 -55	+85 +125	°C
Input Rise and Fall times t_r, t_f : GD54/74HC Types at 2V at 4.5V at 6V GD54/74HCT Types at 4.5V		1000 500 400 500	ns

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HC11		GD54HC11		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2		1.5 3.15 4.2		V
V _{IL}	LOW level input voltage		2.0 4.5 6.0			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH}	I _{OH} =−20μA	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0	1.9 4.4 5.9		1.9 4.4 5.9		V
		or V _{IL}	I _{OH} =−4mA I _{OH} =−5.2mA	4.5 6.0	3.98 5.48	4.3 5.2	3.84 5.34		3.7 5.2		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH}	I _{OL} =20μA	2.0 4.5 6.0			0.1 0.1 0.1	0.1 0.1 0.1		0.1 0.1 0.1	V
		or V _{IL}	I _{OL} =4mA I _{OL} =5.2mA	4.5 6.0		0.17 0.15	0.26 0.26	0.33 0.33		0.4 0.4	
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	6.0			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	6.0			2		20		40	μA

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HCT11		GD54HCT11		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		4.5 to 5.5	2.0			2.0		2.0		V
V _{IL}	LOW level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH}	I _{OH} =−20μA	4.5	4.4	4.5	4.4		4.4		V
		or V _{IL}	I _{OH} =−4mA	4.5	3.98	4.3	3.84		3.7		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH}	I _{OL} =20μA	4.5		0.1		0.1		0.1	V
		or V _{IL}	I _{OL} =4mA	4.5		0.17	0.26	0.33		0.4	
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	5.5			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	5.5			2		20		40	μA

AC Characteristics for HC: $t_r=t_f=6\text{ns}$ $C_L=50\text{pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HC11		GD54HC11		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
$t_{PLH}/$ t_{PHL}	Propagation delay time nA, nB, nC to nY	2.0 4.5 6.0		30 11 9	98 19 16		120 24 20		150 29 25	ns
$t_{TLH}/$ t_{THL}	Output transition time	2.0 4.5 6.0		19 7 6	75 15 13		95 19 16		110 22 19	ns

AC Characteristics for HCT: $t_r=t_f=6\text{ns}$ $C_L=50\text{pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HCT11		GD54HCT11		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
$t_{PLH}/$ t_{PHL}	Propagation delay time nA, nB, nC to nY	4.5		16	28		35		42	ns
$t_{TLH}/$ t_{THL}	Output transition time	4.5		7	15		19		22	ns

AC Waveform

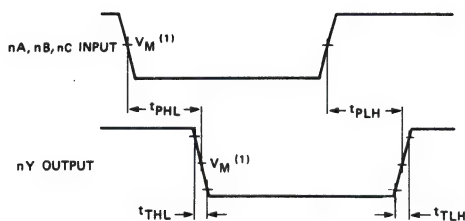


Fig. 3 Waveforms showing the input (nA, nB, nC) to output (nY) propagation delays and the output transition times.

Note to AC waveform

(1) HC : $V_M=50\%$. $V_I=GND$ to V_{CC}

HCT: $V_M=1.3V$. $V_I=GND$ to $3V$.

GD54/74HC14, GD54/74HCT14

HEX SCHMITT-TRIGGER INVERTERS

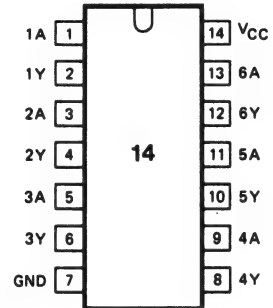
General Description

These devices are identical in pinout to the 54/74LS14. They contain six independent schmitt-trigger inverters. Each circuit functions as an inverter, but because of the schmitt-trigger action, it has different input threshold levels for positive (V_{T+}) and for negative (V_{T-}) going signals. These devices are characterized for operation over wide temperature ranges to meet industry and military specifications.

Features

- Low Power consumption characteristic of CMOS devices
- Output drive capability: 10 LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts
for HCT 4.5 to 5.5 volts
- Low input current: $1\mu\text{A}$ Max.
- Low quiescent current: $20\mu\text{A}$ Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs

Pin Configuration



Suffix-Blank : Plastic Dual In Line Package
 Suffix-J : Ceramic Dual In Line Package
 Suffix-D : Small Outline Package

Logic Symbol and Schematic Diagram

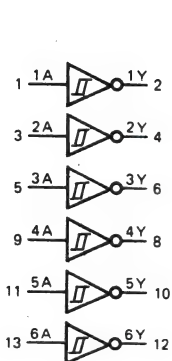


Fig. 1 Logic symbol

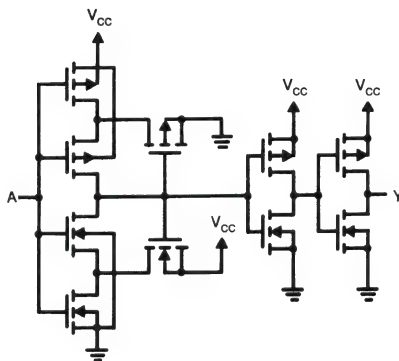


Fig. 2 Schematic diagram

Function Table

INPUT	OUTPUT
nA	nY
L	H
H	L

H=HIGH Voltage level
 L=LOW Voltage level

Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC Supply voltage		-0.5	+7	V
I_{IK}, I_{OK}	DC input or output diode current	for $V_I < -0.5$ or $V_I > V_{CC} + 0.5V$		20	mA
I_O	DC output source or sink current	for $-0.5V < V_O < V_{CC} + 0.5V$		25	mA
I_{CC}	DC V_{CC} or GND current			50	mA
T_{stg}	Storage temperature range		-65	150	°C
P_D	Power dissipation per package	above +70°C: derate linearly with 8mW/K		500	mW
T_L	Lead temperature	At distance 1/16 ± 1/32 in. from case for 60 sec(CERAMIC) 10 sec(PLASTIC)		300 260	°C

Recommended Operating Conditions

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range V_{CC} : GD54/74HC Types	2	6	V
GD54/74HCT Types	4.5	5.5	
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A : GD74 Types	-40	+85	°C
GD54 Types	-55	+125	
Input Rise and Fall times t_r, t_f : GD54/74HC Types at 2V		1000	ns
at 4.5V		500	
at 6V		400	
GD54/74HCT Types at 4.5 V		500	

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HC14		GD54HC14		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2		1.5 3.15 4.2		V
V _{IL}	LOW level input voltage		2.0 4.5 6.0			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH}	I _{OH} =-20μA	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0	1.9 4.4 5.9		1.9 4.4 5.9		V
			I _{OH} =-4mA	4.5 6.0	3.98 5.48	4.3 5.2	3.84 5.34		3.7 5.2		
		or V _{IL}	I _{OH} =-5.2mA	4.5 6.0	3.98 5.48	4.3 5.2	3.84 5.34		3.7 5.2		
			I _{OH} =-5.2mA	4.5 6.0	3.98 5.48	4.3 5.2	3.84 5.34		3.7 5.2		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH}	I _{OL} =20μA	2.0 4.5 6.0			0.1 0.1 0.1		0.1 0.1 0.1		V
			I _{OL} =4mA	4.5 6.0		0.17 0.15	0.26 0.26		0.33 0.33		
		or V _{IL}	I _{OL} =4mA	4.5 6.0		0.17 0.15	0.26 0.26		0.33 0.33		
			I _{OL} =5.2mA	4.5 6.0		0.17 0.15	0.26 0.26		0.33 0.33		
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	6.0			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	6.0			2		20		40	μA

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HCT14		GD54HCT14		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		4.5 to 5.5	2.0			2.0		2.0		V
V _{IL}	LOW level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH}	I _{OH} =-20μA	4.5	4.4	4.5	4.4		4.4		V
		or V _{IL}	I _{OH} =-4mA	4.5	3.98	4.3	3.84		3.7		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH}	I _{OL} =20μA	4.5		0.1		0.1		0.1	V
		or V _{IL}	I _{OL} =4mA	4.5		0.17	0.26	0.33		0.4	
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	5.5			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	5.5			2		20		40	μA

Transfer Characteristic for HC

SYMBOL	PARAMETER	TEST CONDITION	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HC14		GD54HC14		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V_{T+}	Positive-going threshold		2.0	0.7	1.2	1.5	0.7	1.5	0.7	1.5	V
			4.5	1.7	2.4	3.15	1.7	3.15	1.7	3.15	
			6.0	2.1	3.2	4.2	2.1	4.2	2.1	4.2	
V_{T-}	Negative-going threshold		2.0	0.3	0.65	1.0	0.3	1.0	0.3	1.0	V
			4.5	0.9	1.7	2.2	0.9	2.2	0.9	2.2	
			6.0	1.2	2.1	3.0	1.2	3.0	1.2	3.0	
V_H	Hysteresis($V_{T+} - V_{T-}$)		2.0	0.2	0.5	1.0	0.2	1.0	0.2	1.0	V
			4.5	0.4	0.9	1.4	0.4	1.4	0.4	1.4	
			6.0	0.5	1.3	1.7	0.5	1.7	0.5	1.7	

Transfer Characteristic for HCT

SYMBOL	PARAMETER	TEST CONDITION	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HCT14		GD54HCT14		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V_{T+}	Positive-going threshold		4.5	1.2	1.55	1.9	1.2	1.9	1.2	1.9	V
			5.5	1.4	1.75	2.1	1.4	2.1	1.4	2.1	
V_{T-}	Negative-going threshold		4.5	0.5	0.85	1.2	0.5	1.2	0.5	1.2	V
			5.5	0.6	1.0	1.4	0.6	1.4	0.6	1.4	
V_H	Hysteresis($V_{T+} - V_{T-}$)		4.5	0.4	0.9	1.4	0.4	1.4	0.4	1.4	V
			5.5	0.5	1.0	1.5	0.5	1.5	0.5	1.5	

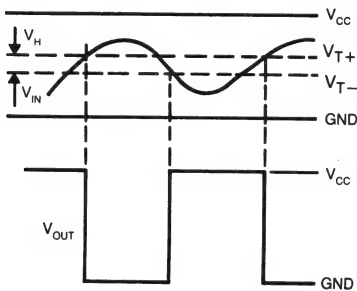
AC Characteristics for HC: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HC14		GD54HC14		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
$t_{PLH}/$ t_{PHL}	Propagation delay time nA to nY	2.0		36	120		150		180	ns
		4.5		11	24		30		36	
		6.0		9	20		24		30	
$t_{TLH}/$ t_{THL}	Output transition time	2.0		19	75		95		110	ns
		4.5		7	15		19		22	
		6.0		6	13		15		19	

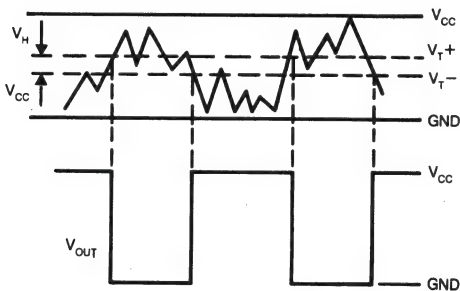
AC Characteristics for HCT: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HCT14		GD54HCT14		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
$t_{PLH}/$ t_{PHL}	Propagation delay time nA to nY	4.5		15	25		31		38	ns
$t_{TLH}/$ t_{THL}	Output transition time	4.5		7	15		19		22	ns

Typical Applications



(a) A Schmitt trigger squares up inputs with slow rise and fall times.



(b) A Schmitt trigger offers offers maximum noise immunity.

Fig. 3 Typical applications

Transfer characteristic waveforms

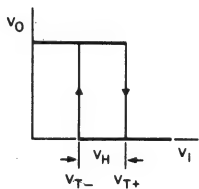


Fig. 4 Transfer characteristic

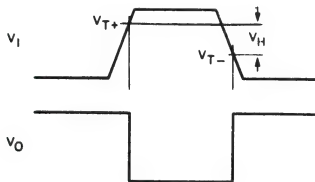


Fig. 5 Wave forms showing the definition of V_{T+} , V_{T-} and V_H ; where V_{T+} and V_{T-} are between limits of 20% and 70%.

AC Waveform

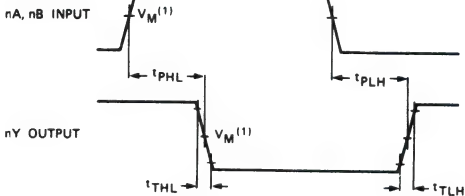


Fig. 6 Waveforms showing the input (nA, nB) to output (nY) propagation delays and the output transition times.

Note to AC waveform

(1) HC : $V_M=50\%$, $V_L=GND$ to V_{CC}
HCT: $V_M=1.3V$; $V_L=GND$ to $3V$.

GD54/74HC20, GD54/74HCT20

DUAL 4-INPUT NAND GATES

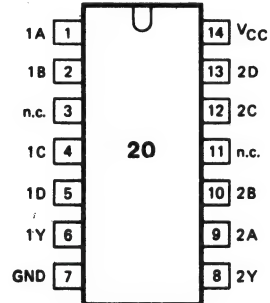
General Description

These devices are identical in pinout to the 54/74LS20. They contain two independent 4-input NAND gates. These devices are characterized for operation over wide temperature ranges to meet industry and military specifications.

Features

- Low Power consumption characteristic of CMOS devices
- Output drive capability: 10 LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts
for HCT 4.5 to 5.5 volts
- Low input current: $1\mu\text{A}$ Max.
- Low quiescent current: $20\mu\text{A}$ Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs

Pin Configuration



Suffix-Blank : Plastic Dual In Line Package
 Suffix-J : Ceramic Dual In Line Package
 Suffix-D : Small Outline Package

Function Table

INPUT				OUTPUT
nA	nB	nC	nD	nY
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H
H	H	H	H	L

H=HIGH Voltage level

L=LOW Voltage level

X=don't care

Logic Symbol and Diagram

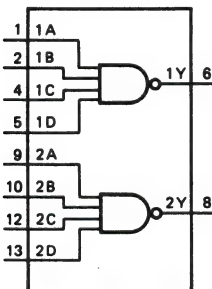


Fig. 1 Logic symbol

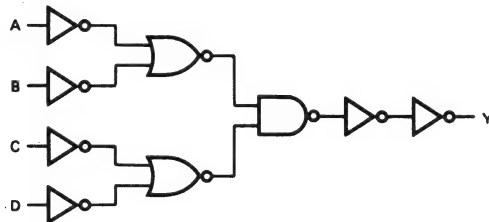


Fig. 2 Logic diagram (one gate)

Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC Supply voltage		-0.5	+7	V
I_{IK}, I_{OK}	DC input or output diode current	for $V_I < -0.5$ or $V_I > V_{CC} + 0.5V$		20	mA
I_O	DC output source or sink current	for $-0.5V < V_O < V_{CC} + 0.5V$		25	mA
I_{CC}	DC V_{CC} or GND current			50	mA
T_{stg}	Storage temperature range		-65	150	°C
P_D	Power dissipation per package	above +70°C: derate linearly with 8mW/K		500	mW
T_L	Lead temperature	At distance $1/16 \pm 1/32$ in. from case for 60 sec(CERAMIC) 10 sec(PLASTIC)		300 260	°C

Recommended Operating Conditions

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range V_{CC} : GD54/74HC Types GD54/74HCT Types	2 4.5	6 5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A : GD74 Types GD54 Types	-40 -55	+85 +125	°C
Input Rise and Fall times t_r, t_f : GD54/74HC Types at 2V at 4.5V at 6V GD54/74HCT Types at 4.5V		1000 500 400 500	ns

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HC20		GD54HC20		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2		1.5 3.15 4.2		V
V _{IL}	LOW level input voltage		2.0 4.5 6.0			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH}	I _{OH} =-20μA	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0	1.9 4.4 5.9		1.9 4.4 5.9		V
		or V _{IL}	I _{OH} =-4mA I _{OH} =-5.2mA	4.5 6.0	3.98 5.48	4.3 5.2	3.84 5.34		3.7 5.2		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH}	I _{OL} =20μA	2.0 4.5 6.0			0.1 0.1 0.1	0.1 0.1 0.1		0.1 0.1 0.1	V
		or V _{IL}	I _{OL} =4mA I _{OL} =5.2mA	4.5 6.0		0.17 0.15	0.26 0.26	0.33 0.33		0.4 0.4	
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	6.0			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	6.0			2		20		40	μA

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HCT20		GD54HCT20		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		4.5 to 5.5	2.0			2.0		2.0		V
V _{IL}	LOW level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH}	I _{OH} =-20μA	4.5	4.4	4.5	4.4		4.4		V
		or V _{IL}	I _{OH} =-4mA	4.5	3.98	4.3	3.84		3.7		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH}	I _{OL} =20μA	4.5			0.1	0.1		0.1	V
		or V _{IL}	I _{OL} =4mA	4.5		0.17	0.26	0.33		0.4	
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	5.5			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	5.5			2		20		40	μA

AC Characteristics for HC: $t_r=t_f=6\text{ns}$ $C_L=50\text{pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HC20		GD54HC20		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
$t_{PLH}/$ t_{PHL}	Propagation delay time nA, nB, nC, nD to nY	2.0 4.5 6.0		28 10 8	90 18 15		110 23 20		130 26 23	ns
$t_{TLH}/$ t_{THL}	Output transition time	2.0 4.5 6.0		25 8 7	70 15 13		85 18 16		100 22 19	ns

AC Characteristics for HCT: $t_r=t_f=6\text{ns}$ $C_L=50\text{pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HCT20		GD54HCT20		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
$t_{PLH}/$ t_{PHL}	Propagation delay time nA, nB, nC, nD to nY	4.5		14	24		30		40	ns
$t_{TLH}/$ t_{THL}	Output transition time	4.5		8	15		18		22	ns

AC Waveform

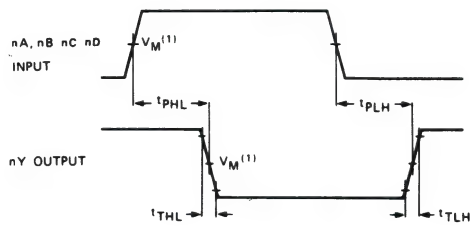


Fig. 3 Waveforms showing the input (nA, nB, nC, nD) to output (nY) propagation delays and the output transition times.

Note to AC waveform

(1) HC : $V_M=50\%$, $V_L=GND$ to V_{CC}
HCT: $V_M=1.3V$, $V_L=GND$ to $3V$.

GD54/74HC21, GD54/74HCT21

DUAL 4-INPUT AND GATES

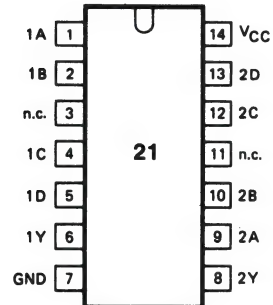
General Description

These devices are identical in pinout to the 54/74LS21. They contain two independent 4-input AND gates. These devices are characterized for operation over wide temperature ranges to meet industry and military specifications.

Features

- Low Power consumption characteristic of CMOS devices
- Output drive capability: 10 LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts
for HCT 4.5 to 5.5 volts
- Low input current: $1\mu\text{A}$ Max.
- Low quiescent current: $20\mu\text{A}$ Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs

Pin Configuration



Suffix-Blank : Plastic Dual In Line Package
 Suffix-J : Ceramic Dual In Line Package
 Suffix-D : Small Outline Package

Function Table

INPUT				OUTPUT
nA	nB	nC	nD	nY
L	X	X	X	L
X	L	X	X	L
X	X	L	X	L
X	X	X	L	L
H	H	H	H	H

H=HIGH Voltage level
 L=LOW Voltage level
 X=don't care

Logic Symbol and Diagram

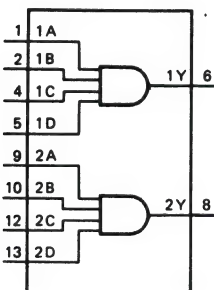


Fig. 1 Logic symbol

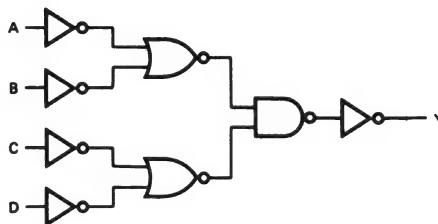


Fig. 2 Logic diagram (one gate)

Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC Supply voltage		-0.5	+7	V
I_{IK}, I_{OK}	DC input or output diode current	for $V_I < -0.5$ or $V_I > V_{CC} + 0.5V$		20	mA
I_O	DC output source or sink current	for $-0.5V < V_O < V_{CC} + 0.5V$		25	mA
I_{CC}	DC V_{CC} or GND current			50	mA
T_{stg}	Storage temperature range		-65	150	°C
P_D	Power dissipation per package	above +70°C: derate linearly with 8mW/K		500	mW
T_L	Lead temperature	At distance $1/16 \pm 1/32$ in. from case for 60 sec(CERAMIC) 10 sec(PLASTIC)		300 260	°C

Recommended Operating Conditions

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range V_{CC} : GD54/74HC Types GD54/74HCT Types	2 4.5	6 5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A : GD74 Types GD54 Types	-40 -55	+85 +125	°C
Input Rise and Fall times t_r, t_f : GD54/74HC Types at 2V at 4.5V at 6V GD54/74HCT Types at 4.5V		1000 500 400 500	ns

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION	V_{CC} (V)	$T_A=25^{\circ}\text{C}$			GD74HC21		GD54HC21		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V_{IH}	HIGH level input Voltage		2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2		1.5 3.15 4.2		V
V_{IL}	LOW level input voltage		2.0 4.5 6.0			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V
V_{OH}	HIGH level output voltage	$V_{IN}=V_{IH}$	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V
		or V_{IL}									
V_{OL}	LOW level output voltage	$V_{IN}=V_{IH}$	2.0 4.5 6.0			0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V
		or V_{IL}									
$ I_{IN} $	Input leakage Current	$V_{IN}=V_{CC}$ or GND	6.0			0.1		1.0		1.0	μA
I_{CC}	Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{out}=0\mu\text{A}$	6.0			2		20		40	μA

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION	V_{CC} (V)	$T_A=25^{\circ}\text{C}$			GD74HCT21		GD54HCT21		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V_{IH}	HIGH level input Voltage		4.5 to 5.5	2.0			2.0		2.0		V
V_{IL}	LOW level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V_{OH}	HIGH level output voltage	$V_{IN}=V_{IH}$	4.5	4.4	4.5		4.4		4.4		V
		or V_{IL}	4.5	3.98	4.3		3.84		3.7		
V_{OL}	LOW level output voltage	$V_{IN}=V_{IH}$	4.5			0.1		0.1		0.1	V
		or V_{IL}	4.5		0.17	0.26		0.33		0.4	
$ I_{IN} $	Input leakage Current	$V_{IN}=V_{CC}$ or GND	5.5			0.1		1.0		1.0	μA
I_{CC}	Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{out}=0\mu\text{A}$	5.5			2		20		40	μA

AC Characteristics for HC: $t_r=t_f=6\text{ns}$ $C_L=50\text{pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HC21		GD54HC21		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
$t_{PLH}/$ t_{PHL}	Propagation delay time nA, nB, nC, nD to nY	2.0 4.5 6.0		28 10 8	90 18 15		110 23 20		130 26 23	ns
$t_{TLH}/$ t_{THL}	Output transition time	2.0 4.5 6.0		25 8 7	70 15 13		85 18 16		100 22 19	ns

AC Characteristics for HCT: $t_r=t_f=6\text{ns}$ $C_L=50\text{pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HCT21		GD54HCT21		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
$t_{PLH}/$ t_{PHL}	Propagation delay time nA, nB, nC, nD to nY	4.5		15	25		30		40	ns
$t_{TLH}/$ t_{THL}	Output transition time	4.5		8	15		18		22	ns

AC Waveform

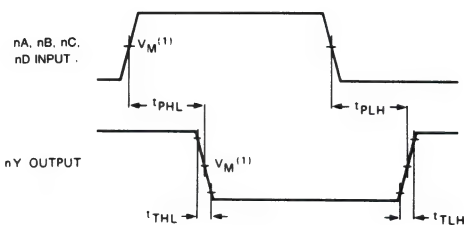


Fig. 3 Waveforms showing the input (nA, nB, nC, nD) to output (nY) propagation delays and the output transition times.

Note to AC waveform

- (1) HC : $V_M=50\%$, $V_I=GND$ to V_{CC}
HCT: $V_M=1.3V$, $V_I=GND$ to $3V$

GD54/74HC27, GD54/74HCT27

TRIPLE 3-INPUT NOR GATES

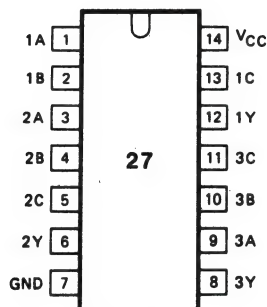
General Description

These devices are identical in pinout to the 54/74LS27. They contain three independent 3-input NOR gates. These devices are characterized for operation over wide temperature ranges to meet industry and military specifications.

Features

- Low Power consumption characteristic of CMOS devices
- Output drive capability: 10 LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts
for HCT 4.5 to 5.5 volts
- Low input current: $1\mu\text{A}$ Max.
- Low quiescent current: $20\mu\text{A}$ Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs

Pin Configuration



Suffix-Blank : Plastic Dual In Line Package
 Suffix-J : Ceramic Dual In Line Package
 Suffix-D : Small Outline Package

Logic Symbol and Diagram

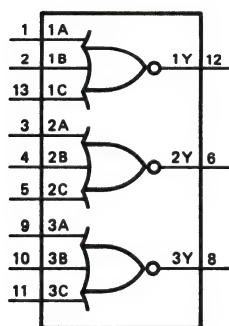
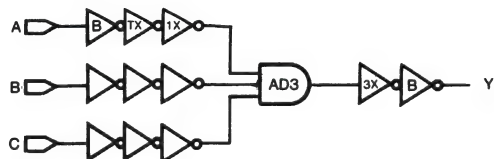


Fig. 1 Logic symbol

Function Table



INPUT			OUTPUT
nA	nB	nC	nY
L	L	L	H
X	X	H	L
X	H	X	L
H	X	X	L

H=HIGH Voltage level
 L=LOW Voltage level
 X=don't care

Fig. 2 Logic diagram (one gate)

Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC Supply voltage		-0.5	+7	V
I_{IK}, I_{OK}	DC input or output diode current	for $V_I < -0.5$ or $V_I > V_{CC} + 0.5V$		20	mA
I_O	DC output source or sink current	for $-0.5V < V_O < V_{CC} + 0.5V$		25	mA
I_{CC}	DC V_{CC} or GND current			50	mA
T_{stg}	Storage temperature range		-65	150	°C
P_D	Power dissipation per package	above +70°C: derate linearly with 8mW/K		500	mW
T_L	Lead temperature	At distance 1/16 ± 1/32 in. from case for 60 sec(CERAMIC) 10 sec(PLASTIC)		300 260	°C

Recommended Operating Conditions

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range V_{CC} : GD54/74HC Types GD54/74HCT Types	2 4.5	6 5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A : GD74 Types GD54 Types	-40 -55	+85 +125	°C
Input Rise and Fall times t_r, t_f : GD54/74HC Types at 2V at 4.5V at 6V GD54/74HCT Types at 4.5V		1000 500 400 500	ns

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A = 25 °C			GD74HC27		GD54HC27		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2		1.5 3.15 4.2		V
V _{IL}	LOW level input voltage		2.0 4.5 6.0			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V
V _{OH}	HIGH level output voltage	V _{IN} = V _{IH}	I _{OH} = -20μA	2.0	1.9	2.0			1.9		V
				4.5	4.4	4.5			4.4		
		or V _{IL}	I _{OH} = -4mA I _{OH} = -5.2mA	6.0	5.9	6.0			5.9		
				4.5	3.98	4.3			3.7		
V _{OL}	LOW level output voltage	V _{IN} = V _{IH}	I _{OL} = 20μA	2.0			0.1		0.1		V
				4.5			0.1		0.1		
		or V _{IL}	I _{OL} = 4mA I _{OL} = 5.2mA	6.0			0.1		0.1		
				4.5	0.17	0.26		0.33		0.4	
I _{IN}	Input leakage Current	V _{IN} = V _{CC} or GND	6.0			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} = V _{CC} or GND I _{out} = 0μA	6.0			2		20		40	μA

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A = 25 °C			GD74HCT27		GD54HCT27		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		4.5 to 5.5	2.0			2.0		2.0		V
V _{IL}	LOW level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V _{OH}	HIGH level output voltage	V _{IN} = V _{IH}	I _{OH} = -20μA	4.5	4.4	4.5			4.4		V
				4.5	3.98	4.3			3.7		
		or V _{IL}	I _{OH} = -4mA	4.5			3.84				
				4.5							
V _{OL}	LOW level output voltage	V _{IN} = V _{IH}	I _{OL} = 20μA	4.5			0.1		0.1		V
				4.5			0.1		0.1		
		or V _{IL}	I _{OL} = 4mA	4.5		0.17	0.26		0.33		
				4.5						0.4	
I _{IN}	Input leakage Current	V _{IN} = V _{CC} or GND	5.5			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} = V _{CC} or GND I _{out} = 0μA	5.5			2		20		40	μA

AC Characteristics for HC: $t_r=t_f=6\text{ns}$ $C_L=50\text{pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HC27		GD54HC27		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
$t_{PLH}/$ t_{PHL}	Propagation delay time nA, nB, nC to nY	2.0 4.5 6.0		28 10 8	90 18 15		115 23 20		135 25 23	ns
$t_{TLH}/$ t_{THL}	Output transition time	2.0 4.5 6.0		19 7 6	75 15 13		95 19 16		110 22 19	ns

AC Characteristics for HCT: $t_r=t_f=6\text{ns}$ $C_L=50\text{pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HCT27		GD54HCT27		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
$t_{PLH}/$ t_{PHL}	Propagation delay time nA, nB, nC to nY	4.5		12	21		26		32	ns
$t_{TLH}/$ t_{THL}	Output transition time	4.5		7	15		19		22	ns

AC Waveform

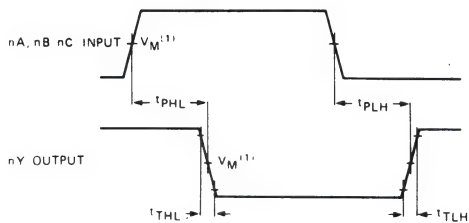


Fig. 3 Waveforms showing the input (nA, nB, nC) to output (nY) propagation delays and the output transition times.

Note to AC waveform

- (1) HC : $V_M=50\%$; $V_I=GND$ to V_{CC}
HCT: $V_M=1.3V$; $V_I=GND$ to $3V$.

GD54/74HC30, GD54/74HCT30

8-INPUT NAND GATE

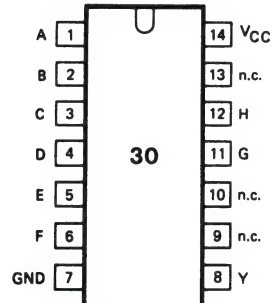
General Description

These devices are identical in pinout to the 54/74LS30. They contain a single 8-input NAND gate. These devices are characterized for operation over wide temperature ranges to meet industry and military specifications.

Features

- Low Power consumption characteristic of CMOS devices
- Output drive capability: 10 LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts
for HCT 4.5 to 5.5 volts
- Low input current: 1 μ A Max.
- Low quiescent current: 20 μ A Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs

Pin Configuration



Suffix-Blank : Plastic Dual In Line Package
 Suffix-J : Ceramic Dual In Line Package
 Suffix-D : Small Outline Package

Logic Symbol and Diagram

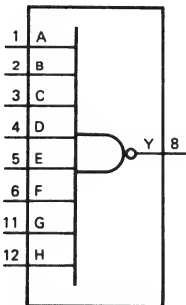


Fig. 1 Logic symbol

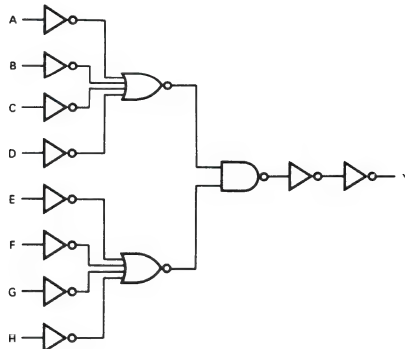


Fig. 2 Logic diagram

Function Table

INPUTS								OUTPUT
A	B	C	D	E	F	G	H	Y
L	X	X	X	X	X	X	X	H
X	L	X	X	X	X	X	X	H
X	X	L	X	X	X	X	X	H
X	X	X	L	X	X	X	X	H
X	X	X	X	L	X	X	X	H
X	X	X	X	X	L	X	X	H
X	X	X	X	X	X	L	X	H
X	X	X	X	X	X	X	L	H
H	H	H	H	H	H	H	H	L

H=HIGH voltage level
 L=LOW voltage level
 X=don't care

Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC Supply voltage		-0.5	+7	V
I_{IK}, I_{OK}	DC input or output diode current	for $V_I < -0.5$ or $V_I > V_{CC} + 0.5V$		20	mA
I_O	DC output source or sink current	for $-0.5V < V_O < V_{CC} + 0.5V$		25	mA
I_{CC}	DC V_{CC} or GND current			50	mA
T_{stg}	Storage temperature range		-65	150	°C
P_D	Power dissipation per package	above +70°C: derate linearly with 8mW/K		500	mW
T_L	Lead temperature	At distance 1/16 ± 1/32 in. from case for 60 sec(CERAMIC) 10 sec(PLASTIC)		300 260	°C

Recommended Operating Conditions

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range V_{CC} : GD54/74HC Types GD54/74HCT Types	2 4.5	6 5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A : GD74 Types GD54 Types	-40 -55	+85 +125	°C
Input Rise and Fall times t_r, t_f : GD54/74HC Types at 2V at 4.5V at 6V GD54/74HCT Types at 4.5V		1000 500 400 500	ns

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HC30		GD54HC30		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2		1.5 3.15 4.2		V
V _{IL}	LOW level input voltage		2.0 4.5 6.0			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH}	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V
		or V _{IL}									
			I _{OH} =-20μA I _{OH} =-4mA I _{OH} =-5.2mA								
V _{OL}	LOW level output voltage	V _{IN} =V _{IH}	2.0 4.5 6.0			0.1 0.1 0.1	0.1 0.1 0.1		0.1 0.1 0.1		V
		or V _{IL}									
			I _{OL} =20μA I _{OL} =4mA I _{OL} =5.2mA		0.17 0.15	0.26 0.26	0.33 0.33		0.4 0.4		
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	6.0			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	6.0			2		20		40	μA

DC Electrical Characteristics for HCT

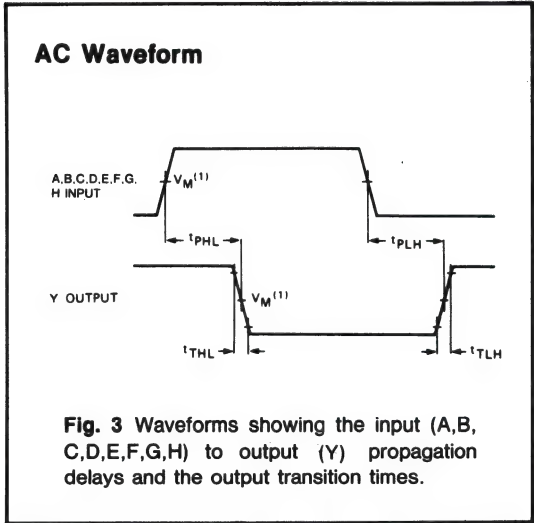
SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HCT30		GD54HCT30		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		4.5 to 5.5	2.0			2.0		2.0		V
V _{IL}	LOW level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH}	4.5	4.4	4.5		4.4		4.4		V
		or V _{IL}	I _{OH} =-20μA I _{OH} =-4mA	4.5	3.98	4.3	3.84		3.7		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH}	4.5			0.1	0.1		0.1		V
		or V _{IL}	I _{OL} =20μA I _{OL} =4mA	4.5	0.17	0.26	0.33		0.4		
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	5.5			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	5.5			2		20		40	μA

AC Characteristics for HC: $t_r=t_f=6\text{ns}$ $C_L=50\text{pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HC30		GD54HC30		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
$t_{PLH}/$ t_{PHL}	Propagation delay time A, B, C, D, E, F, G, H to Y	2.0 4.5 6.0		35 12 10	110 24 20		150 30 26		180 36 32	ns
$t_{TLH}/$ t_{THL}	Output transition time	2.0 4.5 6.0		25 8 7	70 15 13		85 18 16		100 22 19	ns

AC Characteristics for HCT: $t_r=t_f=6\text{ns}$ $C_L=50\text{pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HCT30		GD54HCT30		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
$t_{PLH}/$ t_{PHL}	Propagation delay time A, B, C, D, E, F, G, H to Y	4.5		15	28		36		42	ns
$t_{TLH}/$ t_{THL}	Output transition time	4.5		8	15		19		22	ns



Note to AC waveform

- (1) HC : $V_M=50\%$, $V_L=GND$ to V_{CC}
HCT: $V_M=1.3V$, $V_L=GND$ to $3V$.

GD54/74HC32, GD54/74HCT32

QUAD 2-INPUT OR GATES

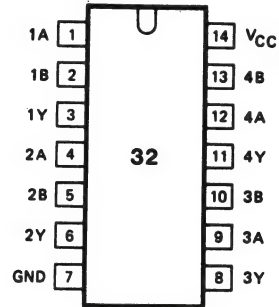
General Description

These devices are identical in pinout to the 54/74LS32. They contain four independent 2-input OR gates. These devices are characterized for operation over wide temperature ranges to meet industry and military specifications.

Features

- Low Power consumption characteristic of CMOS devices
- Output drive capability: 10 LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts for HCT 4.5 to 5.5 volts
- Low input current: $1\mu\text{A}$ Max.
- Low quiescent current: $20\mu\text{A}$ Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs

Pin Configuration



Suffix-Blank : Plastic Dual In Line Package
 Suffix-J : Ceramic Dual In Line Package
 Suffix-D : Small Outline Package

Logic Symbol and Diagram

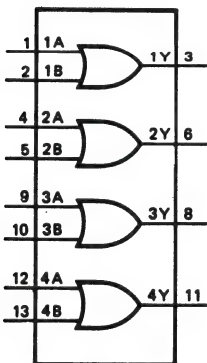


Fig. 1 Logic symbol

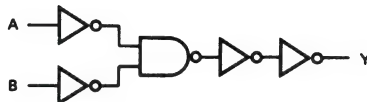


Fig. 2 Logic diagram (one gate)

Function Table

INPUTS		OUTPUT
nA	nB	nY
L	L	L
L	H	H
H	L	H
H	H	H

H=HIGH voltage level
 L=LOW voltage level

Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC Supply voltage		-0.5	+7	V
I_{IK}, I_{OK}	DC input or output diode current	for $V_I < -0.5$ or $V_I > V_{CC} + 0.5V$		20	mA
I_O	DC output source or sink current	for $-0.5V < V_O < V_{CC} + 0.5V$		25	mA
I_{CC}	DC V_{CC} or GND current			50	mA
T_{stg}	Storage temperature range		-65	150	°C
P_D	Power dissipation per package	above +70°C: derate linearly with 8mW/K		500	mW
T_L	Lead temperature	At distance 1/16 ± 1/32 in. from case for 60 sec(CERAMIC) 10 sec(PLASTIC)		300 260	°C

Recommended Operating Conditions

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range V_{CC} : GD54/74HC Types GD54/74HCT Types	2 4.5	6 5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A : GD74 Types GD54 Types	-40 -55	+85 +125	°C
Input Rise and Fall times t_r, t_f : GD54/74HC Types at 2V at 4.5V at 6V GD54/74HCT Types at 4.5V		1000 500 400 500	ns

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A = 25°C			GD74HC32		GD54HC32		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2		1.5 3.15 4.2		V
V _{IL}	LOW level input voltage		2.0 4.5 6.0			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V
V _{OH}	HIGH level output voltage	V _{IN} = V _{IH}	I _{OH} = -20μA	2.0	1.9	2.0		1.9		1.9	V
				4.5	4.4	4.5		4.4		4.4	
		or V _{IL}	I _{OH} = -4mA I _{OH} = -5.2mA	6.0	5.9	6.0		5.9		5.9	
				4.5	3.98	4.3		3.84		3.7	
V _{OL}	LOW level output voltage	V _{IN} = V _{IH}	I _{OL} = 20μA	2.0			0.1		0.1		V
				4.5			0.1		0.1		
		or V _{IL}	I _{OL} = 4mA I _{OL} = 5.2mA	6.0			0.1		0.1		
				4.5		0.17	0.26		0.33		
I _{IN}	Input leakage Current	V _{IN} = V _{CC} or GND	6.0			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} = V _{CC} or GND I _{out} = 0μA	6.0			2		20		40	μA

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A = 25°C			GD74HCT32		GD54HCT32		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		4.5 to 5.5	2.0			2.0		2.0		V
V _{IL}	LOW level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V _{OH}	HIGH level output voltage	V _{IN} = V _{IH}	I _{OH} = -20μA	4.5	4.4	4.5		4.4		4.4	V
		or V _{IL}	I _{OH} = -4mA	4.5	3.98	4.3		3.84		3.7	
V _{OL}	LOW level output voltage	V _{IN} = V _{IH}	I _{OL} = 20μA	4.5			0.1		0.1		V
		or V _{IL}	I _{OL} = 4mA	4.5		0.17	0.26		0.33		
I _{IN}	Input leakage Current	V _{IN} = V _{CC} or GND	5.5			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} = V _{CC} or GND I _{out} = 0μA	5.5			2		20		40	μA

AC Characteristics for HC: $t_r = t_f = 6\text{ns}$ $C_L = 50\text{pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A = 25^\circ\text{C}$			GD74HC32		GD54HC32		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
$t_{PLH}/$ t_{PHL}	Propagation delay time nA, nB to nY	2.0 4.5 6.0		22 8 6	90 18 15		115 23 20		135 27 23	ns
$t_{TLH}/$ t_{THL}	Output transition time	2.0 4.5 6.0		19 7 6	75 15 13		95 19 16		110 22 19	ns

AC Characteristics for HCT: $t_r = t_f = 6\text{ns}$ $C_L = 50\text{pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A = 25^\circ\text{C}$			GD74HCT32		GD74HCT32		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
$t_{PLH}/$ t_{PHL}	Propagation delay time nA, nB, to nY	4.5		13	24		30		36	ns
$t_{TLH}/$ t_{THL}	Output transition time	4.5		7	15		19		22	ns

AC Waveform

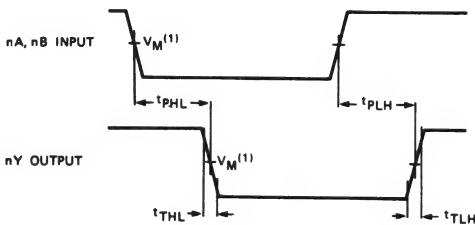


Fig. 3 Waveforms showing the input (nA, nB) to output (nY) propagation delays and the output transition times.

Note to AC waveform

(1) HC : $V_M = 50\%$, $V_I = \text{GND to } V_{CC}$
HCT: $V_M = 1.3\text{V}$, $V_I = \text{GND to } 3\text{V}$.

GD54/74HC34, GD54/74HCT34

HEX BUFFERS

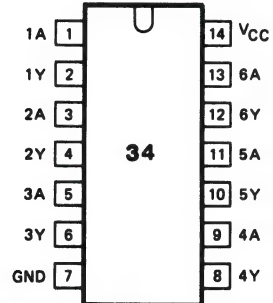
General Description

These devices are identical in pinout to the 54/74LS34. They contain six independent noninverting buffers. Especially, the HCT 34 can be used for interfacing between TTL and NMOS components and standard CMOS devices. These devices are characterized for operation over wide temperature ranges to meet industry and military specifications.

Features

- Low Power consumption characteristic of CMOS devices
- Output drive capability: 10 LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts
for HCT 4.5 to 5.5 volts
- Low input current: 1 μ A Max.
- Low quiescent current: 20 μ A Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs

Pin Configuration



Suffix-Blank : Plastic Dual In Line Package
 Suffix-J : Ceramic Dual In Line Package
 Suffix-D : Small Outline Package

Logic Diagram

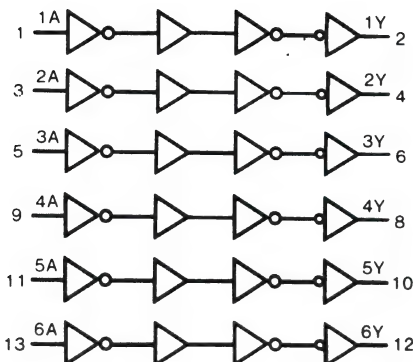


Fig. 1 Logic Diagram

Function Table

INPUT	OUTPUT
nA	nY
H	H
L	L

H= HIGH voltage level
 L= LOW voltage level

Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC Supply voltage		-0.5	+7	V
I_{IK}, I_{OK}	DC input or output diode current	for $V_I < -0.5$ or $V_I > V_{CC} + 0.5V$		20	mA
I_O	DC output source or sink current	for $-0.5V < V_O < V_{CC} + 0.5V$		25	mA
I_{CC}	DC V_{CC} or GND current			50	mA
T_{stg}	Storage temperature range		-65	150	°C
P_D	Power dissipation per package	above +70°C: derate linearly with 8mW/K		500	mW
T_L	Lead temperature	At distance 1/16 ± 1/32 in. from case for 60 sec(CERAMIC) 10 sec(PLASTIC)		300 260	°C

Recommended Operating Conditions

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range V_{CC} : GD54/74HC Types GD54/74HCT Types	2 4.5	6 5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A : GD74 Types GD54 Types	-40 -55	+85 +125	°C
Input Rise and Fall times t_r, t_f : GD54/74HC Types at 2V at 4.5V at 6V GD54/74HCT Types at 4.5 V		1000 500 400 500	ns

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HC34		GD54HC34		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2		1.5 3.15 4.2		V
V _{IL}	LOW level input voltage		2.0 4.5 6.0			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH}	I _{OH} =-20μA	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0	1.9 4.4 5.9		1.9 4.4 5.9		V
		or V _{IL}	I _{OH} =-4mA I _{OH} =-5.2mA	4.5 6.0	3.98 5.48	4.3 5.2	3.84 5.34		3.7 5.2		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH}	I _{OL} =20μA	2.0 4.5 6.0			0.1 0.1 0.1	0.1 0.1 0.1		0.1 0.1 0.1	V
		or V _{IL}	I _{OL} =4mA I _{OL} =5.2mA	4.5 6.0		0.17 0.15	0.26 0.26	0.33 0.33		0.4 0.4	
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	6.0			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	6.0			2		20		40	μA

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HCT34		GD54HCT34		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		4.5 to 5.5	2.0			2.0		2.0		V
V _{IL}	LOW level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH}	I _{OH} =-20μA	4.5	4.4	4.5	4.4		4.4		V
		or V _{IL}	I _{OH} =-4mA	4.5	3.98	4.3	3.84		3.7		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH}	I _{OL} =20μA	4.5		0.1		0.1		0.1	V
		or V _{IL}	I _{OL} =4mA	4.5		0.17	0.26	0.33		0.4	
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	5.5			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	5.5			2		20		40	μA

AC Characteristics for HC: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HC34		GD54HC34		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
$t_{PLH}/$ t_{PHL}	Propagation Delay Time nA to nY	2.0 4.5 6.0		25 8 7	80 16 14		105 21 18		125 26 23	ns
$t_{TLH}/$ t_{THL}	Output Transition Time	2.0 4.5 6.0		25 8 7	70 15 13		85 18 16		100 22 19	ns

AC Characteristics for HCT: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HCT34		GD54HCT34		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
$t_{PLH}/$ t_{PHL}	Propagation Delay Time nA to nY	4.5		12	20		24		28	ns
$t_{TLH}/$ t_{THL}	Output Transition Time	4.5		8	15		19		22	ns

AC Waveform

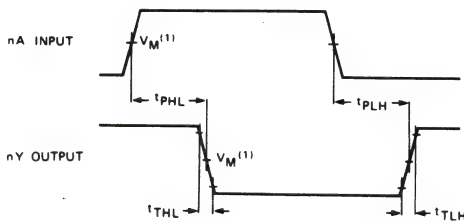


Fig. 3 Waveforms showing the input (nA) to output (nY) propagation delays and the output transition times.

Note to AC waveform

- (1) HC : $V_M=50\%$, $V_L=GND$ to V_{CC}
HCT: $V_M=1.3V$, $V_L=GND$ to $3V$.

GD54/74HC42, GD54/74HCT42

1-OF-10 DECODER

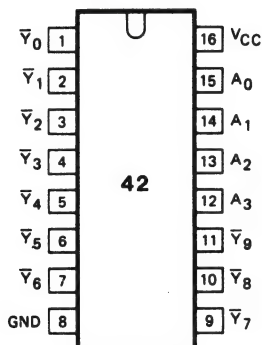
General Description

These devices are identical in pinout to the 54/74LS42. Data on the 4 input pins select one of the 10 outputs corresponding to the value of the BCD number on the inputs. An output will go low when selected, otherwise it remains high. If the input data is not a valid BCD number, i.e., a hexadecimal equivalent greater than 9, all outputs will remain high. These devices are characterized for operation over wide temperature ranges to meet industry and military specifications

Features

- Low Power consumption characteristic of CMOS devices
- Output drive capability: 10 LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts
for HCT 4.5 to 5.5 volts
- Low input current: 1μA Max.
- Low quiescent current: 80μA Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs

Pin Configuration



Suffix-Blank : Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package
Suffix-D : Small Outline Package

Function Table

INPUTS				OUTPUTS									
A ₃	A ₂	A ₁	A ₀	Y ₀	Y ₁	Y ₂	Y ₃	Y ₄	Y ₅	Y ₆	Y ₇	Y ₈	Y ₉
L	L	L	L	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	H	H	L	H	H	H	H	H	H	H
L	L	H	H	H	H	H	L	H	H	H	H	H	H
L	H	L	L	H	H	H	H	L	H	H	H	H	H
L	H	L	H	H	H	H	H	H	L	H	H	H	H
L	H	H	L	H	H	H	H	H	H	L	H	H	H
L	H	H	H	H	H	H	H	H	H	H	L	H	H
H	L	L	L	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L
H	L	H	L	H	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	H	H	H	H	H	H	H
H	H	L	L	H	H	H	H	H	H	H	H	H	H
H	H	L	H	H	H	H	H	H	H	H	H	H	H
H	H	H	L	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H	H	H

H=HIGH voltage level

L=LOW voltage level

Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC Supply voltage		-0.5	+7	V
I_{IK}, I_{OK}	DC input or output diode current	for $V_I < -0.5$ or $V_I > V_{CC} + 0.5V$		20	mA
I_O	DC output source or sink current	for $-0.5V < V_O < V_{CC} + 0.5V$		35	mA
I_{CC}	DC V_{CC} or GND current			70	mA
T_{stg}	Storage temperature range		-65	150	°C
P_D	Power dissipation per package	above +70°C: derate linearly with 8mW/K		500	mW
T_L	Lead temperature	At distance 1/16 ± 1/32 in. from case for 60 sec(CERAMIC) 10 sec(PLASTIC)		300 260	°C

Recommended Operating Conditions

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range V_{CC} : GD54/74HC Types GD54/74HCT Types	2 4.5	6 5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A : GD74 Types GD54 Types	-40 -55	+85 +125	°C
Input Rise and Fall times t_r, t_f : GD54/74HC Types at 2V at 4.5V at 6V GD54/74HCT Types at 4.5 V		1000 500 400 500	ns

Logic Diagram

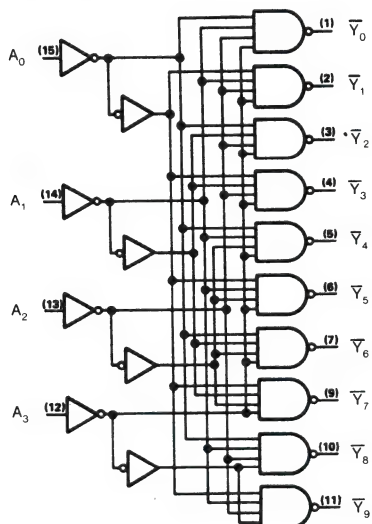


Fig. 1 Logic diagram

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HC42		GD54HC42		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2		1.5 3.15 4.2		V
V _{IL}	LOW level input voltage		2.0 4.5 6.0			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH}	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V
		or V _{IL}									
V _{OL}	LOW level output voltage	V _{IN} =V _{IH}	2.0 4.5 6.0			0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V
		or V _{IL}									
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	6.0			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	6.0			8		80		160	μA

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HCT42		GD54HCT42		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		4.5 to 5.5	2.0			2.0		2.0		V
V _{IL}	LOW level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH}	4.5	4.4	4.5		4.4		4.4		V
		or V _{IL}									
V _{OL}	LOW level output voltage	V _{IN} =V _{IH}	4.5			0.1		0.1		0.1	V
		or V _{IL}									
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	5.5			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	5.5			8		80		160	μA

AC Characteristics for HC: $t_r = t_f = 6\text{ns}$ $CL = 50\text{pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A = 25^\circ\text{C}$			GD74HC42		GD54HC42		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
$t_{PLH}/$ t_{PHL}	Propagation delay time An to \bar{Y}_n	2.0 4.5 6.0		65 17 14	150 30 26		190 38 32		225 45 38	ns
$t_{TLH}/$ t_{THL}	Output transition time	2.0 4.5 6.0		28 7 6	75 15 13		95 19 16		110 22 19	ns

AC Characteristics for HCT: $t_r = t_f = 6\text{ns}$ $CL = 50\text{pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A = 25^\circ\text{C}$			GD74HCT42		GD54HCT42		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
$t_{PLH}/$ t_{PHL}	Propagation delay time An to \bar{Y}_n	4.5		19	35		44		53	ns
$t_{TLH}/$ t_{THL}	Output transition time	4.5		7	15		19		22	ns

AC Waveforms

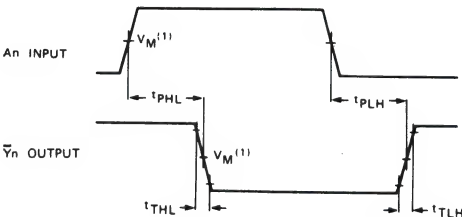


Fig. 3 Waveforms showing the input (An) to output (\bar{Y}_n) propagation delays and the output transition times.

Note to AC waveforms

(1) HC : $V_M = 50\%$. $V_L = \text{GND}$ to V_{CC}
HCT: $V_M = 1.3V$. $V_L = \text{GND}$ to $3V$.

GD54/74HC51, GD54/74HCT51

DUAL AND-OR-INVERT GATES

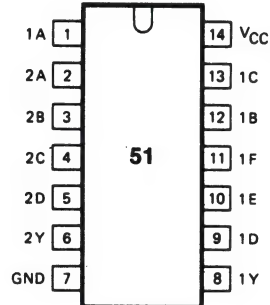
General Description

These devices are identical in pinout to the 54/74LS51. They contain one 2-wide 2-input & one 2-wide 3-input AND-OR-INVERT gates. These devices are characterized for operation over wide temperature ranges to meet industry and military specifications.

Features

- Low Power consumption characteristic of CMOS devices
- Output drive capability: 10 LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts
for HCT 4.5 to 5.5 volts
- Low input current: $1\mu\text{A}$ Max.
- Low quiescent current: $20\mu\text{A}$ Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs

Pin Configuration



Suffix-Blank : Plastic Dual In Line Package
 Suffix-J : Ceramic Dual In Line Package
 Suffix-D : Small Outline Package

Logic Symbol

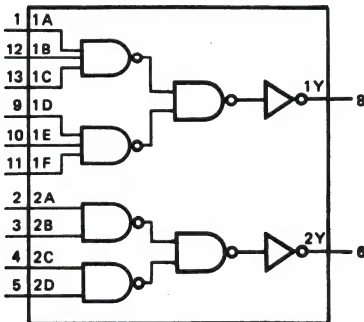


Fig. 1 Logic symbol

Function Table

INPUTS		OUTPUT
N*	M*	nY
L	L	H
H	L	L
L	H	L
H	H	L

$$N^* = 1A \cdot 1B \cdot 1C \text{ or } 2A \cdot 2B$$

$$M^* = 1D \cdot 1E \cdot 1F \text{ or } 2C \cdot 2D$$

$$1Y = 1A \cdot 1B \cdot 1C + 1D \cdot 1E \cdot 1F$$

$$2Y = 2A \cdot 2B + 2C \cdot 2D$$

Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC Supply voltage		-0.5	+7	V
I_{IK}, I_{OK}	DC input or output diode current	for $V_I < -0.5$ or $V_I > V_{CC} + 0.5V$		20	mA
I_O	DC output source or sink current	for $-0.5V < V_O < V_{CC} + 0.5V$		25	mA
I_{CC}	DC V_{CC} or GND current			50	mA
T_{stg}	Storage temperature range		-65	150	°C
P_D	Power dissipation per package	above +70°C: derate linearly with 8mW/K		500	mW
T_L	Lead temperature	At distance 1/16 ± 1/32 in. from case for 60 sec(CERAMIC) 10 sec(PLASTIC)		300 260	°C

Recommended Operating Conditions

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range V_{CC} : GD54/74HC Types GD54/74HCT Types	2 4.5	6 5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A : GD74 Types GD54 Types	-40 -55	+85 +125	°C
Input Rise and Fall times t_r, t_f : GD54/74HC Types at 2V at 4.5V at 6V GD54/74HCT Types at 4.5V		1000 500 400 500	ns

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HC51		GD54HC51		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2		1.5 3.15 4.2		V
V _{IL}	LOW level input voltage		2.0 4.5 6.0			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH}	I _{OH} =-20μA	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0	1.9 4.4 5.9		1.9 4.4 5.9		V
		or V _{IL}	I _{OH} =-4mA I _{OH} =-5.2mA	4.5 6.0	3.98 5.48	4.3 5.2	3.84 5.34		3.7 5.2		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH}	I _{OL} =20μA	2.0 4.5 6.0			0.1 0.1 0.1	0.1 0.1 0.1		0.1 0.1 0.1	V
		or V _{IL}	I _{OL} =4mA I _{OL} =5.2mA	4.5 6.0		0.17 0.15	0.26 0.26	0.33 0.33		0.4 0.4	
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	6.0			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	6.0			2		20		40	μA

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HCT51		GD54HCT51		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		4.5 to 5.5	2.0			2.0		2.0		V
V _{IL}	LOW level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH}	I _{OH} =-20μA	4.5	4.4	4.5	4.4		4.4		V
		or V _{IL}	I _{OH} =-4mA	4.5	3.98	4.3	3.84		3.7		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH}	I _{OL} =20μA	4.5		0.1		0.1		0.1	V
		or V _{IL}	I _{OL} =4mA	4.5		0.17	0.26	0.33		0.4	
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	5.5			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	5.5			2		20		40	μA

AC Characteristics for HC: $t_r=t_f=6\text{ns}$ $C_L=50\text{pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HC51		GD74HC51		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
$t_{PLH}/$ t_{PHL}	Propagation delay time Any Input to nY	2.0 4.5 6.0		54 13 11	125 25 21		158 32 27		186 37 32	ns
$t_{TLH}/$ t_{THL}	Output transition time	2.0 4.5 6.0		28 8 7	75 15 13		95 19 16		110 22 19	ns

AC Characteristics for HCT: $t_r=t_f=6\text{ns}$ $C_L=50\text{pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HCT51		GD54HCT51		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
$t_{PLH}/$ t_{PHL}	Propagation delay time Any Input to nY	4.5		17	29		36		41	ns
$t_{TLH}/$ t_{THL}	Output transition time	4.5		8	15		19		22	ns

AC Waveform

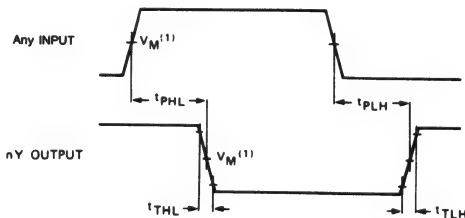


Fig. 3 Waveforms showing the (Any Input) to output (nY) propagation delays and the output transition times.

Note to AC waveform

- (1) HC : $V_M=50\%$, $V_L=\text{GND to } V_{CC}$
HCT: $V_M=1.3\text{V}$, $V_L=\text{GND to } 3\text{V}$.

GD54/74HC58, GD54/74HCT58

DUAL AND-OR GATES

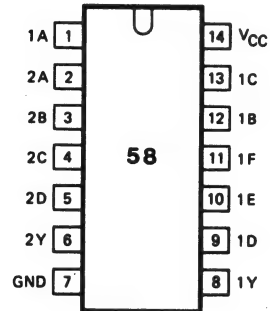
General Description

These devices are identical in pinout to the 54/74LS58. They contain one 2-wide 2-input & one 2-wide 3-input AND-OR gates. These devices are characterized for operation over wide temperature ranges to meet industry and military specifications.

Features

- Low Power consumption characteristic of CMOS devices
- Output drive capability: 10 LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts
for HCT 4.5 to 5.5 volts
- Low input current: $1\mu\text{A}$ Max.
- Low quiescent current: $20\mu\text{A}$ Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs.

Pin Configuration



Suffix-Blank : Plastic Dual In Line Package
 Suffix-J : Ceramic Dual In Line Package
 Suffix-D : Small Outline Package

Logic Symbol

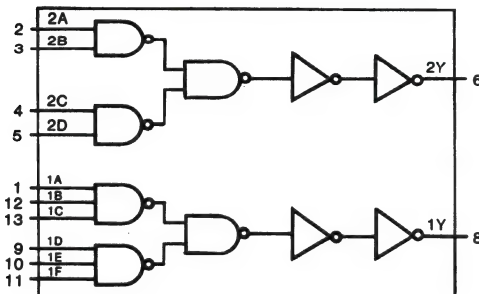


Fig. 1 Logic Symbol

Function Table

INPUTS		OUTPUT
N*	M*	nY
L	L	L
H	L	H
L	H	H
H	H	H

N* = 1A·1B·1C or 2A·2B

M* = 1D·1E·1F or 2C·2D

1Y = 1A·1B·1C + 1D·1E·1F

2Y = 2A·2B + 2C·2D

Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC Supply voltage		-0.5	+7	V
I_{IK}, I_{OK}	DC input or output diode current	for $V_I < -0.5$ or $V_I > V_{CC} + 0.5V$		20	mA
I_O	DC output source or sink current	for $-0.5V < V_O < V_{CC} + 0.5V$		25	mA
I_{CC}	DC V_{CC} or GND current			50	mA
T_{stg}	Storage temperature range		-65	150	°C
P_D	Power dissipation per package	above +70°C: derate linearly with 8mW/K		500	mW
T_L	Lead temperature	At distance 1/16 ± 1/32 in. from case for 60 sec(CERAMIC) 10 sec(PLASTIC)		300 260	°C

Recommended Operating Conditions

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range V_{CC} : GD54/74HC Types GD54/74HCT Types	2 4.5	6 5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A : GD74 Types GD54 Types	-40 -55	+85 +125	°C
Input Rise and Fall times t_r, t_f : GD54/74HC Types at 2V at 4.5V at 6V GD54/74HCT Types at 4.5V		1000 500 400 500	ns

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HC58		GD54HC58		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2		1.5 3.15 4.2		V
V _{IL}	LOW level input voltage		2.0 4.5 6.0			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH}	I _{OH} =-20μA	2.0	1.9	2.0			1.9		V
				4.5	4.4	4.5			4.4		
		or V _{IL}	I _{OH} =-4mA I _{OH} =-5.2mA	6.0	5.9	6.0			5.9		
				4.5	3.98	4.3			3.7		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH}	I _{OL} =20μA	2.0			0.1	0.1		0.1	V
				4.5			0.1	0.1		0.1	
		or V _{IL}	I _{OL} =4mA I _{OL} =5.2mA	6.0			0.1	0.1		0.1	
				4.5		0.17	0.26	0.33		0.4	
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	6.0			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	6.0			2		20		40	μA

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HCT58		GD54HCT58		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		4.5 to 5.5	2.0			2.0		2.0		V
V _{IL}	LOW level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH}	I _{OH} =-20μA	4.5	4.4	4.5	4.4		4.4		V
				4.5	3.98	4.3	3.84		3.7		
		or V _{IL}	I _{OH} =-4mA	4.5	3.98	4.3	3.84		3.7		
				4.5							
V _{OL}	LOW level output voltage	V _{IN} =V _{IH}	I _{OL} =20μA	4.5			0.1	0.1		0.1	V
				4.5			0.1	0.1		0.1	
		or V _{IL}	I _{OL} =4mA	4.5		0.17	0.26	0.33		0.4	
				4.5		0.17	0.26	0.33		0.4	
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	5.5			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	5.5			2		20		40	μA

AC Characteristics for HC: $t_r=t_f=6\text{ns}$ $C_L=50\text{pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HC58		GD54HC58		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
$t_{PLH}/$ t_{PHL}	Propagation delay time Any Input to nY	2.0 4.5 6.0		54 13 11	125 25 21		158 32 27		186 37 32	ns
$t_{TLH}/$ t_{THL}	Output transition time	2.0 4.5 6.0		28 8 7	75 15 13		95 19 16		110 22 19	ns

AC Characteristics for HCT: $t_r=t_f=6\text{ns}$ $C_L=50\text{pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HCT58		GD54HCT58		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
$t_{PLH}/$ t_{PHL}	Propagation delay time Any Input to nY	4.5		17	29		36		41	ns
$t_{TLH}/$ t_{THL}	Output transition time	4.5		8	15		19		22	ns

AC Waveform

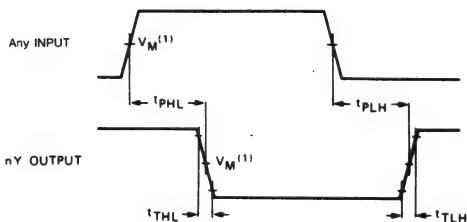


Fig. 2 Waveforms showing the (Any Input) to output (nY) propagation delays and the output transition times.

Note to AC waveform

- (1) HC : $V_M=50\%$, $V_L=\text{GND}$ to V_{CC}
HCT: $V_M=1.3\text{V}$; $V_L=\text{GND}$ to 3V .

GD54/74HC73, GD54/74HCT73

DUAL J-K FLIP-FLOPS WITH CLEAR

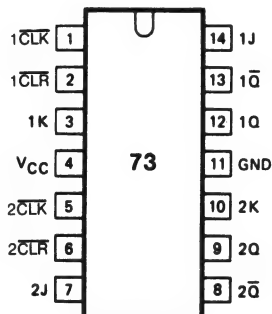
General Description

These devices are identical in pinout to the 54/74LS73. These flip-flops are edge sensitive to the clock input and change state on the negative going transition of the clock pulse. Each flip-flop has independent J, K, Clock, and Clear inputs and Q and \bar{Q} outputs, Clear is independent of the clock and accomplished by a Low level on the input. These devices are characterized for operation over wide temperature ranges to meet industry and military specifications.

Features

- Low Power consumption characteristic of CMOS devices
- Output drive capability: 10 LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts
for HCT 4.5 to 5.5 volts
- Low input current: $1\mu\text{A}$ Max.
- Low quiescent current: $40\mu\text{A}$ Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs

Pin Configuration



Suffix-Blank : Plastic Dual In Line Package
 Suffix-J : Ceramic Dual In Line Package
 Suffix-D : Small Outline Package

Logic Symbol

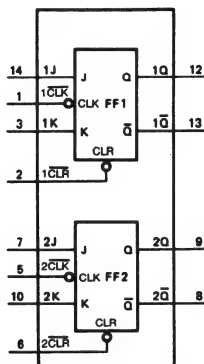


Fig. 1 Logic Symbol

Function Table

OPERATING MODE	INPUTS			OUTPUTS	
	nCLR	nCLK	nJ/nK	nQ	$\bar{n}Q$
asynchronous reset	L	X	X	L	H
toggle	H	\downarrow	h	\bar{q}	q
load "0" (reset)	H	\downarrow	l	L	H
load "1" (set)	H	\downarrow	h	H	L
hold "no change"	H	\downarrow	l	q	\bar{q}

H = HIGH voltage level
 h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CLK transition
 L = LOW voltage level
 l = LOW voltage level one set-up time prior to the LOW-to-HIGH CLK transition
 q = lower case letters indicate the state of the referenced output one set-up time prior to the LOW-to-HIGH CLK transition
 X = don't care
 \downarrow = HIGH-to-LOW CLK transition

Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC Supply voltage		-0.5	+7	V
I_{IK}, I_{OK}	DC input or output diode current	for $V_I < -0.5$ or $V_I > V_{CC} + 0.5V$		20	mA
I_O	DC output source or sink current	for $-0.5V < V_O < V_{CC} + 0.5V$		25	mA
I_{CC}	DC V_{CC} or GND current			50	mA
T_{slg}	Storage temperature range		-65	150	°C
P_D	Power dissipation per package	above +70°C: derate linearly with 8mW/K		500	mW
T_L	Lead temperature	At distance 1/16 ± 1/32 in. from case for 60 sec(CERAMIC) 10 sec(PLASTIC)		300 260	°C

Recommended Operating Conditions

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range V_{CC} : GD54/74HC Types GD54/74HCT Types	2 4.5	6 5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A : GD74 Types GD54 Types	-40 -55	+85 +125	°C
Input Rise and Fall times t_r, t_f : GD54/74HC Types at 2V at 4.5V at 6V GD54/74HCT Types at 4.5V		1000 500 400 500	ns

Logic Diagram

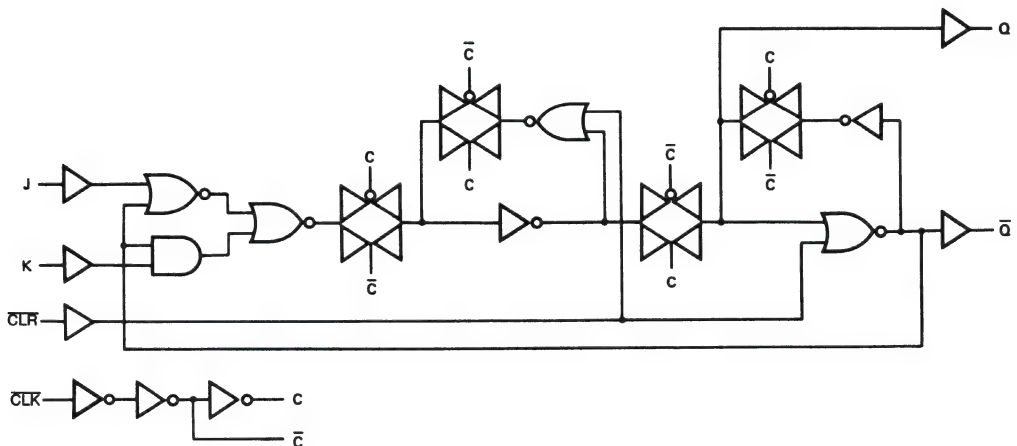


Fig. 2 Logic diagram (one flip-flop)

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HC73		GD54HC73		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2		1.5 3.15 4.2		V
V _{IL}	LOW level input voltage		2.0 4.5 6.0			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH}	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V
		or V _{IL}									
V _{OL}	LOW level output voltage	V _{IN} =V _{IH}	2.0 4.5 6.0			0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V
		or V _{IL}									
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	6.0			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	6.0			4		40		80	μA

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HCT73		GD54HCT73		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		4.5 to 5.5	2.0			2.0		2.0		V
V _{IL}	LOW level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH}	4.5	4.4	4.5		4.4		4.4		V
		or V _{IL}	4.5	3.98	4.3		3.84		3.7		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH}	4.5			0.1		0.1		0.1	V
		or V _{IL}	4.5		0.17	0.26		0.33		0.4	
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	5.5			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	5.5			4		40		80	μA

Timing Requirements for HC: $t_r = t_f = 6\text{ns}$ $C_L = 50\text{ pF}$

SYMBOL	PARAMETER		V_{CC} (V)	$T_A = 25^\circ\text{C}$			GD74HC73		GD54HC73		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_w	Pulse width	$\overline{\text{CLR}}$	2.0	80	30		100		120		ns
			4.5	16	10		20		25		
			6.0	14	8		18		22		
		$\overline{\text{CLK}}$	2.0	80	30		100		120		ns
			4.5	16	10		20		25		
			6.0	14	8		18		22		
t_{su}	Setup time	Data to $\overline{\text{CLK}}$	2.0	60	30		80		100		ns
			4.5	15	10		18		20		
			6.0	14	8		16		18		
t_{rec}	Recovery time	$\overline{\text{CLR}}$ to $\overline{\text{CLK}}$	2.0	5	0		5		5		ns
			4.5	5	0		5		5		
			6.0	5	0		5		5		
t_h	Hold time	$\overline{\text{CLK}}$ to Data	2.0	3	0		3		3		ns
			4.5	3	0		3		3		
			6.0	3	0		3		3		

AC Characteristics for HC: $t_r = t_f = 6\text{ns}$ $C_L = 50\text{ pF}$

SYMBOL	PARAMETER		V_{CC} (V)	$T_A = 25^\circ\text{C}$			GD74HC73		GD54HC73		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
f_{max}	Maximum clock Pulse frequency		2.0	6	20		5		4		MHz
			4.5	30	65		25		20		
			6.0	35	75		30		25		
$t_{PLH} /$ t_{PHL}	Propagation Delay time $n\overline{\text{CLK}}$ to nQ		2.0		46	160		200		240	ns
			4.5		17	30		40		50	
			6.0		15	28		35		45	
$t_{PLH} /$ t_{PHL}	Propagation Delay time $n\overline{\text{CLK}}$ to $n\overline{Q}$		2.0		46	160		200		240	ns
			4.5		17	30		40		50	
			6.0		15	28		35		45	
$t_{PLH} /$ t_{PHL}	Propagation Delay time $n\overline{\text{CLR}}$ to nQ , $n\overline{Q}$		2.0		45	170		210		250	ns
			4.5		16	30		40		50	
			6.0		14	28		35		45	
$t_{TLH} /$ t_{THL}	Output Transition time		2.0		25	70		85		100	ns
			4.5		8	15		18		22	
			6.0		7	13		16		19	

Timing Requirements for HCT : $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER		V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HCT73		GD74HCT73		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_w	Pulse width	$\overline{\text{CLR}}$	4.5	18	10		20		25		ns
		$\overline{\text{CLK}}$	4.5	16	10		20		25		ns
t_{su}	Setup time	Data to $\overline{\text{CLK}}$	4.5	15	10		18		20		ns
t_{rec}	Recovery time	$\overline{\text{CLR}}$ to $\overline{\text{CLK}}$	4.5	5	0		5		5		ns
t_h	Hold time	$\overline{\text{CLK}}$ to Data	4.5	3	0		3		3		ns

AC Characteristics for HCT : $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HCT73		GD54HCT73		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
f_{max}	Maximum clock Pulse frequency	4.5	27	54		22		18		MHz
$t_{PLH} /$ t_{PHL}	Propagation Delay time $n\overline{\text{CLK}}$ to nQ	4.5		18	35		44		53	ns
$t_{PLH} /$ t_{PHL}	Propagation Delay time $n\overline{\text{CLK}}$ to $n\overline{Q}$	4.5		18	35		44		53	ns
$t_{PLH} /$ t_{PHL}	Propagation Delay time $n\overline{\text{CLR}}$ to nQ , $n\overline{Q}$	4.5		20	35		44		53	ns
$t_{TLH} /$ t_{THL}	Output Transition time	4.5		8	15		18		22	ns

AC Waveforms

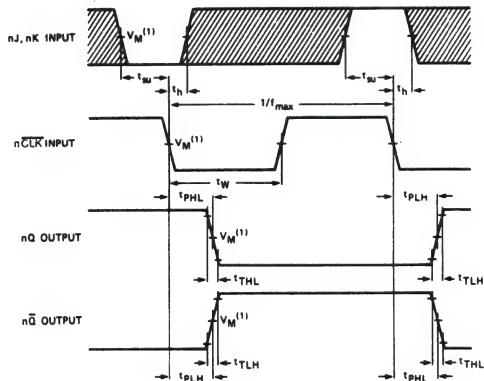


Fig. 3 Waveforms showing the clock ($n\overline{CLK}$) to output (nQ , $n\overline{Q}$) propagation delays, the clock pulse width, the J and K to $n\overline{CLK}$ set-up and hold times, the output transition times and the maximum clock pulse frequency.

Note to Fig. 3

The shaded areas indicate when the input is permitted to change for predictable output performance.

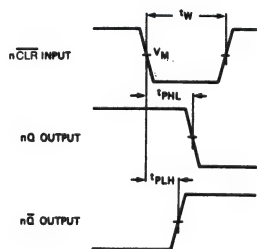


Fig. 4 Waveforms showing the clear ($n\overline{CLR}$) input to output (nQ , $n\overline{Q}$) propagation delays and the clear pulse width.

Note to AC waveforms

- (1) HC : $V_M = 50\%$; $V_i = \text{GND to } V_{CC}$.
HCT : $V_M = 1.3V$; $V_i = \text{GND to } 3V$.

GD54/74HC74, GD54/74HCT74

DUAL D-TYPE FLIP-FLOPS WITH PRESET & CLEAR

General Description

These devices are identical in pinout to the 54/74LS74. They consist of two D-type flip-flops with individual preset, clear, and clock inputs. Information at a D-input is transferred to the corresponding Q output on the next positive going edge of the clock input. Both Q and \bar{Q} outputs are available from each flip-flop. The preset & clear inputs are asynchronous. These devices are characterized for operation over wide temperature ranges to meet industry and military specifications.

Features

- Low Power consumption characteristic of CMOS devices
- Output drive capability: 10 LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts
for HCT 4.5 to 5.5 volts
- Low input current: 1 μ A Max.
- Low quiescent current: 40 μ A Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs

Logic Diagram

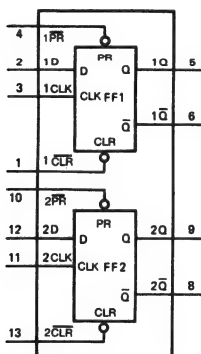
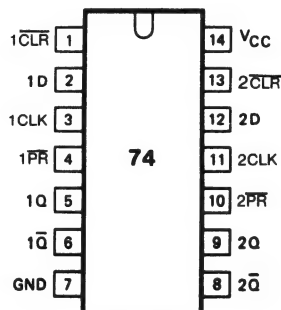


Fig. 1 Logic diagram

Pin Configuration



Suffix-Blank : Plastic Dual In Line Package
 Suffix-J : Ceramic Dual In Line Package
 Suffix-D : Small Outline Package

Function Table

INPUTS				OUTPUTS	
\overline{PR}	\overline{CLR}	CLK	nD	nQ	n \bar{Q}
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H

INPUTS				OUTPUTS	
\overline{PR}	\overline{CLR}	CLK	nD	Q _{n+1}	\bar{Q}_{n+1}
H	H	↑	L	L	H
H	H	↑	H	H	L

H = HIGH voltage level
 L = LOW voltage level
 X = don't care
 ↑ = LOW-to-HIGH CLK transition
 Q_{n+1} = state after the next LOW-to-HIGH CLK transition

Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC Supply voltage		-0.5	+7	V
I_{IK}, I_{OK}	DC input or output diode current	for $V_I < -0.5$ or $V_I > V_{CC} + 0.5V$		20	mA
I_O	DC output source or sink current	for $-0.5V < V_O < V_{CC} + 0.5V$		25	mA
I_{CC}	DC V_{CC} or GND current			50	mA
T_{stg}	Storage temperature range		-65	150	°C
P_D	Power dissipation per package	above +70°C: derate linearly with 8mW/K		500	mW
T_L	Lead temperature	At distance 1/16 ± 1/32 in. from case for 60 sec(CERAMIC) 10 sec(PLASTIC)		300 260	°C

Recommended Operating Conditions

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range V_{CC} : GD54/74HC Types GD54/74HCT Types	2 4.5	6 5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A : GD74 Types GD54 Types	-40 -55	+85 +125	°C
Input Rise and Fall times t_r, t_f : GD54/74HC Types at 2V at 4.5V at 6V GD54/74HCT Types at 4.5V		1000 500 400 500	ns

Logic diagram

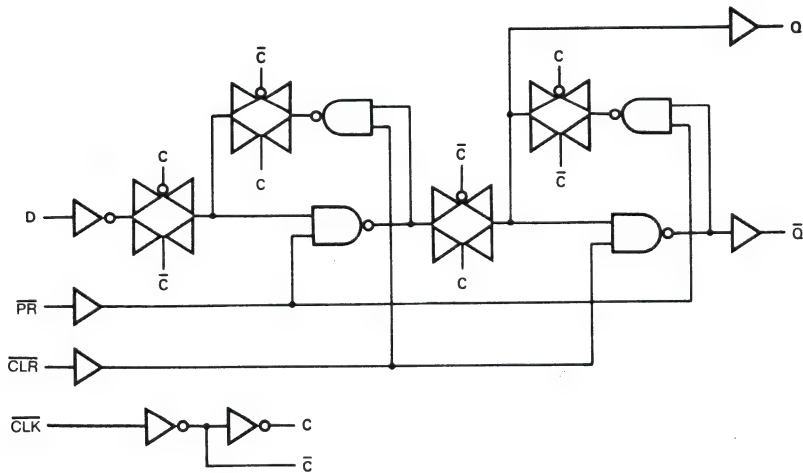


Fig. 2 Logic diagram (one flip-flop)

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HC 74		GD54HC 74		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2		1.5 3.15 4.2		V
V _{IL}	LOW level input voltage		2.0 4.5 6.0			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH}	I _{OH} =-20μA	2.0	1.9	2.0		1.9		1.9	V
				4.5	4.4	4.5		4.4		4.4	
		or V _{IL}	I _{OH} =-4mA I _{OH} =-5.2mA	4.5	3.98	4.3		3.84		3.7	
				6.0	5.48	5.2		5.34		5.2	
V _{OL}	LOW level output voltage	V _{IN} =V _{IH}	I _{OL} =20μA	2.0			0.1	0.1		0.1	V
				4.5			0.1	0.1		0.1	
		or V _{IL}	I _{OL} =4mA I _{OL} =5.2mA	4.5		0.17	0.26	0.33		0.4	
				6.0		0.15	0.26	0.33		0.4	
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	6.0			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	6.0			4		40		80	μA

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HCT74		GD54HCT74		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		4.5 to 5.5	2.0			2.0		2.0		V
V _{IL}	LOW level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH}	I _{OH} =-20μA	4.5	4.4	4.5		4.4		4.4	V
		or V _{IL}	I _{OH} =-4mA	4.5	3.98	4.3		3.84		3.7	
V _{OL}	LOW level output voltage	V _{IN} =V _{IH}	I _{OL} =20μA	4.5			0.1	0.1		0.1	V
		or V _{IL}	I _{OL} =4mA	4.5		0.17	0.26	0.33		0.4	
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	5.5			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	5.5			4		40		80	μA

Timing Requirements for HC: $t_r = t_f = 6\text{ns}$ $C_L = 50\text{ pF}$

SYMBOL	PARAMETER		V_{CC} (V)	$T_A = 25^\circ\text{C}$			GD74HC74		GD54HC74		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_w	Pulse width	\overline{PR} or \overline{CLR} (low)	2.0	80	30		100		120		ns
			4.5	16	10		20		25		
			6.0	14	8		18		22		
		CLK (high or low)	2.0	80	30		100		120		ns
			4.5	16	10		20		25		
			6.0	14	8		18		22		
t_{su}	Setup time	Data before CLK \uparrow	2.0	60	30		80		100		ns
			4.5	15	10		18		20		
			6.0	14	8		16		18		
t_{rec}	Recovery time	\overline{PR} or \overline{CLR} inactive	2.0	5	0		5		5		ns
			4.5	5	0		5		5		
			6.0	5	0		5		5		
t_h	Hold time	Data after CLK \uparrow	2.0	3	0		3		3		ns
			4.5	3	0		3		3		
			6.0	3	0		3		3		

AC Characteristics for HC: $t_r = t_f = 6\text{ns}$ $C_L = 50\text{ pF}$

SYMBOL	PARAMETER		V_{CC} (V)	$T_A = 25^\circ\text{C}$			GD74HC74		GD54HC74		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
f_{max}	Maximum Clock Pulse Frequency		2.0	6	20		5		4		MHz
			4.5	30	65		25		20		
			6.0	35	75		30		25		
$t_{PLH} /$ t_{PHL}	Propagation Delay Time $nCLK$ to nQ , $n\overline{Q}$		2.0		45	170		210		250	ns
			4.5		15	30		40		50	
			6.0		14	28		35		45	
$t_{PLH} /$ t_{PHL}	Propagation Delay Time $n\overline{PR}$ to nQ , $n\overline{Q}$		2.0		45	180		220		260	ns
			4.5		14	32		42		52	
			6.0		13	28		35		45	
$t_{PLH} /$ t_{PHL}	Propagation Delay Time $nCLR$ to nQ , $n\overline{Q}$		2.0		45	180		220		260	ns
			4.5		14	32		42		52	
			6.0		13	28		35		45	
$t_{TLH} /$ t_{THL}	Output Transition Time		2.0		25	70		85		100	ns
			4.5		8	15		18		22	
			6.0		7	13		16		18	

Timing Requirements for HCT : $t_r = t_f = 6\text{ns}$ $C_L = 50\text{ pF}$

SYMBOL	PARAMETER		V_{CC} (V)	$T_A = 25^\circ\text{C}$			GD74HCT74		GD54HCT74		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_w	Pulse width	\overline{PR} or \overline{CLR} (low)	4.5	18	10		20		25		ns
		CLK (high or low)	4.5	16	10		20		25		ns
t_{su}	Setup time	Data before CLK \uparrow	4.5	15	10		18		20		ns
t_{rec}	Recovery time	\overline{PR} or \overline{CLR} inactive	4.5	5	0		5		5		ns
t_h	Hold time	Data after CLK \uparrow	4.5	3	0		3		3		ns

AC Characteristics for HCT : $t_r = t_f = 6\text{ns}$ $C_L = 50\text{ pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A = 25^\circ\text{C}$			GD74HCT74		GD54HCT74		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
f_{max}	Maximum Clock Pulse Frequency	4.5	27	54		22		18		MHz
$t_{PLH} /$ t_{PHL}	Propagation Delay Time $nCLK$ to nQ , $n\overline{Q}$	4.5		18	35		44		53	ns
$t_{PLH} /$ t_{PHL}	Propagation Delay Time $n\overline{PR}$ to nQ , $n\overline{Q}$	4.5		20	35		44		53	ns
$t_{PLH} /$ t_{PHL}	Propagation Delay Time $n\overline{CLR}$ to nQ , $n\overline{Q}$	4.5		20	35		44		53	ns
$t_{TLH} /$ t_{THL}	Output Transition Time	4.5		8	15		18		22	ns

AC Waveform

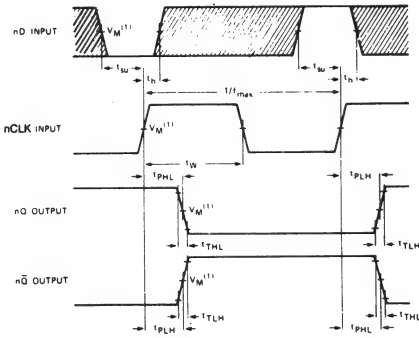


Fig. 3 Waveforms showing the clock (nCLK) to output (nQ, nQ) propagation delays, the clock pulse width, the nD to nCLK set-up, the nCLK to nD hold times, the output transition times and the maximum clock pulse frequency.

Note to Fig. 3

The shaded areas indicate when the input is permitted to change for predictable output performance.

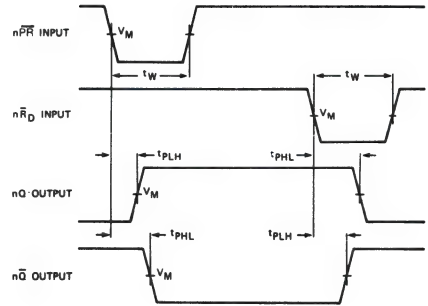


Fig. 4 Waveforms showing the preset and clear input to output (nQ, nQ) propagation delays and the preset and clear pulse width.

Note to AC waveforms

(1) HC: $V_M = 50\%$; $V_I = \text{GND}$ to V_{CC} .

HCT: $V_M = 1.3V$; $V_I = \text{GND}$ to $3V$.

GD54/74HC75, GD54/74HCT75

DUAL 2-BIT (4-BIT) BISTABLE LATCHES

General Description

These devices are identical in pinout to the 54/74LS75. They consist of two independent 2-bit transparent latches. This latch is suited for use as a temporary storage of binary information. Information present at the data input is transferred to the Q output when the enable is high. When the enable goes low, the information that was present at the data input at the time the transition occurred is contained at the Q output until the enable is permitted to go high again. These devices are characterized for operation over wide temperature ranges to meet industry and military specifications.

Features

- Low Power consumption characteristic of CMOS devices
- Output drive capability: 10 LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts
for HCT 4.5 to 5.5 volts
- Low input current: 1 μ A Max.
- Low quiescent current: 40 μ A Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs

Logic Symbol

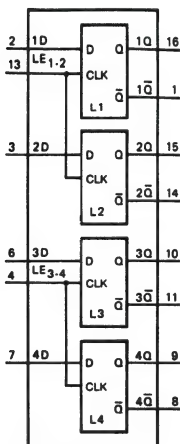
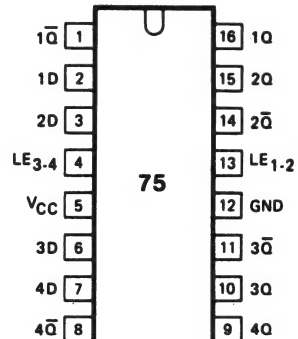


Fig. 1 Logic symbol

Pin Configuration



Suffix-Blank : Plastic Dual In Line Package
 Suffix-J : Ceramic Dual In Line Package
 Suffix-D : Small Outline Package

Function Table

OPERATING MODES	INPUTS		OUTPUTS	
	LE _{n-n}	nD	nQ	nQ $\bar{}$
data enabled	H	L	L	H
	H	H	H	L
data latched	L	X	q	\bar{q}

H = HIGH voltage level

L = LOW voltage level

q = lower case letters indicate the state of the referenced output one set-up time prior to the Low-to-HIGH LE_{n-n} transition.

X = don't care

Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC Supply voltage		-0.5	+7	V
I_{IK}, I_{OK}	DC input or output diode current	for $V_I < -0.5$ or $V_I > V_{CC} + 0.5V$		20	mA
I_O	DC output source or sink current	for $-0.5V < V_O < V_{CC} + 0.5V$		25	mA
I_{CC}	DC V_{CC} or GND current			50	mA
T_{stg}	Storage temperature range		-65	150	°C
P_D	Power dissipation per package	above +70°C: derate linearly with 8mW/K		500	mW
T_L	Lead temperature	At distance $1/16 \pm 1/32$ in. from case for 60 sec(CERAMIC) 10 sec(PLASTIC)		300 260	°C

Recommended Operating Conditions

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range V_{CC} : GD54/74HC Types GD54/74HCT Types	2 4.5	6 5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A : GD74 Types GD54 Types	-40 -55	+85 +125	°C
Input Rise and Fall times t_r, t_f : GD54/74HC Types at 2V at 4.5V at 6V GD54/74HCT Types at 4.5 V		1000 500 400 500	ns

Logic Diagram

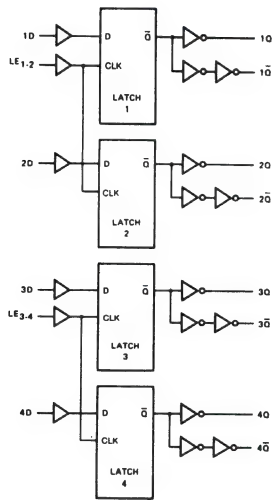


Fig. 2 Logic diagram

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HC75		GD54HC75		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2		1.5 3.15 4.2		V
V _{IL}	LOW level input voltage		2.0 4.5 6.0			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH}	I _{OH} =-20μA	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0	1.9 4.4 5.9		1.9 4.4 5.9		V
			I _{OH} =-4mA	4.5 6.0	3.98 5.48	4.3 5.2	3.84 5.34		3.7 5.2		
		or V _{IL}	I _{OH} =-5.2mA	4.5 6.0	3.98 5.48	4.3 5.2	3.84 5.34		3.7 5.2		
			I _{OH} =-5.2mA	4.5 6.0	3.98 5.48	4.3 5.2	3.84 5.34		3.7 5.2		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH}	I _{OL} =20μA	2.0 4.5 6.0			0.1 0.1 0.1		0.1 0.1 0.1		V
			I _{OL} =4mA	4.5 6.0		0.17 0.15	0.26 0.26		0.33 0.33		
		or V _{IL}	I _{OL} =4mA	4.5 6.0		0.17 0.15	0.26 0.26		0.33 0.33		
			I _{OL} =5.2mA	4.5 6.0		0.17 0.15	0.26 0.26		0.33 0.33		
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	6.0			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	6.0			4		40		80	μA

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HCT75		GD54HCT75		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		4.5 to 5.5	2.0			2.0		2.0		V
V _{IL}	LOW level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH}	I _{OH} =-20μA	4.5	4.4	4.5	4.4		4.4		V
		or V _{IL}	I _{OH} =-4mA	4.5	3.98	4.3	3.84		3.7		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH}	I _{OL} =20μA	4.5			0.1		0.1		V
		or V _{IL}	I _{OL} =4mA	4.5		0.17	0.26		0.33		
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	5.5			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	5.5			4		40		80	μA

Timing Requirements for HC: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HC75		GD54HC75		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_w	Pulse width	LE_n High	2.0	80	30		100		120	ns
			4.5	16	10		20		25	
			6.0	14	8		18		22	
t_{su}	Setup time	Data before $LE \downarrow$	2.0	60	30		100		120	ns
			4.5	12	10		20		25	
			6.0	10	8		18		22	
t_h	Hold time	Data after $LE \downarrow$	2.0	3	0		3		3	ns
			4.5	3	0		3		3	
			6.0	3	0		3		3	

AC Characteristics for HC: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HC75		GD54HC75		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
$t_{PLH}/$ t_{PHL}	Propagation Delay Time nD to nQ	2.0		32	110		140		160	ns
		4.5		12	22		28		32	
		6.0		10	19		24		28	
$t_{PLH}/$ t_{PHL}	Propagation Delay Time nD to $n\bar{Q}$	2.0		32	110		140		160	ns
		4.5		12	22		28		32	
		6.0		10	19		24		28	
$t_{PLH}/$ t_{PHL}	Propagation Delay Time LE_n to nQ	2.0		34	110		140		160	ns
		4.5		14	24		30		34	
		6.0		12	20		25		30	
$t_{PLH}/$ t_{PHL}	Propagation Delay Time LE_n to $n\bar{Q}$	2.0		34	110		140		160	ns
		4.5		14	24		30		34	
		6.0		12	20		25		30	
$t_{TLH}/$ t_{THL}	Output Transition Time	2.0		25	70		85		100	ns
		4.5		8	15		18		22	
		6.0		7	13		16		19	

Timing Requirements for HCT: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HCT75		GD54HCT75		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_w	Pulse width	LE_n high	4.5	16	10		20		25	ns
t_{su}	Setup time	Data before $LE \downarrow$	4.5	12	10		20		25	ns
t_h	Hold time	Data after $LE \downarrow$	4.5	3	0		3		3	ns

AC Characteristics for HCT: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HCT75		GD54HCT75		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
$t_{PLH}/$ t_{PHL}	Propagation Delay Time nD to nQ	4.5		14	24		30		34	ns
$t_{PLH}/$ t_{PHL}	Propagation Delay Time nD to $n\bar{Q}$	4.5		14	24		30		34	ns
$t_{PLH}/$ t_{PHL}	Propagation Delay Time LE_n to nQ	4.5		16	26		32		36	ns
$t_{PLH}/$ t_{PHL}	Propagation Delay Time LE_n to $n\bar{Q}$	4.5		16	26		32		36	ns
$t_{TLH}/$ t_{THL}	Output Transition Time	4.5		8	15		18		22	ns

AC Waveforms

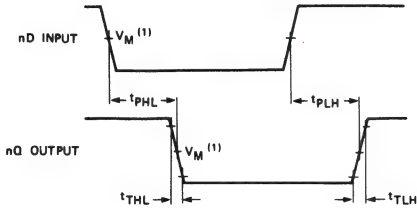


Fig. 3 Waveforms showing the data input (nD) to output (nQ) propagation delays and the output transition times.

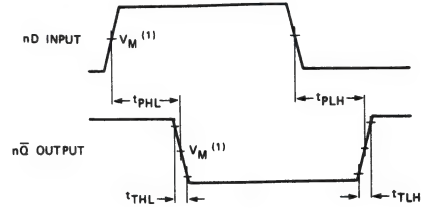


Fig. 4 Waveforms showing the data input (nD) to output (nQ) propagation delays and the output transition times.

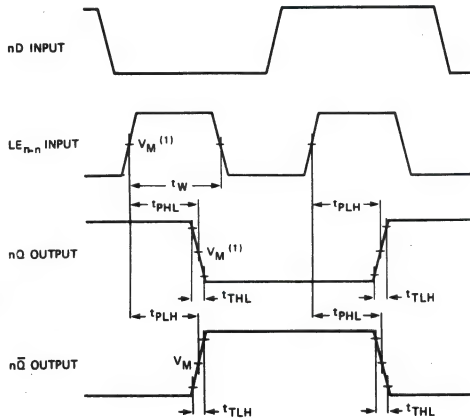


Fig. 5 Waveforms showing the latch enable input (LE_{n-n}) pulse width, the latch enable input to outputs (nQ, $n\bar{Q}$) propagation delays and the output transition times.

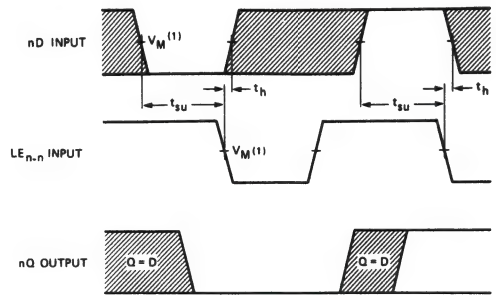


Fig. 6 Waveforms showing the data set-up and hold times for nD input to LE_{n-n} input.

Note to Fig. 6

The shaded areas indicate when the input is permitted to change for predictable output performance.

Note to AC waveforms

- (1) HC : $V_M = 50\%$; $V_I = GND$ to V_{CC} .
HCT : $V_M = 1.3V$; $V_I = GND$ to $3V$.

GD54/74HC76, GD54/74HCT76

DUAL J-K FLIP-FLOPS WITH PRESET & CLEAR

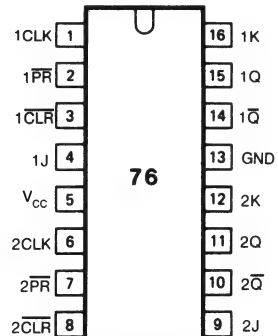
General Description

These devices are identical in pinout to the 54/74LS76. These flip-flops are edge sensitive to the clock input and change state on the negative going transition of the clock pulse. Each flip-flop has independent J, K, clock, preset, and clear inputs and Q and \bar{Q} outputs clear and preset are independent of the clock and accomplished by a low logic level on the corresponding input. These devices are characterized for operation over wide temperature ranges to meet industry and military specifications.

Features

- Low Power consumption characteristic of CMOS devices
- Output drive capability: 10 LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts
for HCT 4.5 to 5.5 volts
- Low input current: 1 μ A Max.
- Low quiescent current: 40 μ A Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs

Pin Configuration



Suffix-Blank : Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package
Suffix-D : Small Outline Package

Function Table

INPUTS					OUTPUTS	
\overline{PR}	\overline{CLR}	CLK	J	K	Q	\bar{Q}
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H \uparrow	H \uparrow
H	H	\downarrow	L	L	Q ₀	\bar{Q}_0
H	H	\downarrow	H	L	H	L
H	H	\downarrow	L	H	L	H
H	H	\downarrow	H	H	TOGGLE	
H	H	H	X	X	Q ₀	\bar{Q}_0

* This configuration is nonstable; that is it will not persist when either preset or clear returns to its inactive (high) level.

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HC76		GD54HC76		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2		1.5 3.15 4.2		V
V _{IL}	LOW level input voltage		2.0 4.5 6.0			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH}	I _{OH} =-20μA	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0	1.9 4.4 5.9		1.9 4.4 5.9		V
			I _{OH} =-4mA	4.5 6.0	3.98 5.48	4.3 5.2	3.84 5.34		3.7 5.2		
		or V _{IL}	I _{OH} =-4mA	4.5 6.0	3.98 5.48	4.3 5.2	3.84 5.34		3.7 5.2		
			I _{OH} =-5.2mA	6.0	5.48	5.2	5.34		5.2		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH}	I _{OL} =20μA	2.0 4.5 6.0			0.1 0.1 0.1	0.1 0.1 0.1		0.1 0.1 0.1	V
			I _{OL} =4mA	4.5 6.0		0.17 0.15	0.26 0.26	0.33 0.33		0.4 0.4	
		or V _{IL}	I _{OL} =4mA	4.5 6.0		0.17 0.15	0.26 0.26	0.33 0.33		0.4 0.4	
			I _{OL} =5.2mA	6.0		0.15	0.26	0.33		0.4	
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	6.0			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	6.0			4		40		80	μA

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HCT76		GD54HCT76		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		4.5 to 5.5	2.0			2.0		2.0		V
V _{IL}	LOW level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH}	I _{OH} =-20μA	4.5	4.4	4.5	4.4		4.4		V
		or V _{IL}	I _{OH} =-4mA	4.5	3.98	4.3	3.84		3.7		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH}	I _{OL} =20μA	4.5			0.1	0.1		0.1	V
		or V _{IL}	I _{OL} =4mA	4.5		0.17	0.26	0.33		0.4	
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	5.5			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	5.5			4		40		80	μA

Timing Requirements for HC: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER		V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HC76		GD54HC76		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_w	Pulse width	$\overline{PR}, \overline{CLR}$	2.0	80	30		100		120		ns
			4.5	16	10		20		25		
			6.0	14	8		18		22		
		CLK	2.0	80	30		100		120		ns
			4.5	16	10		20		25		
			6.0	14	8		18		22		
t_{su}	Set up Time	Data to CLK	2.0	60	30		80		100		ns
			4.5	15	10		18		20		
			6.0	14	8		16		18		
t_{rec}	Recovery time	$\overline{PR}, \overline{CLR}$ to CLK	2.0	5	0		5		5		ns
			4.5	5	0		5		5		
			6.0	5	0		5		5		
t_h	Hold Time	CLK to Data	2.0	3	0		3		3		ns
			4.5	3	0		3		3		
			6.0	3	0		3		3		

AC Characteristics for HC: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER		V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HC76		GD54HC76		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
f_{max}	Maximum Clock Pulse Frequency		2.0	6	20		5		4		MHz
			4.5	30	65		25		20		
			6.0	35	75		30		25		
t_{PLH} / t_{PHL}	Propagation Delay Time nCLK to nQ		2.0		46	160		200		240	ns
			4.5		15	30		40		50	
			6.0		14	28		35		45	
t_{PLH} / t_{PHL}	Propagation Delay Time nCLK to n \overline{Q}		2.0		50	160		200		240	ns
			4.5		17	30		40		50	
			6.0		16	28		35		45	
t_{PLH} / t_{PHL}	Propagation Delay Time n \overline{PR} to nQ, n \overline{Q}		2.0		45	155		190		230	ns
			4.5		15	28		38		45	
			6.0		14	26		34		42	
t_{PLH} / t_{PHL}	Propagation Delay time n \overline{CLR} to nQ, n \overline{Q}		2.0		45	155		190		230	ns
			4.5		15	28		38		45	
			6.8		14	26		34		42	
t_{TLH} / t_{THL}	Output Transition time		2.0		25	70		85		100	ns
			4.5		8	15		18		22	
			6.0		7	13		16		19	

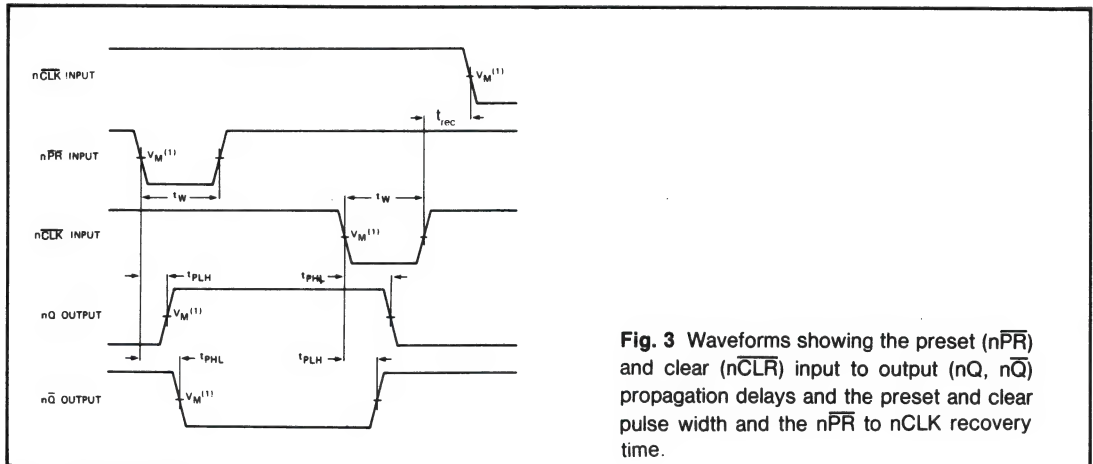
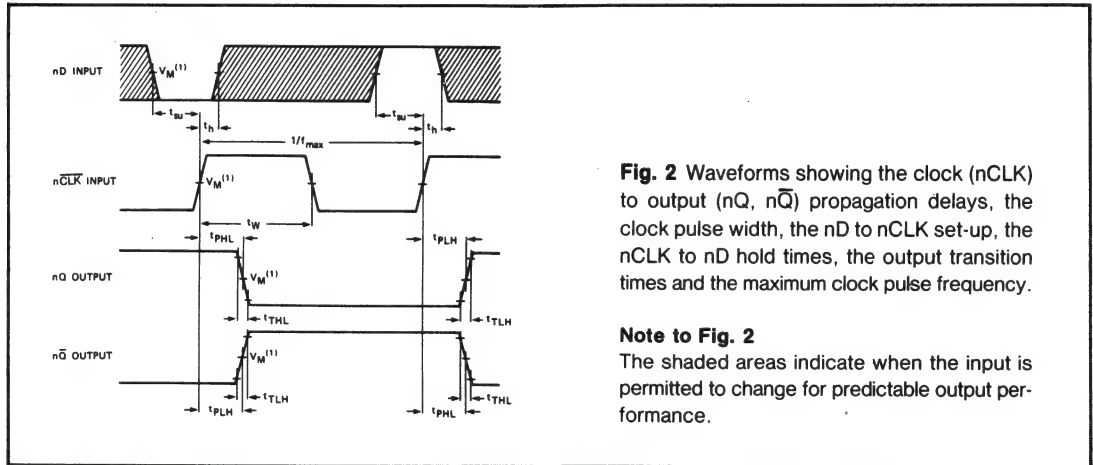
Timing Requirements for HCT: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER		V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HCT76		GD54HCT76		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_w	Pulse width	PR, CLR	4.5	18	10		20		25		ns
		CLK	4.5	16	10		20		25		ns
t_{su}	Set up Time	Data to CLK	4.5	15	10		18		20		ns
t_{rec}	Recovery time	PR, CLR to CLK	4.5	5	0		5		5		ns
t_h	Hold Time	CLK to Data	4.5	3	0		3		3		ns

AC Characteristics for HCT: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HCT76		GD54HCT76		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
f_{max}	Maximum Clock Pulse Frequency	4.5	27	54		22		18		MHz
t_{PLH} / t_{PHL}	Propagation Delay Time nCLK to nQ	4.5		17	30		40		50	ns
t_{PLH} / t_{PHL}	Propagation Delay Time nCLK to n \overline{Q}	4.5		17	30		40		50	ns
t_{PLH} / t_{PHL}	Propagation Delay Time n \overline{PR} to nQ, n \overline{Q}	4.5		15	28		38		45	ns
t_{PLH} / t_{PHL}	Propagation Delay time n \overline{CLR} to nQ, n \overline{Q}	4.5		15	28		38		45	ns
t_{TLH} / t_{THL}	Output Transition time	4.5		8	15		18		22	ns

AC Waveforms



Note to AC waveforms

- (1) HC : $V_M = 50\%$; $V_I = \text{GND to } V_{CC}$.
HCT : $V_M = 1.3V$; $V_I = \text{GND to } 3V$.

GD54/74HC85, GD54/74HCT85

4-BIT MAGNITUDE COMPARATOR

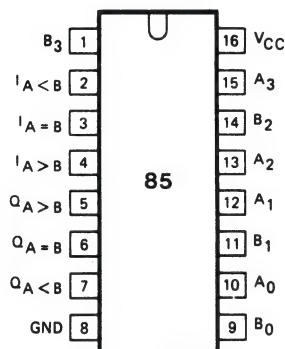
General Description

These devices are identical in pinout to the 54/74LS85. They are intended for HIGH speed comparison of two 4-bit words. The result of comparison is indicated by a high level on one of the decision outputs ($A > B$, $A = B$, $A < B$). By connecting the outputs of the least significant stage to the cascade inputs of the next stage, words of greater than 4-bits can be compared. These devices are characterized for operation over wide temperature ranges to meet industry and military specifications.

Features

- Low Power consumption characteristic of CMOS devices
- Output drive capability: 10 LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts
for HCT 4.5 to 5.5 volts
- Low input current: $1\mu\text{A}$ Max.
- Low quiescent current: $80\mu\text{A}$ Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs

Pin Configuration



Suffix-Blank : Plastic Dual In Line Package
 Suffix-J : Ceramic Dual In Line Package
 Suffix-D : Small Outline Package

Function Table

COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
A_3, B_3	A_2, B_2	A_1, B_1	A_0, B_0	$I_{A>B}$	$I_{A<B}$	$I_{A=B}$	$Q_{A>B}$	$Q_{A<B}$	$Q_{A=B}$
$A_3 > B_3$	X	X	X	X	X	X	H	L	L
$A_3 < B_3$	X	X	X	X	X	X	L	H	L
$A_3 = B_3$	$A_2 > B_2$	X	X	X	X	X	H	L	L
$A_3 = B_3$	$A_2 < B_2$	X	X	X	X	X	L	H	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 > B_1$	X	X	X	X	H	L	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 < B_1$	X	X	X	X	L	H	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 > B_0$	X	X	X	H	L	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 < B_0$	X	X	X	L	H	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	H	L	L	H	L	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	L	H	L	L	H	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	L	L	H	L	L	H
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	X	X	H	L	L	H
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	H	H	L	L	L	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	L	L	L	H	H	L

H=HIGH voltage level
 L=LOW voltage level
 X=don't care

Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC Supply voltage		-0.5	+7	V
$I_{IK} I_{OK}$	DC input or output diode current	for $V_I < -0.5$ or $V_I > V_{CC} + 0.5V$		20	mA
I_O	DC output source or sink current	for $-0.5V < V_O < V_{CC} + 0.5V$		25	mA
I_{CC}	DC V_{CC} or GND current			50	mA
T_{stg}	Storage temperature range		-65	150	°C
P_D	Power dissipation per package	above +70°C: derate linearly with 8mW/K		500	mW
T_L	Lead temperature	At distance $1/16 \pm 1/32$ in. from case for 60 sec(CERAMIC) 10 sec(PLASTIC)		300 260	°C

Recommended Operating Conditions

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range V_{CC} : GD54/74HC Types GD54/74HCT Types	2 4.5	6 5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A : GD74 Types GD54 Types	-40 -55	+85 +125	°C
Input Rise and Fall times t_r, t_f : GD54/74HC Types at 2V at 4.5V at 6V GD54/74HCT Types at 4.5V		1000 500 400 500	ns

Logic Diagram

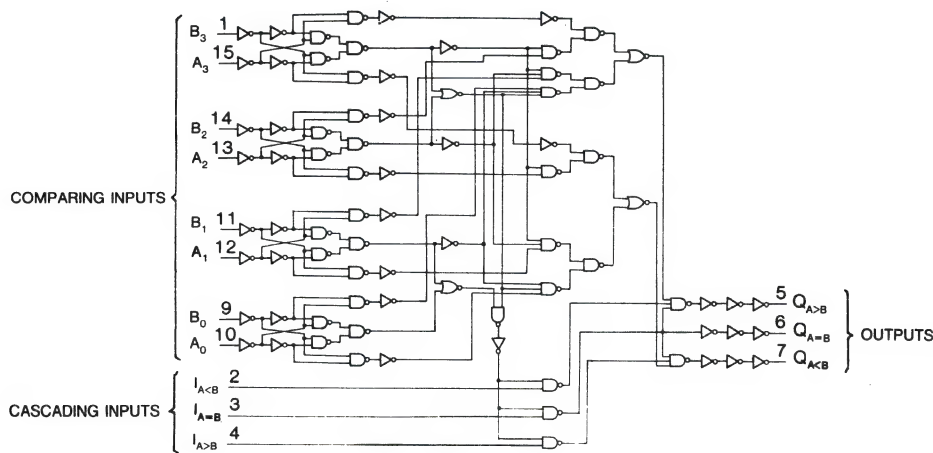


Fig. 1 Logic symbol

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HC85		GD54HC85		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2		1.5 3.15 4.2		V
V _{IL}	LOW level input voltage		2.0 4.5 6.0			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH} I _{OH} =-20μA	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V
		or V _{IL} I _{OH} =-4mA I _{OH} =-5.2mA	4.5 6.0	3.98 5.48	4.3 5.2		3.84 5.34		3.7 5.2		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH} I _{OL} =20μA	2.0 4.5 6.0			0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V
		or V _{IL} I _{OL} =4mA I _{OL} =5.2mA	4.5 6.0		0.17 0.15	0.26 0.26		0.33 0.33		0.4 0.4	
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	6.0			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	6.0			8		80		160	μA

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HCT85		GD54HCT85		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		4.5 to 5.5	2.0			2.0		2.0		V
V _{IL}	LOW level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH} I _{OH} =-20μA	4.5	4.4	4.5		4.4		4.4		V
		or V _{IL} I _{OH} =-4mA	4.5	3.98	4.3		3.84		3.7		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH} I _{OL} =20μA	4.5			0.1		0.1		0.1	V
		or V _{IL} I _{OL} =4mA	4.5		0.17	0.26		0.33		0.4	
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	5.5			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	5.5			8		80		160	μA

AC Characteristics for HC: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HC85		GD54HC85		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} / t_{PHL}	Propagation Delay Time A_n, B_n to $Q_{A>B}$ or $Q_{A<B}$	2.0 4.5 6.0		63 23 18	195 39 33		245 49 42		295 59 50	ns
t_{PLH} / t_{PHL}	Propagation Delay Time A_n, B_n to $Q_{A=B}$	2.0 4.5 6.0		50 18 14	175 35 30		220 44 37		265 53 45	ns
t_{PLH} / t_{PHL}	Propagation Delay Time $I_{A<B}, I_{A=B}, I_{A>B}$ to $Q_{A<B}, Q_{A>B}$	2.0 4.5 6.0		44 16 13	140 28 24		175 35 30		210 42 36	ns
t_{PLH} / t_{PHL}	Propagation Delay Time $I_{A=B}$ to $Q_{A=B}$	2.0 4.5 6.0		33 12 10	120 24 20		150 30 25		180 36 31	ns
t_{TLH} / t_{THL}	Output Transition Time	2.0 4.5 6.0		19 7 6	75 15 13		95 19 16		110 22 19	ns

AC Characteristics for HCT: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HCT85		GD54HCT85		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} / t_{PHL}	Propagation Delay Time A_n, B_n to $Q_{A>B}$ or $Q_{A<B}$	4.5		25	41		51		61	ns
t_{PLH} / t_{PHL}	Propagation Delay Time A_n, B_n to $Q_{A=B}$	4.5		20	38		48		57	ns
t_{PLH} / t_{PHL}	Propagation Delay Time $I_{A<B}, I_{A=B}, I_{A>B}$ to $Q_{A<B}, Q_{A>B}$	4.5		18	31		39		46	ns
t_{PLH} / t_{PHL}	Propagation Delay Time $I_{A=B}$ to $Q_{A=B}$	4.5		14	28		34		40	ns
t_{TLH} / t_{THL}	Output Transition Time	4.5		7	15		19		22	ns

AC Waveform

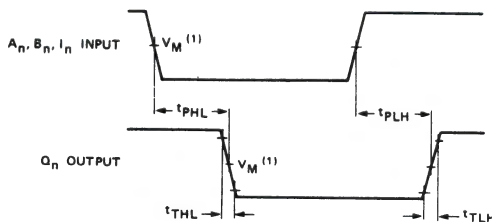


Fig. 2 Waveforms showing the word A inputs (A_n), word B inputs (B_n) and expansion inputs (I_n) to the outputs (Q_n) propagation delays and the output transition times.

Note to AC waveform

- (1) HC : $V_M=50\%$; $V_i=\text{GND to } V_{CC}$
HCT : $V_M=1.3\text{V}$; $V_i=\text{GND to } 3\text{V}$.

GD54/74HC86, GD54/74HCT86

QUAD 2- INPUT EXCLUSIVE OR GATES

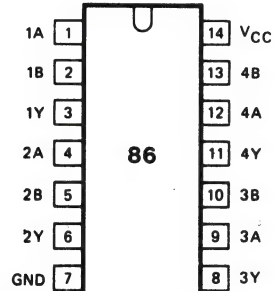
General Description

These devices are identical in pinout to the 54/74LS86. They contain four independent 2-input Exclusive OR gates. These devices are characterized for operation over wide temperature ranges to meet industry and military specifications.

Features

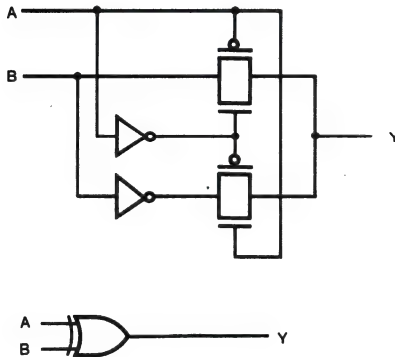
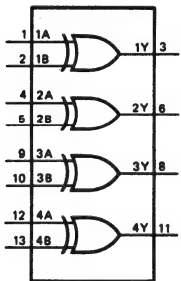
- Low Power consumption characteristic of CMOS devices
- Output drive capability: 10 LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts for HCT 4.5 to 5.5 volts
- Low input current: $1\mu\text{A}$ Max.
- Low quiescent current: $20\mu\text{A}$ Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs

Pin Configuration



Suffix-Blank : Plastic Dual In Line Package
 Suffix-J : Ceramic Dual In Line Package
 Suffix-D : Small Outline Package

Logic Symbol and Diagram



Function Table

INPUTS		OUTPUT
nA	nB	nY
L	L	L
L	H	H
H	L	H
H	H	L

H=HIGH voltage level
 L=LOW voltage level

Fig. 1 Logic symbol

Fig. 2 Logic diagram (one gate)

Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC Supply voltage		-0.5	+7	V
I_{IK}, I_{OK}	DC input or output diode current	for $V_I < -0.5$ or $V_I > V_{CC} + 0.5V$		20	mA
I_O	DC output source or sink current	for $-0.5V < V_O < V_{CC} + 0.5V$		25	mA
I_{CC}	DC V_{CC} or GND current			50	mA
T_{stg}	Storage temperature range		-65	150	°C
P_D	Power dissipation per package	above +70°C: derate linearly with 8mW/K		500	mW
T_L	Lead temperature	At distance 1/16±1/32 in. from case for 60 sec(CERAMIC) 10 sec(PLASTIC)		300 260	°C

Recommended Operating Conditions

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range V_{CC} : GD54/74HC Types GD54/74HCT Types	2 4.5	6 5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A : GD74 Types GD54 Types	-40 -55	+85 +125	°C
Input Rise and Fall times t_r, t_f : GD54/74HC Types at 2V at 4.5V at 6V GD54/74HCT Types at 4.5 V		1000 500 400 500	ns

Circuit Diagram

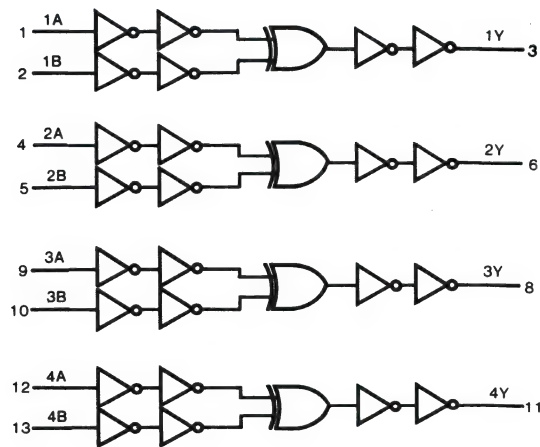


Fig. 3 Circuit diagram

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HC86		GD54HC86		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2		1.5 3.15 4.2		V
V _{IL}	LOW level input voltage		2.0 4.5 6.0			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH}	I _{OH} =-20μA	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0	1.9 4.4 5.9		1.9 4.4 5.9		V
			I _{OH} =-4mA	4.5 6.0	3.98 5.48	4.3 5.2	3.84 5.34		3.7 5.2		
		or V _{IL}	I _{OH} =-5.2mA	4.5 6.0	3.98 5.48	4.3 5.2	3.84 5.34		3.7 5.2		
			I _{OH} =-5.2mA	4.5 6.0	3.98 5.48	4.3 5.2	3.84 5.34		3.7 5.2		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH}	I _{OL} =20μA	2.0 4.5 6.0			0.1 0.1 0.1	0.1 0.1 0.1		0.1 0.1 0.1	V
			I _{OL} =4mA	4.5 6.0		0.17 0.15	0.26 0.26	0.33 0.33		0.4 0.4	
		or V _{IL}	I _{OL} =4mA	4.5 6.0		0.17 0.15	0.26 0.26	0.33 0.33		0.4 0.4	
			I _{OL} =5.2mA	4.5 6.0		0.17 0.15	0.26 0.26	0.33 0.33		0.4 0.4	
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	6.0			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	6.0			2		20		40	μA

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HCT86		GD54HCT86		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		4.5 to 5.5	2.0			2.0		2.0		V
V _{IL}	LOW level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH}	I _{OH} =-20μA	4.5	4.4	4.5	4.4		4.4		V
		or V _{IL}	I _{OH} =-4mA	4.5	3.98	4.3	3.84		3.7		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH}	I _{OL} =20μA	4.5			0.1	0.1		0.1	V
		or V _{IL}	I _{OL} =4mA	4.5		0.17	0.26	0.33		0.4	
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	5.5			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	5.5			2		20		40	μA

AC Characteristics for HC: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^{\circ}\text{C}$			GD74HC86		GD54HC86		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
$t_{PLH}/$ t_{PHL}	Propagation delay time nA, nB to nY	2.0 4.5 6.0		36 11 9	65 21 19		85 28 24		100 29 27	ns
$t_{TLH}/$ t_{THL}	Output transition time	2.0 4.5 6.0		19 7 6	75 15 13		95 19 16		110 22 19	ns

AC Characteristics for HCT: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^{\circ}\text{C}$			GD74HCT86		GD54HCT86		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
$t_{PLH}/$ t_{PHL}	Propagation delay time nA, nB, to nY	4.5		14	28		36		44	ns
$t_{TLH}/$ t_{THL}	Output transition time	4.5		7	15		19		22	ns

AC Waveform

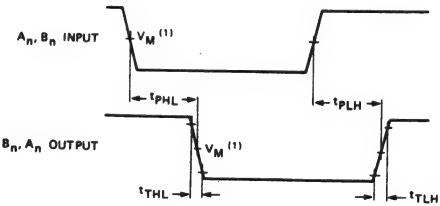


Fig. 4 Waveforms showing the input (nA, nB) to output (nY) propagation delays and the output transition times.

Note to AC waveforms

- (1) HC : $V_M=50\%$; $V_I=GND$ to V_{CC} .
- HCT : $V_M=1.3V$; $V_I=GND$ to $3V$.

GD54/74HC93, GD54/74HCT93

4-BIT BINARY RIPPLE COUNTER

General Description

These devices are identical in pinout to the 54/74LS93. Each circuit contains a 4-bit ripple counter consisting of four master/slave flip-flops that are internally connected to provide separate divide-by-two (Q_0 output) and divide-by-eight (Q_1 , Q_2 , & Q_3 outputs) sections. Each section has a separate clock input which initiates state changes of the counter on the negative edge of clock transition. A gated and asynchronous reset is provided which resets all the flip-flops. Because Q_0 is not internally connected to the succeeding stages, the devices may be operated in a 3-bit or 4-bit ripple counter. These devices are characterized for operation over wide temperature ranges to meet industry and military specifications.

Features

- Low Power consumption characteristic of CMOS devices
- Output drive capability: 10 LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts
for HCT 4.5 to 5.5 volts
- Low input current: $1\mu\text{A}$ Max.
- Low quiescent current: $80\mu\text{A}$ Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs

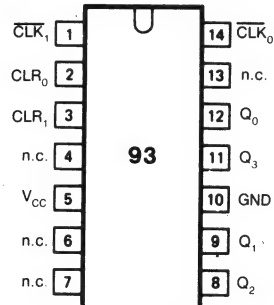
Mode Selection

RESET INPUTS		OUTPUTS			
CLR ₀	CLR ₁	Q ₀	Q ₁	Q ₂	Q ₃
H	H	L	L	L	L
L	H	count			
H	L	count			
L	L	count			

Note to function table
Output Q_0 connected to $\overline{\text{CLK}}_1$.

H=HIGH voltage level
L=LOW voltage level

Pin Configuration



Suffix-Blank : Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package
Suffix-D : Small Outline Package

Count Sequence

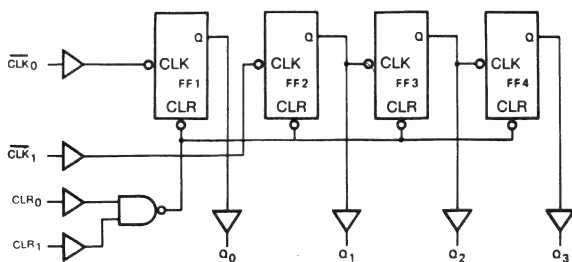
COUNT	OUTPUTS			
	Q ₀	Q ₁	Q ₂	Q ₃
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
10	L	H	L	H
11	H	H	L	H
12	L	L	H	H
13	H	L	H	H
14	L	H	H	H
15	H	H	H	H

Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC Supply voltage		-0.5	+7	V
I_{IK}, I_{OK}	DC input or output diode current	for $V_I < -0.5$ or $V_I > V_{CC} + 0.5V$		20	mA
I_O	DC output source or sink current	for $-0.5V < V_O < V_{CC} + 0.5V$		25	mA
I_{CC}	DC V_{CC} or GND current			50	mA
T_{stg}	Storage temperature range		-65	150	°C
P_D	Power dissipation per package	above +70°C: derate linearly with 8mW/K		500	mW
T_L	Lead temperature	At distance $1/16 \pm 1/32$ in. from case for 60 sec(CERAMIC) 10 sec(PLASTIC)		300 260	°C

Recommended Operating Conditions

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range V_{CC} : GD54/74HC Types GD54/74HCT Types	2 4.5	6 5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A : GD74 Types GD54 Types	-40 -55	+85 +125	°C
Input Rise and Fall times t_r, t_f : GD54/74HC Types at 2V at 4.5V at 6V GD54/74HCT Types at 4.5 V		1000 500 400 500	ns

Logic Diagram**Fig. 1** Logic diagram

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION	V_{CC} (V)	$T_A=25^{\circ}\text{C}$			GD74HC93		GD54HC93		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V_{IH}	HIGH level input Voltage		2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2		1.5 3.15 4.2		V
V_{IL}	LOW level input voltage		2.0 4.5 6.0			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V
V_{OH}	HIGH level output voltage	$V_{IN}=V_{IH}$	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V
		$I_{OH}=-20\mu\text{A}$									
		or V_{IL}									
V_{OL}	LOW level output voltage	$V_{IN}=V_{IH}$	2.0 4.5 6.0			0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V
		$I_{OL}=20\mu\text{A}$									
		or V_{IL}									
I_{IN}	Input leakage Current	$V_{IN}=V_{CC}$ or GND	6.0			0.1		1.0		1.0	μA
		$I_{OH}=-4\text{mA}$	4.5 6.0	3.98 5.48	4.3 5.2		3.84 5.34		3.7 5.2		
		$I_{OL}=5.2\text{mA}$									
I_{CC}	Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{out}=0\mu\text{A}$	6.0			8		80		160	μA

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION	V_{CC} (V)	$T_A=25^{\circ}\text{C}$			GD74HCT93		GD54HCT93		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V_{IH}	HIGH level input Voltage		4.5 to 5.5	2.0			2.0		2.0		V
V_{IL}	LOW level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V_{OH}	HIGH level output voltage	$V_{IN}=V_{IH}$	4.5	4.4	4.5		4.4		4.4		V
		$I_{OH}=-20\mu\text{A}$									
		or V_{IL}									
V_{OL}	LOW level output voltage	$V_{IN}=V_{IH}$	4.5			0.1		0.1		0.1	V
		$I_{OL}=20\mu\text{A}$									
		or V_{IL}									
I_{IN}	Input leakage Current	$V_{IN}=V_{CC}$ or GND	5.5			0.1		1.0		1.0	μA
		$I_{OH}=-4\text{mA}$	4.5 6.0	3.98 5.48	4.3 5.2		3.84 5.34		3.7 5.2		
		$I_{OL}=5.2\text{mA}$									
I_{CC}	Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{out}=0\mu\text{A}$	5.5			8		80		160	μA

Timing Requirements for HC: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER		V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HC93		GD54HC93		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_w	Pulse width	$\overline{\text{CLK}}_n, \text{CLR}_n$	2.0	80			100		120		ns
			4.5	16			20		24		
			6.0	14			17		20		
t_{su}	Recovery time	CLR_n to $\overline{\text{CLK}}_n$	2.0	50			65		75		ns
			4.5	10			13		15		
			6.0	9			11		13		

AC Characteristics for HC: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER		V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HC93		GD54HC93		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
f_{max}	Maximum Clock Pulse Frequency		2.0	6			4.8		4.0		MHz
			4.5	31			25		21		
			6.0	36			29		25		
$t_{\text{PLH}}/$ t_{PHL}	Propagation Delay Time $\overline{\text{CLK}}_0$ to Q_0		2.0		41	125		155		190	ns
			4.5		15	25		31		38	
			6.0		12	21		26		32	
$t_{\text{PLH}}/$ t_{PHL}	Propagation Delay Time $\overline{\text{CLK}}_1$ to Q_1		2.0		49	135		170		205	ns
			4.5		16	27		34		41	
			6.0		13	23		29		35	
$t_{\text{PLH}}/$ t_{PHL}	Propagation Delay Time $\overline{\text{CLK}}_1$ to Q_2		2.0		61	185		230		280	ns
			4.5		22	37		46		56	
			6.0		18	31		39		48	
$t_{\text{PLH}}/$ t_{PHL}	Propagation Delay Time $\overline{\text{CLK}}_1$ to Q_3		2.0		89	245		305		370	ns
			4.5		29	49		61		71	
			6.0		23	42		52		63	
t_{PHL}	Propagation Delay Time CLR_n to Q_n		2.0		50	155		195		235	ns
			4.5		18	31		39		47	
			6.0		14	26		33		40	
$t_{\text{TLH}}/$ t_{THL}	Output Transition Time		2.0		29	75		95		110	ns
			4.5		7	15		19		22	
			6.0		6	13		16		19	

Timing Requirements for HCT: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER		V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HCT93		GD54HCT93		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
f_{clock}	Pulse width	$\overline{\text{CLK}}_n, \text{CLR}_n$	4.5	16			20		24		ns
t_{su}	Recovery time	CLR_n to $\overline{\text{CLK}}_n$	4.5	10			13		15		ns

AC Characteristics for HCT: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HCT93		GD54HCT93		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
f_{max}	Maximum Clock Pulse Frequency	4.5	30			24		20		MHz
$t_{\text{PLH}}/$ t_{PHL}	Propagation Delay Time $\overline{\text{CLK}}_0$ to Q_0	4.5		18	34		43		51	ns
$t_{\text{PLH}}/$ t_{PHL}	Propagation Delay Time $\overline{\text{CLK}}_1$ to Q_1	4.5		18	34		43		51	ns
$t_{\text{PLH}}/$ t_{PHL}	Propagation Delay Time $\overline{\text{CLK}}_1$ to Q_2	4.5		24	46		58		69	ns
$t_{\text{PLH}}/$ t_{PHL}	Propagation Delay Time $\overline{\text{CLK}}_1$ to Q_3	4.5		30	58		73		87	ns
t_{PHL}	Propagation Delay Time CLR_n to Q_n	4.5		17	33		41		50	ns
$t_{\text{TLH}}/$ t_{THL}	Output Transition Time	4.5		7	15		19		22	ns

AC Waveforms

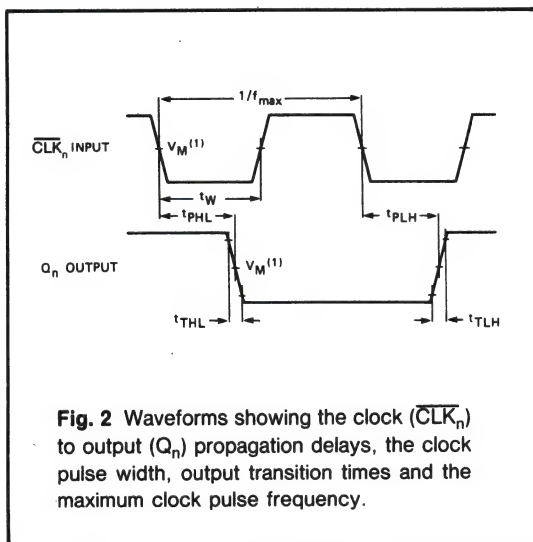


Fig. 2 Waveforms showing the clock ($\overline{\text{CLK}}_n$) to output (Q_n) propagation delays, the clock pulse width, output transition times and the maximum clock pulse frequency.

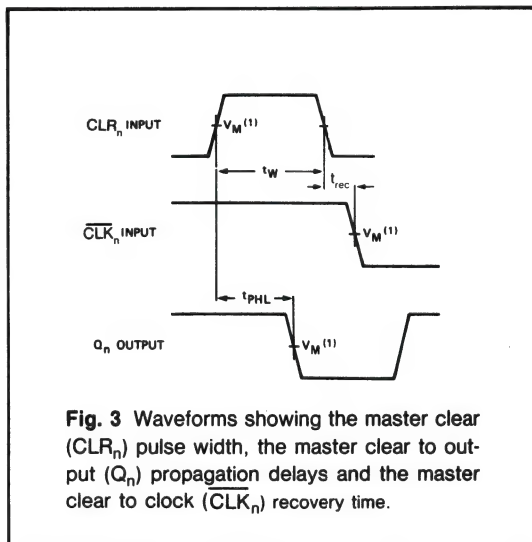


Fig. 3 Waveforms showing the master clear (CLR_n) pulse width, the master clear to output (Q_n) propagation delays and the master clear to clock ($\overline{\text{CLK}}_n$) recovery time.

Note to AC waveform

(1) HC: $V_M = 50\% \cdot V_I = \text{GND to } V_{\text{CC}}$.

HCT: $V_M = 1.3 \cdot V_I = \text{GND to } 3\text{V}$.

GD54/74HC107, GD54/74HCT107

DUAL J-K FLIP-FLOPS WITH CLEAR

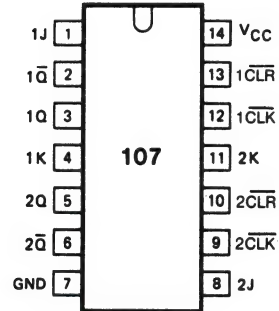
General Description

These devices are identical in pinout to the 54/74LS107. They consist of two J-K flip-flops with individual J, K, clock, and clear inputs. These flip-flops are edge sensitive to the clock input and change state on the negative going transition of the clock pulse. Both Q and \bar{Q} outputs are available from each flip-flop clear is independent of the clock and accomplished by a low on the input. These devices are characterized for operation over wide temperature ranges to meet industry and military specifications.

Features

- Low Power consumption characteristic of CMOS devices
- Output drive capability: 10 LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts
for HCT 4.5 to 5.5 volts
- Low input current: $1\mu\text{A}$ Max.
- Low quiescent current: $40\mu\text{A}$ Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs

Pin Configuration



Suffix-Blank : Plastic Dual In Line Package
 Suffix-J : Ceramic Dual In Line Package
 Suffix-D : Small Outline Package

Function Table

OPERATING MODE	INPUTS				OUTPUTS	
	$\bar{n}\text{CLR}$	$\bar{n}\text{CLK}$	J	K	Q	\bar{Q}
asynchronous reset	L	X	X	X	L	H
toggle	H	\downarrow	h	h	q	\bar{q}
load "0" (reset)	H	\downarrow	l	h	L	H
load "1" (set)	H	\downarrow	h	l	H	L
hold "no change"	H	\downarrow	l	l	q	\bar{q}

H = HIGH voltage level
 \bar{h} = HIGH voltage level one set-up time prior to the LOW-to-HIGH CLK transition
 L = LOW voltage level
 \bar{l} = LOW voltage level one set-up time prior to the LOW-to-HIGH CLK transition
 q = lower case letters indicate the state of the referenced output one set-up time prior to the LOW-to-HIGH CLK transition
 X = don't care
 \downarrow = HIGH-to-LOW CLK transition

Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC Supply voltage		-0.5	+7	V
$I_{IK} I_{OK}$	DC input or output diode current	for $V_I < -0.5$ or $V_I > V_{CC} + 0.5V$		20	mA
I_O	DC output source or sink current	for $-0.5V < V_O < V_{CC} + 0.5V$		25	mA
I_{CC}	DC V_{CC} or GND current			50	mA
T_{stq}	Storage temperature range		-65	150	°C
P_D	Power dissipation per package	above +70°C: derate linearly with 8mW/K		500	mW
T_L	Lead temperature	At distance 1.16 ± 1/32 in. from case for 60 sec(CERAMIC) 10 sec(PLASTIC)		300 260	°C

Recommended Operating Conditions

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range V_{CC} : GD54/74HC Types GD54/74HCT Types	2 4.5	6 5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A : GD74 Types GD54 Types	-40 -55	+85 +125	°C
Input Rise and Fall times t_r, t_f : GD54/74HC Types at 2V at 4.5V at 6V GD54/74HCT Types at 4.5V		1000 500 400 500	ns

Logic Diagram

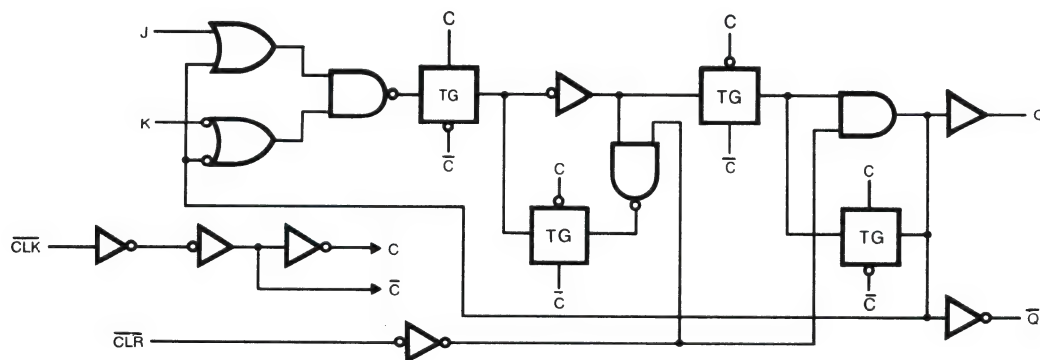


Fig. 1 Logic diagram (one flip flop)

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION		V _{CC} (V)	T _A =25°C			GD74HC107		GD54HC107		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage			2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2		1.5 3.15 4.2		V
V _{IL}	LOW level input voltage			2.0 4.5 6.0			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH}	I _{OH} = -20μA	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V
			I _{OH} = -4mA I _{OH} = -5.2mA	4.5 6.0	3.98 5.48	4.3 5.2		3.84 5.34		3.7 5.2		
		or V _{IL}	I _{OL} =20μA	2.0 4.5 6.0			0.1 0.1 0.1	0.1 0.1 0.1		0.1 0.1 0.1		
			I _{OL} =4mA I _{OL} =5.2mA	4.5 6.0		0.17 0.15	0.26 0.26	0.33 0.33		0.4 0.4		
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND		6.0			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA		6.0			4		40		80	μA

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION		V _{CC} (V)	T _A =25°C			GD74HCT107		GD54HCT107		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage			4.5 to 5.5	2.0			2.0		2.0		V
V _{IL}	LOW level input voltage			4.5 to 5.5			0.8		0.8		0.8	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH}	I _{OH} = -20μA	4.5	4.4	4.5		4.4		4.4		V
		or V _{IL}	I _{OH} = -4mA	4.5	3.98	4.3		3.84		3.7		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH}	I _{OL} =20μA	4.5			0.1		0.1		0.1	V
		or V _{IL}	I _{OL} =4mA	4.5		0.17	0.26		0.33		0.4	
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND		5.5			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA		5.5			4		40		80	μA

Timing Requirements for HC: $t_r = t_f = 6\text{ns}$ $C_L = 50\text{ pF}$

SYMBOL	PARAMETER		V_{CC} (V)	$T_A = 25^\circ\text{C}$			GD74HC107		GD54HC107		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_w	Pulse width	$\overline{\text{CLR}}$ (low)	2.0	80	30		100		120		ns
			4.5	16	10		20		25		
			6.0	14	8		18		22		
		$\overline{\text{CLK}}$ (high or low)	2.0	80	30		100		120		ns
			4.5	16	10		20		25		
			6.0	14	8		18		22		
t_{su}	Set up Time	Data to $\overline{\text{CLK}}$ †	2.0	60	30		80		100		ns
			4.5	15	10		18		20		
			6.0	14	8		16		18		
t_{rec}	Recovery time	$\overline{\text{CLR}}$ to $\overline{\text{CLK}}$	2.0	5	0		5		5		ns
			4.5	5	0		5		5		
			6.0	5	0		5		5		
t_h	Hold Time	Data to $\overline{\text{CLK}}$ †	2.0	3	0		3		3		ns
			4.5	3	0		3		3		
			6.0	3	0		3		3		

AC Characteristics for HC: $t_r = t_f = 6\text{ns}$ $C_L = 50\text{ pF}$

SYMBOL	PARAMETER		V_{CC} (V)	$T_A = 25^\circ\text{C}$			GD54HC107		GD74HC107		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
f_{max}	Maximum Clock Pulse Frequency		2.0	6	20		5		4		MHz
			4.5	30	65		25		20		
			6.0	35	75		30		25		
$t_{PLH} /$ t_{PHL}	Propagation Delay Time $n\overline{\text{CLK}}$ to nQ		2.0		46	160		200		240	ns
			4.5		15	30		40		50	
			6.0		14	28		35		45	
$t_{PLH} /$ t_{PHL}	Propagation Delay Time $n\overline{\text{CLK}}$ to $n\overline{Q}$		2.0		50	160		200		240	ns
			4.5		17	30		40		50	
			6.0		16	28		35		45	
$t_{PLH} /$ t_{PHL}	Propagation Delay time $n\overline{\text{CLR}}$ to nQ , $n\overline{Q}$		2.0		45	155		190		230	ns
			4.5		15	28		38		45	
			6.8		14	26		34		40	
$t_{TLH} /$ t_{THL}	Output Transition time		2.0		25	70		85		100	ns
			4.5		8	15		18		22	
			6.0		7	13		16		19	

Timing Requirements for HCT: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER		V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HCT107		GD54HCT107		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_w	Pulse width	$\overline{\text{CLR}}$ (low)	4.5	18	10		20		25		ns
		$\overline{\text{CLK}}$ (high or low)	4.5	10	10		20		25		ns
t_{su}	Set up Time	Data to $\overline{\text{CLK}}\uparrow$	4.5	15	10		15		20		ns
t_{rec}	Recovery time	$\overline{\text{CLR}}$ to $\overline{\text{CLK}}$	4.5	5	0		5		5		ns
t_h	Hold Time	Data to $\overline{\text{CLK}}\uparrow$	4.5	3	0		3		3		ns

AC Characteristics for HCT: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HCT107		GD54HCT107		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
f_{max}	Maximum Clock Pulse Frequency	4.5	27	54		22		18		MHz
t_{PLH} / t_{PHL}	Propagation Delay Time $n\overline{\text{CLK}}$ to nQ	4.5		17	30		40		50	ns
t_{PLH} / t_{PHL}	Propagation Delay Time $n\overline{\text{CLK}}$ to $n\overline{Q}$	4.5		17	30		40		50	ns
t_{PLH} / t_{PHL}	Propagation Delay Time $n\overline{\text{CLR}}$ to nQ , $n\overline{Q}$	4.5		15	28		38		45	ns
t_{TLH} / t_{THL}	Output Transition Time	4.5		8	15		18		22	ns

AC Waveforms

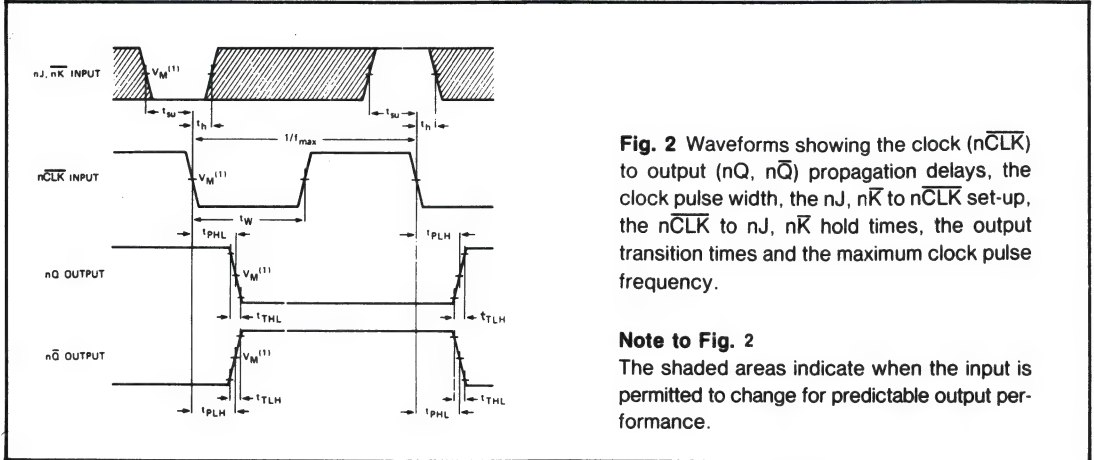


Fig. 2 Waveforms showing the clock ($n\bar{CLK}$) to output (nQ , $n\bar{Q}$) propagation delays, the clock pulse width, the nJ , $n\bar{K}$ to $n\bar{CLK}$ set-up, the $n\bar{CLK}$ to nJ , $n\bar{K}$ hold times, the output transition times and the maximum clock pulse frequency.

Note to Fig. 2

The shaded areas indicate when the input is permitted to change for predictable output performance.

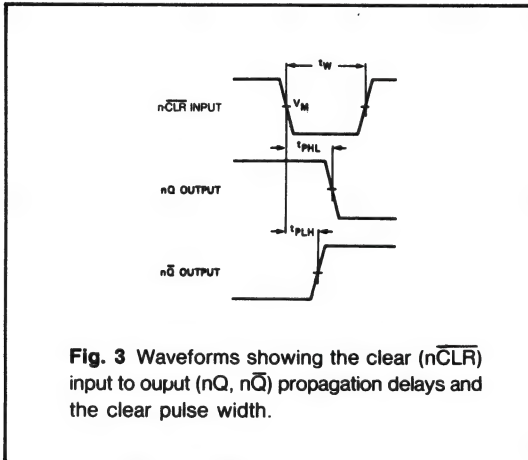


Fig. 3 Waveforms showing the clear ($n\bar{CLR}$) input to output (nQ , $n\bar{Q}$) propagation delays and the clear pulse width.

Note to AC waveforms

- (1) HC : $V_M=50\%$; $V_I=GND$ to V_{CC} .
HCT : $V_M=1.3V$; $V_I=GND$ to $3V$.

GD54/74HC109, GD54/74HCT109

DUAL J- \bar{K} FLIP-FLOPS WITH PRESET & CLEAR

General Description

These devices are identical in pinout to the 54/74LS109. They consist of two J- \bar{K} flip-flops with individual J, K, Clock, Preset, and Clear inputs. These flip-flops are edge sensitive to the clock input and change state on the negative going transition of the clock pulse. Both Q and \bar{Q} outputs are available from each flip-flop. Preset and Clear is independent of the clock and accomplished by a Low level on the corresponding input. These devices are characterized for operation over wide temperature ranges to meet industry and military specifications

Features

- Low Power consumption characteristic of CMOS devices
- Output drive capability: 10 LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts
for HCT 4.5 to 5.5 volts
- Low input current: 1 μ A Max.
- Low quiescent current: 40 μ A Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs

Logic Symbol

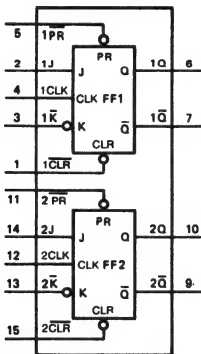
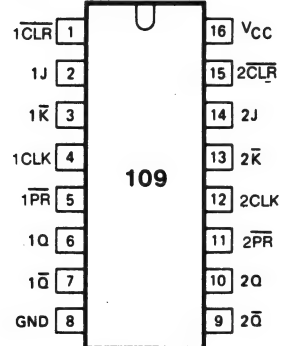


Fig. 1 Logic symbol

Pin Configuration



Suffix-Blank : Plastic Dual In Line Package
 Suffix-J : Ceramic Dual In Line Package
 Suffix-D : Small Outline Package

Function Table

INPUTS					OUTPUTS	
nPR	nCLR	nCLK	nJ	nK	nQ	nQ $\bar{}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H \dagger	H \dagger
H	H	\uparrow	L	L	L	H
H	H	\uparrow	H	L	TOGGLE	TOGGLE
H	H	\uparrow	L	H	Q $_0$	H $_0$
H	H	\uparrow	H	H	H	L
H	H	L	X	X	Q $_0$	Q $_0$

\dagger The output levels in this configuration are not guaranteed to meet the minimum levels for V $_{OH}$ if the lows at preset and clear are near V $_{IL}$ maximum. Furthermore this configuration is nonstable; that is, it will not persist when preset or clear return to their inactive (high) level.

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HC109		GD54HC109		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2		1.5 3.15 4.2		V
V _{IL}	LOW level input voltage		2.0 4.5 6.0			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH}	I _{OH} =-20μA	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0	1.9 4.4 5.9		1.9 4.4 5.9		V
			I _{OH} =-4mA	4.5 6.0	3.98 5.48	4.3 5.2	3.84 5.34		3.7 5.2		
		or V _{IL}	I _{OH} =-5.2mA	4.5 6.0	3.98 5.48	4.3 5.2	3.84 5.34		3.7 5.2		
			I _{OH} =-5.2mA	4.5 6.0	3.98 5.48	4.3 5.2	3.84 5.34		3.7 5.2		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH}	I _{OL} =20μA	2.0 4.5 6.0			0.1 0.1 0.1	0.1 0.1 0.1		0.1 0.1 0.1	V
			I _{OL} =4mA	4.5 6.0		0.17 0.15	0.26 0.26	0.33 0.33		0.4 0.4	
		or V _{IL}	I _{OL} =4mA	4.5 6.0		0.17 0.15	0.26 0.26	0.33 0.33		0.4 0.4	
			I _{OL} =5.2mA	4.5 6.0		0.17 0.15	0.26 0.26	0.33 0.33		0.4 0.4	
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	6.0			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	6.0			4		40		80	μA

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HCT109		GD54HCT109		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		4.5 to 5.5	2.0			2.0		2.0		V
V _{IL}	LOW level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH}	I _{OH} =-20μA	4.5	4.4	4.5	4.4		4.4		V
		or V _{IL}	I _{OH} =-4mA	4.5	3.98	4.3	3.84		3.7		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH}	I _{OL} =20μA	4.5			0.1	0.1		0.1	V
		or V _{IL}	I _{OL} =4mA	4.5		0.17	0.26	0.33		0.4	
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	5.5			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	5.5			4		40		80	μA

Timing Requirements for HC: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER		V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HC109		GD54HC109		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_w	Pulse width	$\overline{\text{PR}}, \overline{\text{CLR}}$	2.0	80	30		100		120		ns
			4.5	16	10		20		25		
			6.0	14	8		18		22		
		CLK	2.0	80	30		100		120		ns
			4.5	16	10		20		25		
			6.0	14	8		18		22		
t_{su}	Set up Time	Data to CLK	2.0	60	30		80		100		ns
			4.5	15	10		18		20		
			6.0	14	8		16		18		
t_{rec}	Recovery time	$\overline{\text{PR}}, \overline{\text{CLR}}$ to CLK	2.0	5	0		5		5		ns
			4.5	5	0		5		5		
			6.0	5	0		5		5		
t_h	Hold Time	CLK to Data	2.0	3	0		3		3		ns
			4.5	3	0		3		3		
			6.0	3	0		3		3		

AC Characteristics for HC: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER		V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HC109		GD54HC109		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
f_{max}	Maximum Clock Pulse Frequency		2.0	6	20		5		4		MHz
			4.5	30	65		25		20		
			6.0	35	75		30		25		
t_{PLH} / t_{PHL}	Propagation Delay Time nCLK to nQ		2.0		46	160		200		240	ns
			4.5		15	30		40		50	
			6.0		14	28		35		45	
t_{PLH} / t_{PHL}	Propagation Delay Time nCLK to n $\overline{\text{Q}}$		2.0		50	160		200		240	ns
			4.5		17	30		40		50	
			6.0		16	28		35		45	
t_{PLH} / t_{PHL}	Propagation Delay Time n $\overline{\text{PR}}$ to nQ, n $\overline{\text{Q}}$		2.0		45	155		190		230	ns
			4.5		15	28		38		45	
			6.0		14	26		34		42	
t_{PLH} / t_{PHL}	Propagation Delay time n $\overline{\text{CLR}}$ to nQ, n $\overline{\text{Q}}$		2.0		45	155		190		230	ns
			4.5		15	28		38		45	
			6.8		14	26		34		42	
t_{TLH} / t_{THL}	Output Transition time		2.0		25	70		85		100	ns
			4.5		8	15		18		22	
			6.0		7	13		16		19	

Timing Requirements for HCT: $t_r = t_f = 6\text{ns}$ $C_L = 50\text{ pF}$

SYMBOL	PARAMETER		V_{CC} (V)	$T_A = 25^\circ\text{C}$			GD74HCT109		GD54HCT109		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_w	Pulse width	$\overline{PR}, \overline{CLR}$	4.5	18	10		20		25		ns
		CLK	4.5	16	10		20		25		ns
t_{su}	Set up Time	Data to CLK	4.5	15	10		18		20		ns
t_{rec}	Recovery time	$\overline{PR}, \overline{CLR}$ to CLK	4.5	5	0		5		5		ns
t_h	Hold Time	CLK to Data	4.5	3	0		3		3		ns

AC Characteristics for HCT: $t_r = t_f = 6\text{ns}$ $C_L = 50\text{ pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A = 25^\circ\text{C}$			GD74HCT109		GD54HCT109		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
f_{max}	Maximum clock Pulse frequency	4.5	27	54		22		18		MHz
$t_{PLH} /$ t_{PHL}	Propagation Delay time $n\text{CLK}$ to nQ	4.5		17	30		40		50	ns
$t_{PLH} /$ t_{PHL}	Propagation Delay time $n\text{CLK}$ to $n\overline{Q}$	4.5		17	30		40		50	ns
$t_{PLH} /$ t_{PHL}	Propagation Delay time $n\overline{PR}$ to nQ , $n\overline{Q}$	4.5		15	28		38		45	ns
$t_{PLH} /$ t_{PHL}	Propagation Delay time $n\overline{CLR}$ to nQ , $n\overline{Q}$	4.5		15	28		38		45	ns
$t_{TLH} /$ t_{THL}	Output Transition time	4.5		8	15		18		22	ns

AC Waveforms

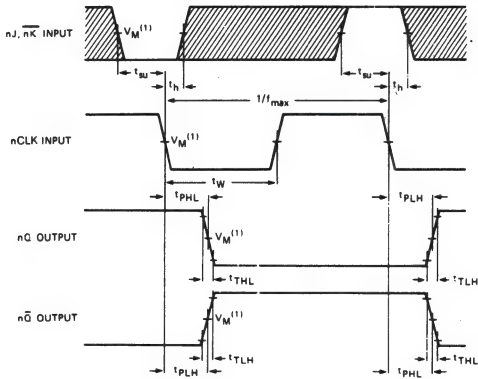


Fig. 3 Waveforms showing the clock (nCLK) to output (nQ, n \bar{Q}) propagation delays, the clock pulse width, the nJ, n \bar{K} to nCLK set-up, the nCLK to nJ, n \bar{K} hold times, the output transition times and the maximum clock pulse frequency.

Note to Fig. 3

The shaded areas indicate when the input is permitted to change for predictable output performance.

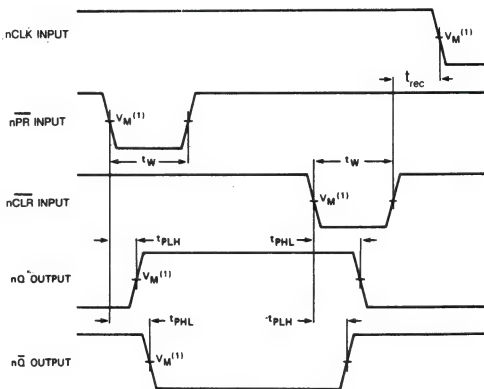


Fig. 4 Waveforms showing the preset and clear input to output (nQ, n \bar{Q}) propagation delays and the preset and clear pulse width.

Note to AC waveforms

(1) HC : $V_M = 50\%$; $V_I = \text{GND to } V_{CC}$
 HCT : $V_M = 1.3V$; $V_I = \text{GND to } 3V$.

GD54/74HC112, GD54/74HCT112

DUAL J-K FLIP-FLOPS WITH PRESET & CLEAR

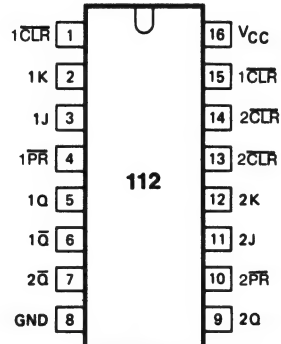
General Description

These devices are identical in pinout to the 54/74LS112. They consist of two J-K flip-flops with individual J, K, CLOCK, PRESET, and CLEAR inputs. These flip-flops are edge sensitive to the clock input and change state on the negative going transition of the clock pulse. Both Q and \bar{Q} outputs are available from each flip-flop. PRESET and CLEAR is independent of the clock and accomplished by a LOW level on the corresponding input. These devices are characterized for operation over wide temperature ranges to meet industry and military specifications

Features

- Low Power consumption characteristic of CMOS devices
- Output drive capability: 10 LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts
for HCT 4.5 to 5.5 volts
- Low input current: 1 μ A Max.
- Low quiescent current: 40 μ A Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs

Pin Configuration



Suffix-Blank : Plastic Dual In Line Package
 Suffix-J : Ceramic Dual In Line Package
 Suffix-D : Small Outline Package

Function Table

OPERATING MODE	INPUTS					OUTPUTS	
	nPR	nCLR	nCLK	nJ	nK	nQ	nQ-bar
asynchronous set	L	H	X	X	X	H	L
asynchronous reset	H	L	X	X	X	L	H
undetermined	L	L	X	X	X	H	H
toggle	H	H	↓	h	h	q-bar	q
load "0" (reset)	H	H	↓	l	h	L	H
load "1" (set)	H	H	↓	h	l	H	L
hold "no change"	H	H	↓	l	l	q	q-bar

Note to function table

Both outputs will be HIGH while both nPR and nCLR are LOW, but the output states are unpredictable if nPR and nCLR go HIGH simultaneously

H = HIGH voltage level

h = HIGH voltage level one set-up time prior to the HIGH-to-LOW CLK transition.

L = LOW voltage level

l = LOW voltage level one set-up time prior to the HIGH-to-LOW CLK transition

q = lower case letters indicate the state of the referenced output one set up time prior to the HIGH-to-LOW CLK transition

X = don't care

↓ = HIGH-to-LOW CLK transition

Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC Supply voltage		-0.5	+7	V
I_{IK}, I_{OK}	DC input or output diode current	for $V_I < -0.5$ or $V_I > V_{CC} + 0.5V$		20	mA
I_O	DC output source or sink current	for $-0.5V < V_O < V_{CC} + 0.5V$		25	mA
I_{CC}	DC V_{CC} or GND current			50	mA
T_{stg}	Storage temperature range		-65	150	°C
P_D	Power dissipation per package	above +70°C: derate linearly with 8mW/K		500	mW
T_L	Lead temperature	At distance $1/16 \pm 1/32$ in. from case for 60 sec(CERAMIC) 10 sec(PLASTIC)		300 260	°C

Recommended Operating Conditions

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range V_{CC} : GD54/74HC Types GD54/74HCT Types	2 4.5	6 5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A : GD74 Types GD54 Types	-40 -55	+85 +125	°C
Input Rise and Fall times t_r, t_f : GD54/74HC Types at 2V at 4.5V at 6V GD54/74HCT Types at 4.5V		1000 500 400 500	ns

Logic Diagram

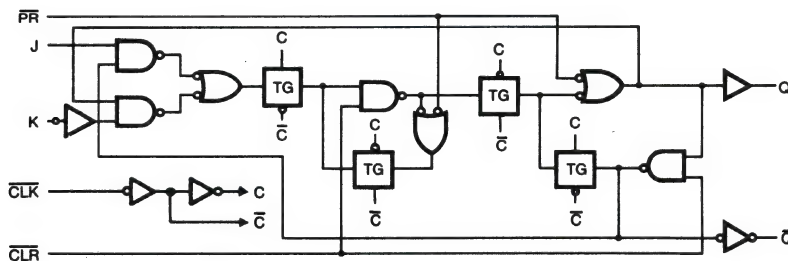


Fig. 2 logic diagram

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HC112		GD54HC112		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2		1.5 3.15 4.2		V
V _{IL}	LOW level input voltage		2.0 4.5 6.0			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH}	I _{OH} =-20μA	2.0	1.9	2.0	1.9		1.9		V
				4.5	4.4	4.5	4.4		4.4		
		or V _{IL}	I _{OH} =-4mA I _{OH} =-5.2mA	6.0	5.9	6.0	5.9		5.9		
				4.5	3.98	4.3	3.84		3.7		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH}	I _{OL} =20μA	2.0			0.1		0.1		V
				4.5			0.1		0.1		
		or V _{IL}	I _{OL} =4mA I _{OL} =5.2mA	6.0			0.1		0.1		
				4.5		0.17	0.26		0.33		
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	6.0			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	6.0			4		40		80	μA

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HCT112		GD54HCT112		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		4.5 to 5.5	2.0			2.0		2.0		V
V _{IL}	LOW level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH}	I _{OH} =-20μA	4.5	4.4	4.5	4.4		4.4		V
		or V _{IL}	I _{OH} =-4mA	4.5	3.98	4.3	3.84		3.7		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH}	I _{OL} =20μA	4.5			0.1		0.1		V
		or V _{IL}	I _{OL} =4mA	4.5		0.17	0.26		0.33		
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	5.5			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	5.5			4		40		80	μA

Timing Requirements for HC: $t_r = t_f = 6\text{ns}$ $C_L = 50\text{ pF}$

SYMBOL	PARAMETER		V _{CC} (V)	T _A = 25°C			GD74HC112		GD54HC112		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t _w	Pulse width	$\overline{PR}, \overline{CLR}$ (high or low)	2.0	80	30		100		120		ns
			4.5	16	10		20		25		
			6.0	14	8		18		22		
		\overline{CLK} (high or low)	2.0	80	30		100		120		ns
			4.5	16	10		20		25		
			6.0	14	8		18		22		
t _{su}	Set up Time	Data to \overline{CLK}	2.0	60	30		80		100		ns
			4.5	15	10		18		20		
			6.0	14	8		16		18		
t _{rec}	Recovery time	$\overline{PR}, \overline{CLR}$ to \overline{CLK}	2.0	5	0		5		5		ns
			4.5	5	0		5		5		
			6.0	5	0		5		5		
t _h	Hold Time	Data to \overline{CLK}	2.0	3	0		3		3		ns
			4.5	3	0		3		3		
			6.0	3	0		3		3		

AC Characteristics for HC: $t_r = t_f = 6\text{ns}$ $C_L = 50\text{ pF}$

SYMBOL	PARAMETER		V _{CC} (V)	T _A = 25°C			GD74HC112		GD54HC112		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
f _{max}	Maximum Clock Pulse Frequency		2.0	6	20		5		4		MHz
			4.5	30	65		25		20		
			6.0	35	75		30		25		
t _{PLH} / t _{PHL}	Propagation Delay Time n \overline{CLK} to nQ		2.0		46	160		200		240	ns
			4.5		15	30		40		50	
			6.0		14	28		35		45	
t _{PLH} / t _{PHL}	Propagation Delay Time n \overline{CLK} to n \overline{Q}		2.0		50	160		200		240	ns
			4.5		17	30		40		50	
			6.0		16	28		35		45	
t _{PLH} / t _{PHL}	Propagation Delay Time n \overline{PR} to nQ, n \overline{Q}		2.0		45	155		190		230	ns
			4.5		15	28		38		45	
			6.0		14	26		34		42	
t _{PLH} / t _{PHL}	Propagation Delay time n \overline{CLR} to nQ, n \overline{Q}		2.0		45	155		190		230	ns
			4.5		15	28		38		45	
			6.8		14	26		34		42	
t _{TLH} / t _{THL}	Output Transition time		2.0		25	70		85		100	ns
			4.5		8	15		18		22	
			6.0		7	13		16		19	

Timing Requirements for HCT: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER		V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HCT112		GD54HCT112		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_w	Pulse width	$\overline{PR}, \overline{CLR}$ (low)	4.5	18	10		20		25		ns
		\overline{CLK} (high or low)	4.5	16	10		20		25		ns
t_{su}	Set up Time	Data to \overline{CLK}	4.5	15	10		18		20		ns
t_{rec}	Recovery time	$\overline{PR}, \overline{CLR}$ to \overline{CLK}	4.5	5	0		5		5		ns
t_h	Hold Time	Data to $\overline{CLK}\uparrow$	4.5	3	0		3		3		ns

AC Characteristics for HCT: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HCT112		GD54HCT112		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
f_{max}	Maximum Clock Pulse Frequency	4.5	27	54		22		18		MHz
t_{PLH} / t_{PHL}	Propagation Delay Time $n\overline{CLK}$ to nQ	4.5		17	30		40		50	ns
t_{PLH} / t_{PHL}	Propagation Delay Time $n\overline{CLK}$ to $n\overline{Q}$	4.5		17	30		40		50	ns
t_{PLH} / t_{PHL}	Propagation Delay Time $n\overline{PR}$ to $nQ, n\overline{Q}$	4.5		15	28		38		45	ns
t_{PLH} / t_{PHL}	Propagation Delay time $n\overline{CLR}$ to $nQ, n\overline{Q}$	4.5		15	28		38		45	ns
t_{TLH} / t_{THL}	Output Transition time	4.5		8	15		18		22	ns

AC Waveforms

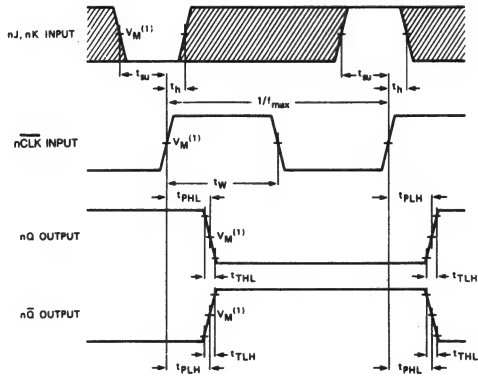


Fig. 2 Waveforms showing the clock (\overline{nCLK}) to output (nQ , $n\overline{Q}$) propagation delays, the clock pulse width, the nJ , nK to \overline{nCLK} set-up times, the \overline{nCLK} to nJ , nK hold times, the output transition times and the maximum clock pulse frequency.

Note to Fig. 2

The shaded areas indicate when the input is permitted to change for predictable output performance.

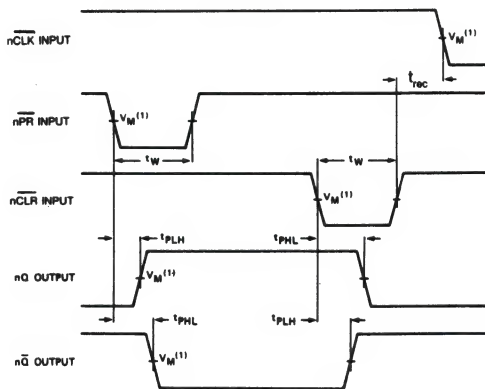


Fig. 3 Waveforms showing the preset (\overline{nPR}) and clear (\overline{nCLR}) input to input (nQ , $n\overline{Q}$) propagation delays, the preset and clear pulse width and the \overline{nPR} to \overline{nCLK} recovery time.

Note to AC waveforms

- (1) HC : $V_M = 50\%$; $V_I = \text{GND to } V_{CC}$.
HCT : $V_M = 1.3V$; $V_I = \text{GND to } 3V$.

GD54/74HC113, GD54/74HCT113

DUAL J-K FLIP-FLOPS WITH PRESET

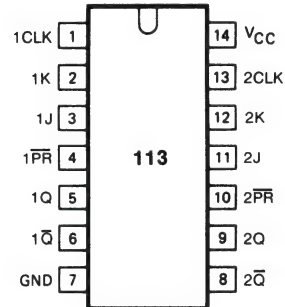
General Description

These devices are identical in pinout to the 54/74LS113. They consist of two J-K flip-flops with individual J, K, Clock, and Preset inputs. These flip-flops are edge sensitive to the clock input and change state on the negative going transition of the clock pulse. Both Q and \bar{Q} outputs are available from each flip-flop. Preset is independent of the Clock and accomplished by a Low level on the input. These devices are characterized for operation over wide temperature ranges to meet industry and military specifications.

Features

- Low Power consumption characteristic of CMOS devices
- Output drive capability: 10 LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts
for HCT 4.5 to 5.5 volts
- Low input current: $1\mu\text{A}$ Max.
- Low quiescent current: $40\mu\text{A}$ Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs.

Pin Configuration



Suffix-Blank : Plastic Dual In Line Package
 Suffix-J : Ceramic Dual In Line Package
 Suffix-D : Small Outline Package

Logic Symbol

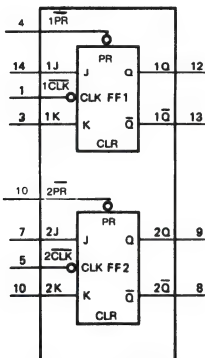


Fig. 1 Logic symbol

Function Table

INPUTS				OUTPUTS	
\overline{nPR}	$nCLK$	nJ	nK	nQ	\overline{nQ}
L	X	X	X	H	L
H	\downarrow	L	L	Q_0	$\overline{Q_0}$
H	\downarrow	H	L	H	L
H	\downarrow	L	H	L	H
H	\downarrow	H	H	TOGGLE	
H	H	X	X	Q_0	$\overline{Q_0}$

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HC113		GD54HC113		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2		1.5 3.15 4.2		V
V _{IL}	LOW level input voltage		2.0 4.5 6.0			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH}	I _{OH} =−20μA	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0	1.9 4.4 5.9		1.9 4.4 5.9		V
		or V _{IL}	I _{OH} =−4mA I _{OH} =−5.2mA	4.5 6.0	3.98 5.48	4.3 5.2	3.84 5.34		3.7 5.2		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH}	I _{OL} =20μA	2.0 4.5 6.0			0.1 0.1 0.1		0.1 0.1 0.1		V
		or V _{IL}	I _{OL} =4mA I _{OL} =5.2mA	4.5 6.0		0.17 0.15	0.26 0.26		0.33 0.33		
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	6.0			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	6.0			4		40		80	μA

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HCT113		GD54HCT113		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		4.5 to 5.5	2.0			2.0		2.0		V
V _{IL}	LOW level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH}	I _{OH} =−20μA	4.5	4.4	4.5	4.4		4.4		V
		or V _{IL}	I _{OH} =−4mA	4.5	3.98	4.3	3.84		3.7		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH}	I _{OL} =20μA	4.5		0.1	0.1		0.1		V
		or V _{IL}	I _{OL} =4mA	4.5		0.17	0.33		0.4		
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	5.5			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	5.5			4		40		80	μA

Timing Requirements for HC: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER		V_{CC} (V)	$T_A=25^\circ\text{C}$			GD54HC113		GD54HC113		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_w	Pulse width	\overline{PR}	2.0	80	30		100		120		ns
			4.5	16	10		20		25		
			6.0	14	8		18		22		
		CLK	2.0	80	30		100		120		ns
			4.5	16	10		20		25		
			6.0	14	8		18		22		
t_{su}	Setup time	Data to CLK	2.0	60	30		80		100		ns
			4.5	15	10		18		20		
			6.0	14	8		16		18		
t_{rec}	Recovery time	\overline{PR} to CLK	2.0	5	0		5		5		ns
			4.5	5	0		5		5		
			6.0	5	0		5		5		
t_h	Hold time	CLK to Data	2.0	3	0		3		3		ns
			4.5	3	0		3		3		
			6.0	3	0		3		3		

AC Characteristics for HC: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER		V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HC113		GD54HC113		UNIT
				MIN.	TPY.	MAX.	MIN.	MAX.	MIN.	MAX.	
f_{max}	Maximum Clock Pulse Frequency		2.0	6	20		5		4		MHz
			4.5	30	65		25		20		
			6.0	35	75		30		25		
$t_{PLH}/$ t_{PHL}	Propagation Delay Time $n\text{CLK}$ to nQ		2.0		46	160		200		240	ns
			4.5		15	30		40		45	
			6.0		14	28		35		50	
$t_{PLH}/$ t_{PHL}	Propagation Delay Time $n\text{CLK}$ to $n\overline{Q}$		2.0		50	160		200		240	ns
			4.5		17	30		40		50	
			6.0		16	28		35		45	
$t_{PLH}/$ t_{PHL}	Propagation Delay Time $n\overline{PR}$ to nQ , $n\overline{Q}$		2.0		45	155		190		230	ns
			4.5		15	28		38		45	
			6.0		14	26		34		40	
$t_{TLH}/$ t_{THL}	Output Transition Time		2.0		25	70		85		100	ns
			4.5		8	15		18		22	
			6.0		7	13		16		19	

Timing Requirements for HCT: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER		V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HCT113		GD54HCT113		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_w	Pulse width	\overline{PR}	4.5	18	10		20		25		ns
		CLK	4.5	16	10		20		25		ns
t_{su}	Setup time	Data to CLK	4.5	15	10		18		20		ns
t_{rec}	Recovery time	\overline{PR} to CLK	4.5	5	0		5		5		ns
t_h	Hold time	CLK to Data	4.5	3	0		3		3		ns

AC Characteristics for HC: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HCT113		GD54HCT113		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
f_{max}	Maximum Clock Pulse Frequency	4.5	27	54		22		18		MHz
t_{PLH}/t_{PHL}	Propagation Delay Time nCLK to nQ	4.5		17	30		40		50	ns
t_{PLH}/t_{PHL}	Propagation Delay Time nCLK to n \overline{Q}	4.5		17	30		40		50	ns
t_{PLH}/t_{PHL}	Propagation Delay Time n \overline{PR} to nQ, n \overline{Q}	4.5		15	28		38		45	ns
t_{TLH}/t_{THL}	Output Transition Time	4.5		8	15		18		22	ns

AC Waveforms

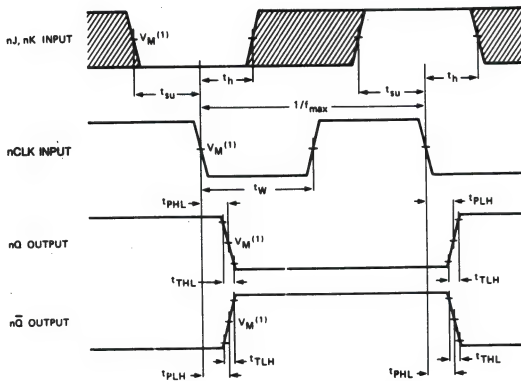


Fig. 3 Waveforms showing the clock (nCLK) to output (nQ, nQ̄) propagation delays, the clock pulse width, the nJ and nK to nCLK set-up and hold times, the output transition times and the maximum clock pulse frequency.

Note to Fig. 3

The shaded areas indicate when the input is permitted to change for predictable output performance.

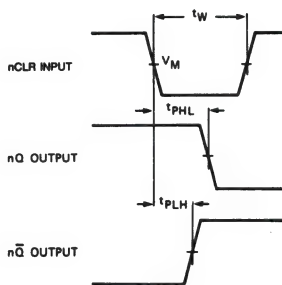


Fig. 4 Waveforms showing the clear (nCLR) input to output (nQ, nQ̄) propagation delays and the clear pulse width.

Note to AC waveforms

- (1) HC : $V_M = 50\%$; $V_I = \text{GND}$ to V_{CC} .
HCT : $V_M = 1.3V$; $V_I = \text{GND}$ to $3V$.

GD54/74HC123, GD54/74HCT123

DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATORS

General Description

These devices are identical in pinout to the 54/74LS123. They consist of two retriggerable monostable multivibrators. Each multivibrator features an active-low asynchronous clear and both negative-and positive-edge triggered inputs, either of which can be used as an enable. Also included is a clear input that when taken low resets the one shot. The output pulse width can be controlled with stability by the simple equation:

$$PW = (R_{EXT}) (C_{EXT})$$

Where PW is in seconds, R_{EXT} is in ohms, and C_{EXT} is in farads. Refer to GD74HC/HCT 221 and 423 for different functionalities.

Features

- Low Power consumption characteristic of CMOS devices
- Output drive capability: 10 LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts
for HCT 4.5 to 5.5 volts
- Low input current: $1\mu A$ Max.
- Low quiescent current: $80\mu A$ Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs

Functional Symbol

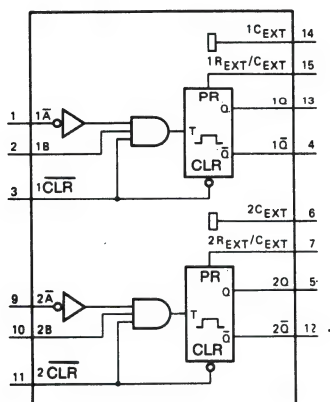
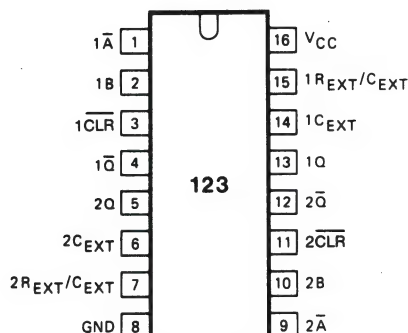


Fig. 1 Functional symbol

Pin Configuration



Suffix-Blank : Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package
Suffix-D : Small Outline Package

Function Table

INPUTS			OUTPUTS	
\overline{nCLR}	\overline{nA}	nB	nQ	\overline{nQ}
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	\uparrow	\square	\square
H	\downarrow	H	\square	\square
\uparrow	L	H	\square	\square

\square = one HIGH level output pulse
 \square = one LOW level output pulse

Timing Component

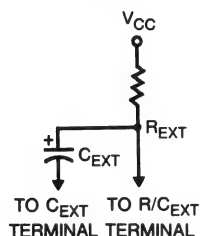
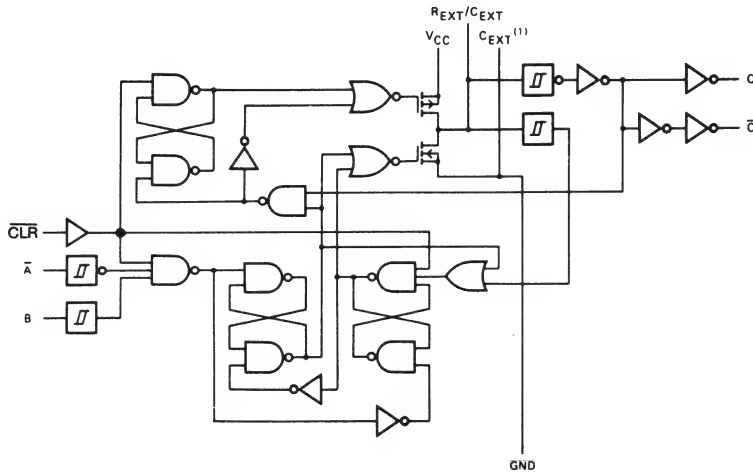


Fig. 2 Timing Component

Logic Diagram



It is recommended to ground pins 6 ($2C_{EXT}$) and 14 ($1C_{EXT}$) externally to pin 8 (GND).

Fig. 3 Logic diagram

Theory of Operation

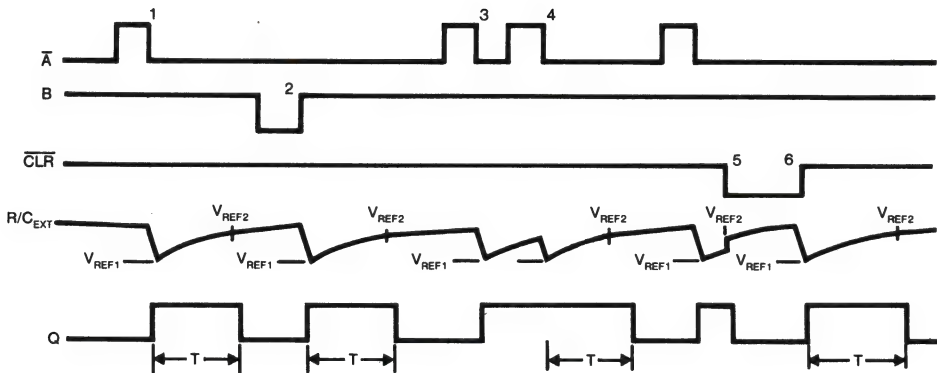


Fig. 4 (1) POSITIVE EDGE TRIGGER
(2) NEGATIVE EDGE TRIGGER
(3) POSITIVE EDGE TRIGGER
(4) POSITIVE EDGE RE-TRIGGER (PULSE LENGTHENING)
(5) RESET PULSE SHORTENING
(6) CLEAR TRIGGER

Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC Supply voltage		-0.5	+7	V
I_{IK}, I_{OK}	DC input or output diode current	for $V_I < -0.5$ or $V_I > V_{CC} + 0.5V$		20	mA
I_O	DC output source or sink current	for $-0.5V < V_O < V_{CC} + 0.5V$		25	mA
I_{CC}	DC V_{CC} or GND current			50	mA
T_{stg}	Storage temperature range		-65	150	°C
P_D	Power dissipation per package	above +70°C: derate linearly with 8mW/K		500	mW
T_L	Lead temperature	At distance 1/16 ± 1/32 in. from case for 60 sec(CERAMIC) 10 sec(PLASTIC)		300 260	°C

Recommended Operating Conditions

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range V_{CC} : GD54/74HC Types GD54/74HCT Types	2 4.5	6 5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A : GD74 Types GD54 Types	-40 -55	+85 +125	°C
Input Rise and Fall times t_r, t_f : GD54/74HC Types at 2V at 4.5V at 6V GD54/74HCT Types at 4.5V		1000 500 400 500	ns

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HC123		GD54HC123		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2		1.5 3.15 4.2		V
V _{IL}	LOW level input voltage		2.0 4.5 6.0			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH} or V _{IL}	I _{OH} =-20μA	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0	1.9 4.4 5.9		1.9 4.4 5.9		V
				I _{OH} =-4mA I _{OH} =-5.2mA	4.5 6.0	3.98 5.48	4.3 5.2		3.84 5.34	3.7 5.2	
			I _{OL} =20μA	2.0 4.5 6.0			0.1 0.1 0.1		0.1 0.1 0.1		
				I _{OL} =4mA I _{OL} =5.2mA	4.5 6.0	0.17 0.15	0.26 0.26		0.33 0.33	0.4 0.4	
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	6.0			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	6.0			8		80		160	μA

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HCT123		GD54HCT123		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		4.5 to 5.0	2.0			2.0		2.0		V
V _{IL}	LOW level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH} or V _{IL}	I _{OH} =-20μA	4.5	4.4	4.5	4.4		4.4		V
			I _{OH} =-4mA	4.5	3.98	4.3	3.84		3.7		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH} or V _{IL}	I _{OL} =20μA	4.5			0.1		0.1		V
			I _{OL} =4mA	4.5		0.17	0.26		0.33		
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	5.5			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	5.5			8		80		160	μA

Timing Requirements for HC: $t_r = t_f = 6\text{ns}$ $C_L = 50\text{ pF}$

SYMBOL	PARAMETER		V_{CC} (V)	$T_A = 25^\circ\text{C}$			GD74HC123		GD54HC123		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_w	Pulse width	Trigger $n\bar{A} = \text{low}$, $nB = \text{high}$ Clear $n\overline{\text{CLR}} = \text{low}$	2.0 4.5 6.0	100 20 17			125 25 21		150 30 26		ns
		Output $nQ = \text{high}$, $n\bar{Q} = \text{low}$ $C_{EXT} = 100\text{nF}$, $R_{EXT} = 10\text{K}\Omega$	5.0		450						μs
		Output $nQ = \text{high}$, $n\bar{Q} = \text{low}$ $C_{EXT} = 0\text{pF}$, $R_{EXT} = 5\text{K}\Omega$	5.0		75						ns
t_{rt}	Retrigger time	$n\bar{A}$, nB $C_{EXT} = 0\text{pF}$, $R_{EXT} = 5\text{K}\Omega$	5.0		44						ns
R_{ext}	External timing resistor. Note 2		2.0 5.0	10 2		1,000 100					$\text{K}\Omega$
C_{ext}	External timing capacitor. Note 3		5.0	No limits							pF

AC Characteristics for HC: $t_r = t_f = 6\text{ns}$ $C_L = 50\text{ pF}$

SYMBOL	PARAMETER		V_{CC} (V)	$T_A = 25^\circ\text{C}$			GD74HC123		GD54HC123		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PHL}	Propagation Delay Time $n\overline{\text{CLR}}$, $n\bar{A}$, nB to $n\bar{Q}$		2.0 4.5 6.0		83 30 24	225 51 43		290 64 54		360 64 54	ns
t_{PLH}	Propagation Delay Time $n\overline{\text{CLR}}$, $n\bar{A}$, nB to nQ		2.0 4.5 6.0		80 30 24	225 51 43		290 64 54		360 64 54	ns
t_{PHL}	Propagation Delay Time $n\overline{\text{CLR}}$ to $n\bar{Q}$		2.0 4.5 6.0		66 24 19	200 43 37		260 54 46		310 54 46	ns
t_{PLH}	Propagation Delay Time $n\overline{\text{CLR}}$ to nQ		2.0 4.5 6.0		66 24 19	200 43 37		260 54 46		310 54 46	ns
$t_{TLH}/$ t_{THL}	Output Transition Time		2.0 4.5 6.0		19 7 6	75 15 13		95 19 15		110 22 19	ns

Timing Requirements for HCT: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER		V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HCT123		GD54HCT123		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_w	Pulse width	Trigger $n\bar{A}=\text{low}$, $nB=\text{high}$ Clear $n\bar{CLR}=\text{low}$	4.5	20			25		30		ns
		Output $nQ=\text{high}$, $n\bar{Q}=\text{low}$ $C_{EXT}=100\text{nF}$, $R_{EXT}=10\text{K}\Omega$	5.0		450						μs
		Output $nQ=\text{high}$, $n\bar{Q}=\text{low}$ $C_{EXT}=\text{OpF}$, $R_{EXT}=5\text{K}\Omega$	5.0		75						ns
t_{rt}	Retrigger time	$n\bar{A}$, nB $C_{EXT}=\text{OpF}$, $R_{EXT}=5\text{K}\Omega$	5.0		44						ns
R_{ext}	External timing resistor. Note 2		5.0	2		100					$\text{K}\Omega$
C_{ext}	External timing capacitor. Note 3		5.0	No limits							pF

AC Characteristics for HCT: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HCT123		GD54HCT123		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PHL}	Propagation Delay Time $n\bar{CLR}$, $n\bar{A}$, nB to $n\bar{Q}$	4.5		30	51		64		77	ns
t_{PLH}	Propagation Delay Time $n\bar{CLR}$, $n\bar{A}$, nB to nQ	4.5		30	51		64		77	ns
t_{PHL}	Propagation Delay Time $n\bar{CLR}$ to $n\bar{Q}$	4.5		27	46		58		68	ns
t_{PLH}	Propagation Delay Time $n\bar{CLR}$ to nQ	4.5		27	46		58		68	ns
$t_{TLH}/$ t_{THL}	Output Transition Time	4.5		7	15		19		22	ns

AC Waveforms

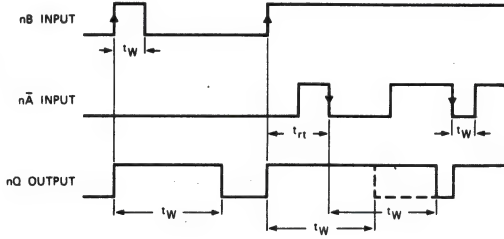


Fig. 5 Output pulse control using retrigger pulse; $n\overline{CLR}$ =HIGH.

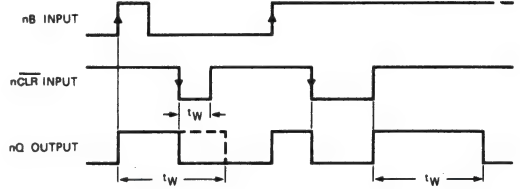


Fig. 6 Output pulse control using reset input $n\overline{CLR}$; $n\overline{A}$ =LOW.

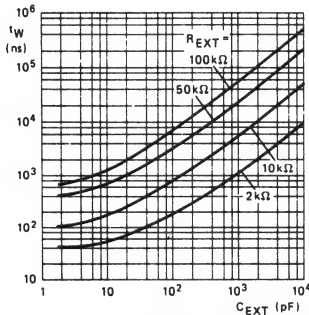


Fig. 7 Typical output pulse width as a function of the external capacitor values at V_{CC} =5.0V and T_{amb} =25°C.

Notes to AC characteristics

- For other R_{EXT} and C_{EXT} combinations see Fig. 7

If $C_{EXT} > 10\text{nF}$, the next formula is valid:

$$t_W = K \times R_{EXT} \times C_{EXT} \text{ (typ.)}$$

where, t_W = output pulse width in ns;

R_{EXT} = external resistor in kΩ;

C_{EXT} = external capacitor in pF;

K = constant=0.45 for

V_{CC} =5.0V and 0.48 for V_{CC} =2.0V.

The inherent test jig and pin capacitance at pins 15 and 7 (nR_{EXT}/C_{EXT}) is approximately 7 pF.

- The time to retrigger the monostable multivibrator depends on the values of R_{EXT} and C_{EXT} . The output pulse width will only be extended when the time between the active-going edges of the trigger input pulses meets the minimum retrigger time. If $C_{EXT} > 10\text{nF}$, the next formula (at V_{CC} =5.0V) for the set-up time of a retrigger pulse is valid:

$$t_{RT} = 35 + (0.11 \times C_{EXT}) + (0.04 \times R_{EXT} \times C_{EXT}) \text{ (typ.)}$$

where, t_{RT} = retrigger time in ns;

C_{EXT} = external capacitor in pF;

R_{EXT} = external resistor in kΩ.

The inherent test jig and pin capacitance at pins 15 and 7 (nR_{EXT}/C_{EXT}) is approximately 7 pF.

- When the device is powered-up, initiate the device via a reset pulse, when $C_{EXT} < 50\text{pF}$.

GD54/74HC125, GD54/74HCT125

QUAD 3-STATE (ACT-LOW) NONINVERTING BUFFERS

General Description

These devices are identical in pinout to the 54/74LS125. They contain four independent 3-state noninverting buffers which are designed to be used with 3-state memory address drivers, clock drivers, and other bus-oriented systems. The GD54/74 HC/HCT 125 requires the 3-state control input to be taken high to put the output into the high impedance state (active low). Refer to GD54/74 HC/HCT 126 for active-high operation with same functionality. Both of them have current driving capabilities. These devices are characterized for operation over wide temperature ranges to meet industry and military specifications

Features

- Low Power consumption characteristic of CMOS devices
- Output drive capability: 15 LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts
for HCT 4.5 to 5.5 volts
- Low input current: $1\mu\text{A}$ Max.
- Low quiescent current: $80\mu\text{A}$ Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs

Logic Diagram

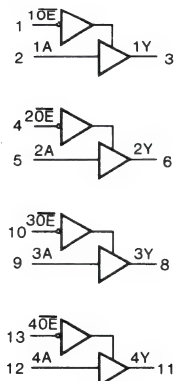
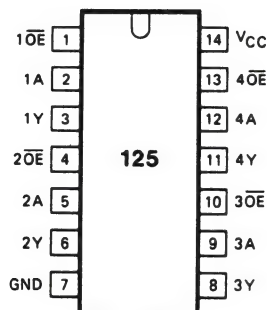


Fig. 1 Logic diagram

Pin Configuration



Suffix-Blank : Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package
Suffix-D : Small Outline Package

Function Table

INPUTS		OUTPUT
nOE	nA	nY
L	L	L
L	H	H
H	X	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC Supply voltage		-0.5	+7	V
I_{IK}, I_{OK}	DC input or output diode current	for $V_I < -0.5$ or $V_I > V_{CC} + 0.5V$		20	mA
I_O	DC output source or sink current	for $-0.5V < V_O < V_{CC} + 0.5V$		35	mA
I_{CC}	DC V_{CC} or GND current			70	mA
T_{stg}	Storage temperature range		-65	150	°C
P_D	Power dissipation per package	above +70°C: derate linearly with 8mW/K		500	mW
T_L	Lead temperature	At distance 1/16±1/32 in. from case for 60 sec(CERAMIC) 10 sec(PLASTIC)		300 260	°C

Recommended Operating Conditions

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range V_{CC} : GD54/74HC Types GD54/74HCT Types	2 4.5	6 5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A : GD74 Types GD54 Types	-40 -55	+85 +125	°C
Input Rise and Fall times t_r, t_f : GD54/74HC Types at 2V at 4.5V at 6V GD54/74HCT Types at 4.5V		1000 500 400 500	ns

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD54HC125		GD74HC125		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2		1.5 3.15 4.2		V
V _{IL}	LOW level input voltage		2.0 4.5 6.0			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH} or V _{IL}	I _{OH} =-20μA	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0	1.9 4.4 5.9		1.9 4.4 5.9		V
			I _{OH} =-6mA I _{OH} =-7.8mA	4.5 6.0	3.98 5.48	4.3 5.2	3.84 5.34		3.7 5.2		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH} or V _{IL}	I _{OL} =20μA	2.0 4.5 6.0			0.1 0.1 0.1	0.1 0.1 0.1		0.1 0.1 0.1	V
			I _{OL} =6mA I _{OL} =7.8mA	4.5 6.0		0.17 0.15	0.26 0.26	0.33 0.33		0.4 0.4	
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	6.0			0.1		1.0		1.0	μA
I _{OZ}	Three-State leakage current	V _{IN} =V _{IH} or V _{IL} V _O =V _{CC} or GND	6.0		0.01	0.5		5.0		10.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	6.0			8		80		160	μA

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HCT125		GD54HCT125		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		4.5 to 5.0	2.0			2.0		2.0		V
V _{IL}	LOW level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH} or V _{IL}	I _{OH} =-20μA	4.5	4.4	4.5	4.4		4.4		V
			I _{OH} =-6mA	4.5	3.98	4.3	3.84		3.7		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH} or V _{IL}	I _{OL} =20μA	4.5		0.1		0.1		0.1	V
			I _{OL} =6mA	4.5		0.17	0.26	0.33		0.4	
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	5.5			0.1		1.0		1.0	μA
I _{OZ}	Three-State leakage current	V _{IN} =V _{IH} or V _{IL} V _O =V _{CC} or GND	5.5		0.01	0.5		5.0		10.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	5.5			8		80		160	μA

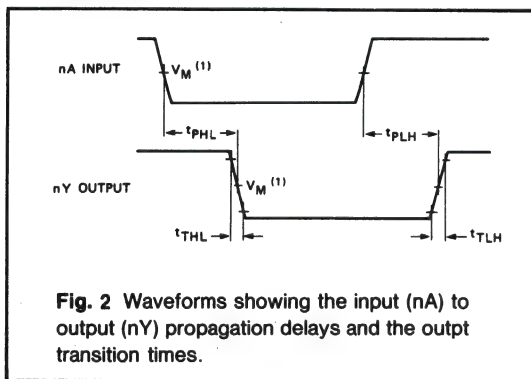
AC Characteristics for HC: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HC125		GD54HC125		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} / t_{PHL}	Propagation Delay Time nA to nY	2.0 4.5 6.0		30 10 9	100 20 16		125 25 20		150 30 25	ns
t_{PZH} / t_{PZL}	3-state Output Enable time $n\overline{OE}$ to nY	2.0 4.5 6.0		32 12 10	120 24 20		155 30 25		180 38 32	ns
t_{PHZ} / t_{PLZ}	3-state Output Disable Time $n\overline{OE}$ to nY	2.0 4.5 6.0		32 13 10	120 25 20		155 30 25		180 38 32	ns
t_{TLH} / t_{THL}	Output Transition Time	2.0 4.5 6.0		20 7 6	60 12 10		75 15 13		90 18 15	ns

AC Characteristics for HCT: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

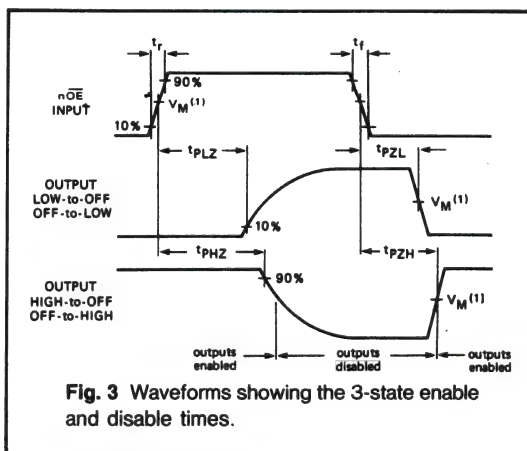
SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HCT125		GD54HCT125		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} / t_{PHL}	Propagation Delay Time nA to nY	4.5		14	26		33		38	ns
t_{PZH} / t_{PZL}	3-state Output Enable time $n\overline{OE}$ to nY	4.5		14	28		33		38	ns
t_{PHZ} / t_{PLZ}	3-state Output Disable Time $n\overline{OE}$ to nY	4.5		15	28		35		40	ns
t_{TLH} / t_{THL}	Output Transition Time	4.5		7	12		15		18	ns

AC Waveforms



Note to AC waveforms

- (1) HC : $V_M=50\%$; $V_I=\text{GND to } V_{CC}$.
HCT : $V_M=1.3\text{V}$; $V_I=\text{GND to } 3\text{V}$.



GD54/74HC126, GD54/74HCT126

QUAD 3-STATE (ACT-HIGH) NONINVERTING BUFFERS

General Description

These devices are identical in pinout to the 54/74LS126. They contain four independent 3-state noninverting buffers which are designed to be used with 3-state memory address drivers, clock drivers, and other bus-oriented systems. The GD54/74 HC/HCT126 requires the 3-state control input to be taken low to put the output into the high impedance state (active-high). Refer to GD54/74 HC/HCT125 for active-low operation with same functionality. Both of them have high current driving capabilities. These devices are characterized for operation over wide temperature ranges to meet industry and military specifications

Features

- Low Power consumption characteristic of CMOS devices
- Output drive capability: 15 LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts
for HCT 4.5 to 5.5 volts
- Low input current: 1 μ A Max.
- Low quiescent current: 80 μ A Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs

Logic Diagram

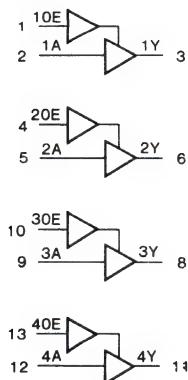
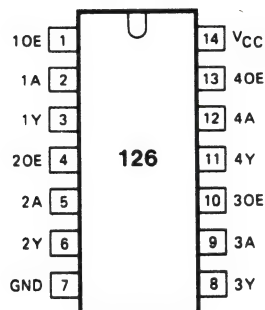


Fig. 1 Logic diagram

Pin Configuration



Suffix-Blank : Plastic Dual In Line Package
 Suffix-J : Ceramic Dual In Line Package
 Suffix-D : Small Outline Package

Function Table

INPUTS		OUTPUT
nOE	nA	nY
H	L	L
H	H	H
L	X	Z

H = HIGH voltage level

L = LOW voltage level

X = don't care

Z = high impedance OFF-state

Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC Supply voltage		-0.5	+7	V
I_{IK}, I_{OK}	DC input or output diode current	for $V_I < -0.5$ or $V_I > V_{CC} + 0.5V$		20	mA
I_O	DC output source or sink current	for $-0.5V < V_O < V_{CC} + 0.5V$		35	mA
I_{CC}	DC V_{CC} or GND current			70	mA
T_{stg}	Storage temperature range		-65	150	°C
P_D	Power dissipation per package	above +70°C: derate linearly with 8mW/K		500	mW
T_L	Lead temperature	At distance 1/16 ± 1/32 in. from case for 60 sec(CERAMIC) 10 sec(PLASTIC)		300 260	°C

Recommended Operating Conditions

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range V_{CC} : GD54/74HC Types GD54/74HCT Types	2 4.5	6 5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A : GD74 Types GD54 Types	-40 -55	+85 +125	°C
Input Rise and Fall times t_r, t_f : GD54/74HC Types at 2V at 4.5V at 6V GD54/74HCT Types at 4.5V		1000 500 400 500	ns

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HC126		GD54HC126		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2		1.5 3.15 4.2		V
V _{IL}	LOW level input voltage		2.0 4.5 6.0			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH} or V _{IL}	I _{OH} =−20μA	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0	1.9 4.4 5.9		1.9 4.4 5.9		V
				I _{OH} =−6mA I _{OH} =−7.8mA	4.5 6.0	3.98 5.48	4.3 5.2		3.84 5.34	3.7 5.2	
			I _{OL} =20μA	2.0 4.5 6.0			0.1 0.1 0.1		0.1 0.1 0.1	0.1 0.1 0.1	
				I _{OL} =6mA I _{OL} =7.8mA	4.5 6.0	0.17 0.15	0.26 0.26		0.33 0.33	0.4 0.4	
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	6.0			0.1		1.0		1.0	μA
I _{OZ}	Three-State leakage current	V _{IN} =V _{IH} or V _{IL} V _O =V _{CC} or GND	6.0		0.01	0.5		5.0		10.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	6.0			8		80		160	μA

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HCT126		GD54HCT126		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		4.5 to 5.0	2.0			2.0		2.0		V
V _{IL}	LOW level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH} or V _{IL}	I _{OH} =−20μA	4.5	4.4	4.5	4.4		4.4		V
			I _{OH} =−6mA	4.5	3.98	4.3	3.84		3.7		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH} or V _{IL}	I _{OL} =20μA	4.5			0.1		0.1		V
			I _{OL} =6mA	4.5		0.17	0.26		0.33		
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	5.5			0.1		1.0		1.0	μA
I _{OZ}	Three-State leakage current	V _{IN} =V _{IH} or V _{IL} V _O =V _{CC} or GND	5.5		0.01	0.5		5.0		10.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	5.5			8		80		160	μA

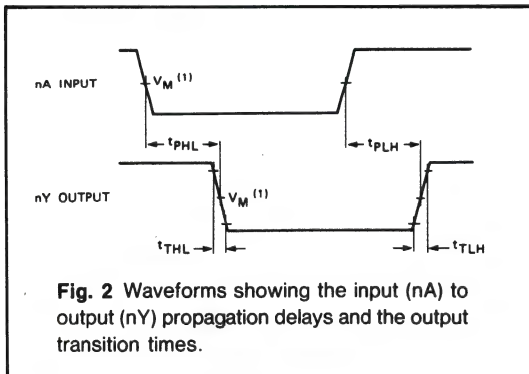
AC Characteristics for HC: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HC126		GD54HC126		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} / t_{PHL}	Propagation Delay Time nA to nY	2.0 4.5 6.0		30 10 9	100 20 16		125 25 20		150 30 25	ns
t_{PZH} / t_{PZL}	3-state Output Enable time nOE to nY	2.0 4.5 6.0		32 11 10	120 24 20		155 30 25		180 38 32	ns
t_{PHZ} / t_{PLZ}	3-state Output Disable Time nOE to nY	2.0 4.5 6.0		32 13 10	120 25 20		155 30 25		180 38 32	ns
t_{TLH} / t_{THL}	Output Transition Time	2.0 4.5 6.0		20 7 6	60 12 10		75 15 13		90 18 15	ns

AC Characteristics for HCT: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

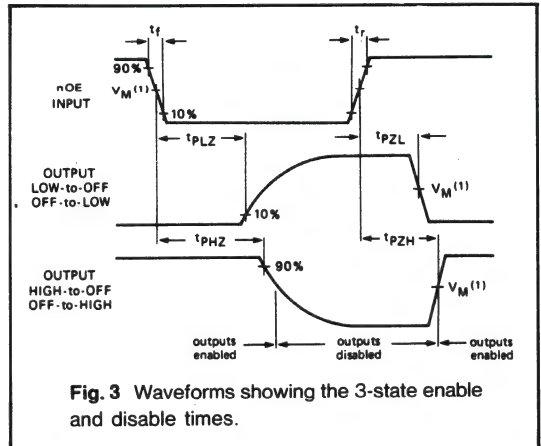
SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HCT126		GD54HCT126		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} / t_{PHL}	Propagation Delay Time nA to nY	4.5		14	26		33		38	ns
t_{PLH} / t_{PHL}	Propagation Delay Time nOE to nY	4.5		14	28		33		38	ns
t_{PLH} / t_{PHL}	Propagation Delay Time nOE to nY	4.5		15	28		35		40	ns
t_{TLH} / t_{THL}	Output Transition Time	4.5		7	12		15		18	ns

AC Waveforms



Note to AC waveforms

- (1) HC : $V_M=50\%$; $V_I=\text{GND}$ to V_{CC} .
HCT: $V_M=1.3\text{V}$; $V_I=\text{GND}$ to 3V .



GD54/74HC132, GD54/74HCT132

QUAD 2-INPUT SCHMITT-TRIGGER NAND GATES

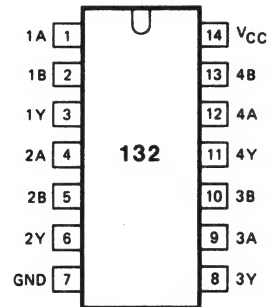
General Description

These devices are identical in pinout to the 54/74LS132. They contain four independent 2-Input NAND gates. Each input has hysteresis and can, therefore, be used to enhance noise immunity or to square up slowly changing waveforms. These devices are characterized for operation over wide temperature ranges to meet industry and military specifications

Features

- Low Power consumption characteristic of CMOS devices
- Output drive capability: 10 LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts
for HCT 4.5 to 5.5 volts
- Low input current: 1 μ A Max.
- Low quiescent current: 20 μ A Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs

Pin Configuration



Suffix-Blank : Plastic Dual In Line Package
 Suffix-J : Ceramic Dual In Line Package
 Suffix-D : Small Outline Package

Logic Symbol and Diagram

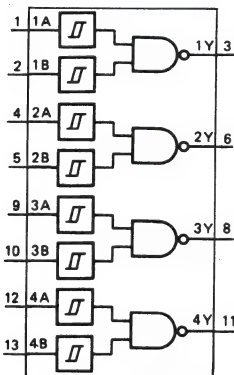


Fig. 1 Logic symbol

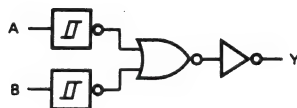


Fig. 2 Logic diagram (one schmitt trigger)

Function Table

INPUTS		OUTPUT
nA	nB	nY
L	L	H
L	H	H
H	L	H
H	H	L

H = HIGH voltage level
 L = LOW voltage level

Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC Supply voltage		-0.5	+7	V
I_{IK}, I_{OK}	DC input or output diode current	for $V_I < -0.5$ or $V_I > V_{CC} + 0.5V$		20	mA
I_O	DC output source or sink current	for $-0.5V < V_O < V_{CC} + 0.5V$		25	mA
I_{CC}	DC V_{CC} or GND current			50	mA
T_{stg}	Storage temperature range		-65	150	°C
P_D	Power dissipation per package	above +70°C: derate linearly with 8mW/K		500	mW
T_L	Lead temperature	At distance 1/16 ± 1/32 in. from case for 60 sec(CERAMIC) 10 sec(PLASTIC)		300 260	°C

Recommended Operating Conditions

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range V_{CC} : GD54/74HC Types GD54/74HCT Types	2 4.5	6 5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A : GD74 Types GD54 Types	-40 -55	+85 +125	°C
Input Rise and Fall times t_r, t_f : GD54/74HC Types at 2V at 4.5V at 6V GD54/74HCT Types at 4.5 V		1000 500 400 500	ns

Transfer Characteristic Waveforms

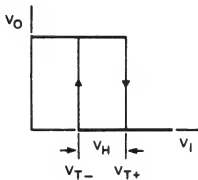


Fig. 3 Transfer characteristic

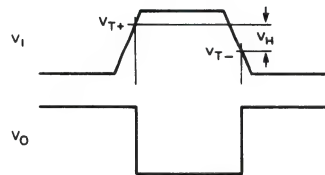


Fig. 4 Waveforms the definition of V_{T+} , V_{T-} and V_H : where V_{T+} and V_{T-} are between limits of 20% and 70%.

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A = 25 °C			GD74HC132		GD54HC132		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2		1.5 3.15 4.2		V
V _{IL}	LOW level input voltage		2.0 4.5 6.0			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V
V _{OH}	HIGH level output voltage	V _{IN} = V _{IH}	I _{OH} = -20 μA	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9	V
			I _{OH} = -4 mA	4.5 6.0	3.98 5.48	4.3 5.2		3.84 5.34		3.7 5.2	
		or V _{IL}	I _{OL} = 20 μA	2.0 4.5 6.0			0.1 0.1 0.1	0.1 0.1 0.1		0.1 0.1 0.1	
			I _{OL} = 4 mA	4.5 6.0		0.17 0.15	0.26 0.26	0.33 0.33		0.4 0.4	
V _{OL}	LOW level output voltage	V _{IN} = V _{IH}	I _{OL} = 20 μA	2.0 4.5 6.0			0.1 0.1 0.1	0.1 0.1 0.1		0.1 0.1 0.1	V
I _{IN}	Input leakage Current	V _{IN} = V _{CC} or GND		6.0		0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} = V _{CC} or GND I _{out} = 0 μA		6.0		2		20		40	μA

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A = 25 °C			GD74HCT132		GD54HCT132		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		4.5 to 5.5	2.0			2.0		2.0		V
V _{IL}	LOW level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V _{OH}	HIGH level output voltage	V _{IN} = V _{IH}	I _{OH} = -20 μA	4.5	4.4	4.5	4.4		4.4		V
		or V _{IL}	I _{OH} = -4 mA	4.5	3.98	4.3	3.84		3.7		
V _{OL}	LOW level output voltage	V _{IN} = V _{IH}	I _{OL} = 20 μA	4.5			0.1	0.1		0.1	V
		or V _{IL}	I _{OL} = 4 mA	4.5		0.17	0.26	0.33		0.4	
I _{IN}	Input leakage Current	V _{IN} = V _{CC} or GND		5.5		0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} = V _{CC} or GND I _{out} = 0 μA		5.5		2		20		40	μA

Transfer Characteristic for HC

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HC132		GD54HC132		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{T+}	Positive-going threshold		2.0 4.5 6.0	0.7 1.7 2.1	1.2 2.4 3.2	1.5 3.15 4.2	0.7 1.7 2.1	1.5 3.15 4.2	0.7 1.7 2.1	1.5 3.15 4.2	V
V _{T-}	negative-going threshold		2.0 4.5 6.0	0.3 0.9 1.2	0.65 1.7 2.1	1.0 2.2 3.0	0.3 0.9 1.2	1.0 2.2 3.0	0.3 0.9 1.2	1.0 2.2 3.0	V
V _H	Hysteresis(V _{T+} -V _{T-})		2.0 4.5 6.0	0.2 0.4 0.5	0.6 0.9 1.3	1.0 1.4 1.7	0.2 0.4 0.5	1.0 1.4 1.7	0.2 0.4 0.5	1.0 1.4 1.7	V

Transfer Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HCT132		GD54HCT132		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{T+}	Positive-going threshold		4.5 5.5	1.2 1.4	1.55 1.75	1.9 2.1	1.2 1.4	1.9 2.1	1.2 1.4	1.9 2.1	V
V _{T-}	Negative-going threshold		4.5 5.5	0.5 0.6	0.85 1.0	1.2 1.4	0.5 0.6	1.2 1.4	0.5 0.6	1.2 1.4	V
V _H	Hysteresis(V _{T+} -V _{T-})		4.5 5.5	0.4 0.5	0.9 1.0	1.4 1.5	0.4 0.5	1.4 1.5	0.4 0.5	1.4 1.5	V

AC Characteristics for HC: t_p=t_r=6ns C_L=50 pF

SYMBOL	PARAMETER	V _{CC} (V)	T _A =25°C			GD74HC132		GD54HC132		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t _{PLH} / t _{PHL}	Propagation delay time nA, nB to nY	2.0 4.5 6.0		36 12 10	125 25 21		155 30 25		190 36 30	ns
t _{PLH} / t _{THL}	Output transition time	2.0 4.5 6.0		28 7 6	75 15 13		95 19 16		110 22 19	ns

AC Characteristics for HCT: t_p=t_r=6ns C_L=50 pF

SYMBOL	PARAMETER	V _{CC} (V)	T _A =25°C			GD74HCT132		GD54HCT132		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t _{PLH} / t _{PHL}	Propagation delay time nA, nB to nY	4.5		18	30		38		45	ns
t _{PLH} / t _{THL}	Output transition time	4.5		7	15		19		22	ns

GD54/74HC133, GD54/74HCT133

13-INPUT NAND GATE

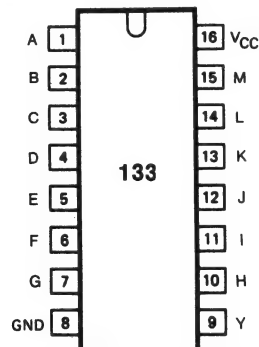
General Description

These devices are identical in pinout to the 54/74LS133. They contain a single 13-input NAND gate. These devices are characterized for operation over wide temperature ranges to meet industry and military specifications.

Features

- Low Power consumption characteristic of CMOS devices
- Output drive capability: 10 LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts
for HCT 4.5 to 5.5 volts
- Low input current: $1\mu\text{A}$ Max.
- Low quiescent current: $20\mu\text{A}$ Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs

Pin Configuration



Suffix-Blank : Plastic Dual In Line Package
 Suffix-J : Ceramic Dual In Line Package
 Suffix-D : Small Outline Package

Logic Diagram

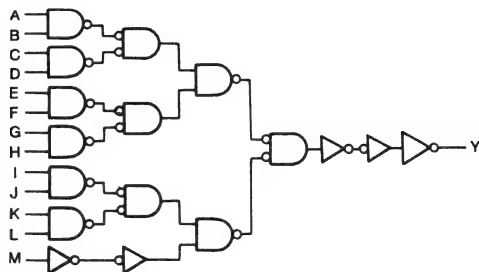


Fig. 1 Logic diagram

Function Table

INPUTS A THRU M	OUTPUT Y
All inputs H one or more inputs L	L H

Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC Supply voltage		-0.5	+7	V
I_{IK}, I_{OK}	DC input or output diode current	for $V_I < -0.5$ or $V_I > V_{CC} + 0.5V$		20	mA
I_O	DC output source or sink current	for $-0.5V < V_O < V_{CC} + 0.5V$		25	mA
I_{CC}	DC V_{CC} or GND current			50	mA
T_{stg}	Storage temperature range		-65	150	°C
P_D	Power dissipation per package	above +70°C: derate linearly with 8mW/K		500	mW
T_L	Lead temperature	At distance 1/16 ± 1/32 in. from case for 60 sec(CERAMIC) 10 sec(PLASTIC)		300 260	°C

Recommended Operating Conditions

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range V_{CC} : GD54/74HC Types GD54/74HCT Types	2 4.5	6 5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A : GD74 Types GD54 Types	-40 -55	+85 +125	°C
Input Rise and Fall times t_r, t_f : GD54/74HC Types at 2V at 4.5V at 6V GD54/74HCT Types at 4.5V		1000 500 400 500	ns

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HC133		GD54HC133		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2		1.5 3.15 4.2		V
V _{IL}	LOW level input voltage		2.0 4.5 6.0			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH}	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V
		or V _{IL}									
V _{OL}	LOW level output voltage	V _{IN} =V _{IH}	2.0 4.5 6.0			0.1 0.1 0.1	0.1 0.1 0.1		0.1 0.1 0.1		V
		or V _{IL}									
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	6.0			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	6.0			2		20		40	μA

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HCT133		GD54HCT133		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		4.5 to 5.5	2.0			2.0		2.0		V
V _{IL}	LOW level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH}	4.5	4.4	4.5		4.4		4.4		V
		or V _{IL}	4.5	3.98	4.3		3.84		3.7		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH}	4.5			0.1		0.1		0.1	V
		or V _{IL}	4.5		0.17	0.26		0.33		0.4	
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	5.5			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	5.5			2		20		40	μA

AC Characteristics for HC: $t_r=t_f=6\text{ns}$ $C_L=50\text{pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HC133		GD54HC133		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
$t_{PLH}/$ t_{PHL}	Propagation delay time A thru H to Y	2.0 4.5 6.0		65 15 12	140 29 25		180 36 31		210 42 36	ns
$t_{TLH}/$ t_{THL}	Output transition time	2.0 4.5 6.0		25 8 7	75 15 13		95 19 16		110 22 19	ns

AC Characteristics for HCT: $t_r=t_f=6\text{ns}$ $C_L=50\text{pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HCT133		GD54HCT133		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
$t_{PLH}/$ t_{PHL}	Propagation delay time A thru H to Y	4.5		18	31		40		46	ns
$t_{TLH}/$ t_{THL}	Output transition time	4.5		8	15		19		22	ns

AC Waveform

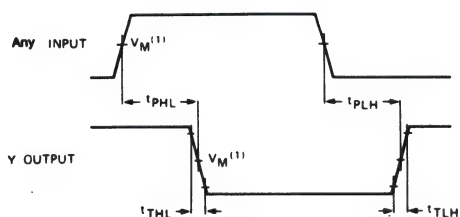


Fig. 2 Waveforms showing the (Any) Input to output (Y) propagation delays and the output transition times.

Note to AC waveform

(1) HC : $V_M=50\%$, $V_L=\text{GND to } V_{CC}$

HCT: $V_M=1.3V$; $V_L=\text{GND to } 3V$.

GD54/74HC137, GD54/74HCT137

3-TO-8 LINE DECODER/DEMULTIPLEXER WITH ADDRESS LATCH

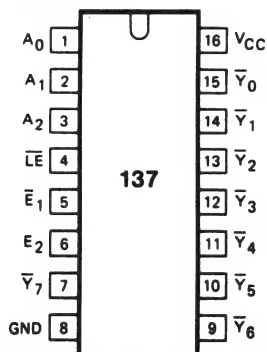
General Description

These devices are identical in pinout to the 54/74LS137. Each device decodes a 3-bit address to 1-of-3 active-low outputs. It has a transparent latch for storage of the address. Two chip selects, one active-low and one active-high, are provided to facilitate the demultiplexing, cascading, and chip-selecting functions. These devices are characterized for operation over wide temperature ranges to meet industry and military specifications.

Features

- Low Power consumption characteristic of CMOS devices
- Output drive capability: 10 LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts
for HCT 4.5 to 5.5 volts
- Low input current: 1 μ A Max.
- Low quiescent current: 80 μ A Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs

Pin Configuration



Suffix-Blank : Plastic Dual In Line Package
 Suffix-J : Ceramic Dual In Line Package
 Suffix-D : Small Outline Package

Function Table

INPUTS						OUTPUTS							
\overline{LE}	$\overline{E_1}$	E_2	A_0	A_1	A_2	$\overline{Y_0}$	$\overline{Y_1}$	$\overline{Y_2}$	$\overline{Y_3}$	$\overline{Y_4}$	$\overline{Y_5}$	$\overline{Y_6}$	$\overline{Y_7}$
H	L	H	X	X	X	stable							
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

H = HIGH voltage level
 L = LOW voltage level
 X = don't care

Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC Supply voltage		-0.5	+7	V
I_{IK}, I_{OK}	DC input or output diode current	for $V_I < -0.5$ or $V_I > V_{CC} + 0.5V$		20	mA
I_O	DC output source or sink current	for $-0.5V < V_O < V_{CC} + 0.5V$		25	mA
I_{CC}	DC V_{CC} or GND current			50	mA
T_{stg}	Storage temperature range		-65	150	°C
P_D	Power dissipation per package	above +70°C: derate linearly with 8mW/K		500	mW
T_L	Lead temperature	At distance 1/16 ± 1/32 in. from case for 60 sec(CERAMIC) 10 sec(PLASTIC)		300 260	°C

Recommended Operating Conditions

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range V_{CC} : GD54/74HC Types GD54/74HCT Types	2 4.5	6 5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A : GD74 Types GD54 Types	-40 -55	+85 +125	°C
Input Rise and Fall times t_r, t_f : GD54/74HC Types at 2V at 4.5V at 6V GD54/74HCT Types at 4.5V		1000 500 400 500	ns

Logic Diagram

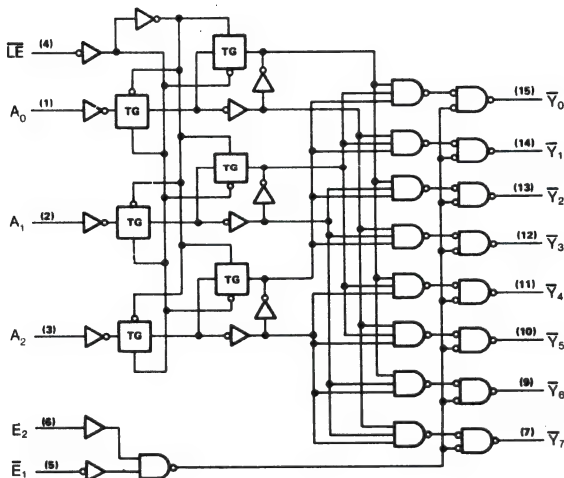


Fig. 1 Logic diagram

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION	V_{CC} (V)	$T_A = 25^\circ\text{C}$			GD74HC137		GD54HC137		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V_{IH}	HIGH level input Voltage		2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2		1.5 3.15 4.2		V
V_{IL}	LOW level input voltage		2.0 4.5 6.0			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V
V_{OH}	HIGH level	$V_{IN} = V_{IH}$	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V
	output voltage	$I_{OH} = -20\mu\text{A}$									
		or V_{IL} $I_{OH} = -4\text{mA}$ $I_{OH} = -5.2\text{mA}$	4.5 6.0	3.98 5.48	4.3 5.2		3.84 5.34		3.7 5.2		
V_{OL}	LOW level	$V_{IN} = V_{IH}$	2.0 4.5 6.0			0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V
	output voltage	$I_{OL} = 20\mu\text{A}$									
		or V_{IL} $I_{OL} = 4\text{mA}$ $I_{OL} = 5.2\text{mA}$	4.5 6.0		0.17 0.15	0.26 0.26		0.33 0.33		0.4 0.4	
$ I_{IN} $	Input leakage Current	$V_{IN} = V_{CC}$ or GND	6.0			0.1		1.0		1.0	μA
I_{CC}	Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND $I_{out} = 0\mu\text{A}$	6.0			8		80		160	μA

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION	V_{CC} (V)	$T_A = 25^\circ\text{C}$			GD74HCT137		GD54HCT137		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V_{IH}	HIGH level input Voltage		4.5 to 5.5	2.0			2.0		2.0		V
V_{IL}	LOW level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V_{OH}	HIGH level output voltage	$V_{IN} = V_{IH}$	4.5	4.4	4.5		4.4		4.4		V
		or V_{IL} $I_{OH} = -4\text{mA}$	4.5	3.98	4.3		3.84		3.7		
V_{OL}	LOW level output voltage	$V_{IN} = V_{IH}$	4.5			0.1		0.1		0.1	V
		or V_{IL} $I_{OL} = 20\mu\text{A}$ $I_{OL} = 4\text{mA}$	4.5		0.17	0.26		0.33		0.4	
$ I_{IN} $	Input leakage Current	$V_{IN} = V_{CC}$ or GND	5.5			0.1		1.0		1.0	μA
I_{CC}	Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND $I_{out} = 0\mu\text{A}$	5.5			8		80		160	μA

Timing Requirements for HC: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER		V _{CC} (V)	T _A =25°C			GD74HC137		GD54HC137		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t _w	Pulse width	LE to CLK	2.0	75			100		120		ns
			4.5	15			20		24		
			6.0	13			17		20		
t _{su}	Setup time	A _n before LE	2.0	75			95		115		ns
			4.5	15			19		23		
			6.0	13			16		20		
t _h	Hold time	A _n after LE	2.0	5			5		5		ns
			4.5	5			5		5		
			6.0	5			5		5		

AC Characteristics for HC: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER		V _{CC} (V)	T _A =25°C			GD74HC137		GD54HC137		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t _{PLH} / t _{PHL}	Propagation Delay Time A,B,C to \bar{Y}_n		2.0		82	190		230		280	ns
			4.5		22	36		45		55	
			6.0		19	31		40		46	
t _{PLH} / t _{PHL}	Propagation Delay Time E ₁ to \bar{Y}_n		2.0		55	140		180		220	ns
			4.5		17	28		35		42	
			6.0		14	24		30		35	
t _{PLH} / t _{PHL}	Propagation Delay Time E ₂ to \bar{Y}_n		2.0		55	140		180		220	ns
			4.5		17	28		35		42	
			6.0		14	24		30		35	
t _{PLH} / t _{PHL}	Propagation Delay Time LE to \bar{Y}_n		2.0		75	180		225		280	ns
			4.5		22	36		45		55	
			6.0		19	31		40		46	
t _{TLH} / t _{THL}	Output Transition Time		2.0		38	75		95		110	ns
			4.5		7	15		19		22	
			6.0		6	13		16		19	

Timing Requirements HCT: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER		V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HCT137		GD54HCT137		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_w	Pulse width	\overline{LE} to CLK	4.5	26			33		39		ns
t_{su}	Setup time	A_n before \overline{LE}	4.5	15			19		23		ns
t_h	Hold time	A_n after \overline{LE}	4.5	5			5		5		ns

AC Characteristics for HCT: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HCT137		GD54HCT137		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
$t_{PLH}/$ t_{PHL}	Propagation Delay Time A, B, C to \overline{Y}_n	4.5		25	36		45		55	ns
$t_{PLH}/$ t_{PHL}	Propagation Delay Time E_1 to \overline{Y}_n	4.5		20	29		36		42	ns
$t_{PLH}/$ t_{PHL}	Propagation Delay Time E_2 to \overline{Y}_n	4.5		20	29		36		42	ns
$t_{PLH}/$ t_{PHL}	Propagation Delay Time \overline{LE} to \overline{Y}_n	4.5		30	40		50		61	ns
$t_{TLH}/$ t_{THL}	Output Transition Time	4.5		8	15		19		22	ns

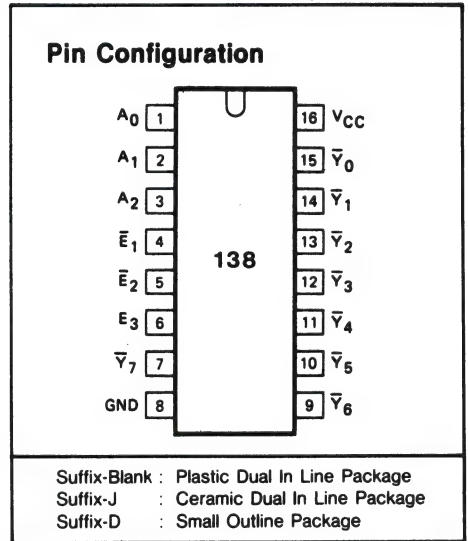
3-TO-8 LINE DECODER/DEMULTIPLEXER

General Description

These devices are identical in pinout to the 54/74LS138. Each device has 3 Binary select (A, B, and C), and decodes A 3-Bit address to 1-of-8 active-LOW outputs. This device features three chip enable inputs. Two active-LOW and one active-HIGH to facilitate the demultiplexing, cascading, and chip-selecting functions. These devices are characterized for operation over wide temperature ranges to meet industry and military specifications

Features

- Low Power consumption characteristic of CMOS devices
- Output drive capability: 10 LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts
for HCT 4.5 to 5.5 volts
- Low input current: $1\mu\text{A}$ Max.
- Low quiescent current: $80\mu\text{A}$ Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs



Function Table

INPUTS						OUTPUTS							
E ₁	E ₂	E ₃	A ₀	A ₁	A ₂	Y ₀	Y ₁	Y ₂	Y ₃	Y ₄	Y ₅	Y ₆	Y ₇
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	L	L	L	L	H	H	H	H	H	H
L	L	H	L	H	L	L	H	H	L	H	H	H	H
L	L	H	H	H	L	L	H	H	H	H	H	H	H
L	L	H	L	L	H	L	H	H	H	L	H	H	H
L	L	H	L	H	H	L	H	H	H	H	L	L	H
L	L	H	H	H	H	L	H	H	H	H	H	L	L

H = HIGH voltage level
L = LOW voltage level
X = don't care

Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC Supply voltage		-0.5	+7	V
I_{IK}, I_{OK}	DC input or output diode current	for $V_I < -0.5$ or $V_I > V_{CC} + 0.5V$		20	mA
I_O	DC output source or sink current	for $-0.5V < V_O < V_{CC} + 0.5V$		25	mA
I_{CC}	DC V_{CC} or GND current			50	mA
T_{stg}	Storage temperature range		-65	150	°C
P_D	Power dissipation per package	above +70°C: derate linearly with 8mW/K		500	mW
T_L	Lead temperature	At distance 1/16 ± 1/32 in. from case for 60 sec(CERAMIC) 10 sec(PLASTIC)		300 260	°C

Recommended Operating Conditions

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range V_{CC} : GD54/74HC Types GD54/74HCT Types	2 4.5	6 5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A : GD74 Types GD54 Types	-40 -55	+85 +125	°C
Input Rise and Fall times t_r, t_f : GD54/74HC Types at 2V at 4.5V at 6V GD54/74HCT Types at 4.5V		1000 500 400 500	ns

Logic Diagram

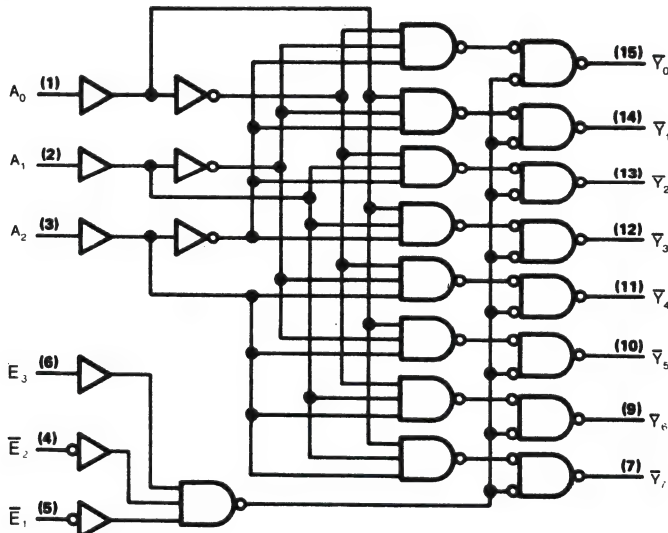


Fig. 1 Logic diagram

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HC138		GD54HC138		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2		1.5 3.15 4.2		V
V _{IL}	LOW level input voltage		2.0 4.5 6.0			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH}	I _{OH} =-20μA	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0	1.9 4.4 5.9		1.9 4.4 5.9		V
		or V _{IL}	I _{OH} =-4mA I _{OH} =-5.2mA	4.5 6.0	3.98 5.48	4.3 5.2	3.84 5.34		3.7 5.2		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH}	I _{OL} =20μA	2.0 4.5 6.0			0.1 0.1 0.1	0.1 0.1 0.1		0.1 0.1 0.1	V
		or V _{IL}	I _{OL} =4mA I _{OL} =5.2mA	4.5 6.0		0.17 0.15	0.26 0.26	0.33 0.33		0.4 0.4	
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	6.0			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	6.0			8		80		160	μA

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HCT138		GD54HCT138		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		4.5 to 5.5	2.0			2.0		2.0		V
V _{IL}	LOW level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH}	I _{OH} =-20μA	4.5	4.4	4.5	4.4		4.4		V
		or V _{IL}	I _{OH} =-4mA	4.5	3.98	4.3	3.84		3.7		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH}	I _{OL} =20μA	4.5		0.1	0.1		0.1		V
		or V _{IL}	I _{OL} =4mA	4.5		0.17	0.26	0.33	0.4		
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	5.5			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	5.5			8		80		160	μA

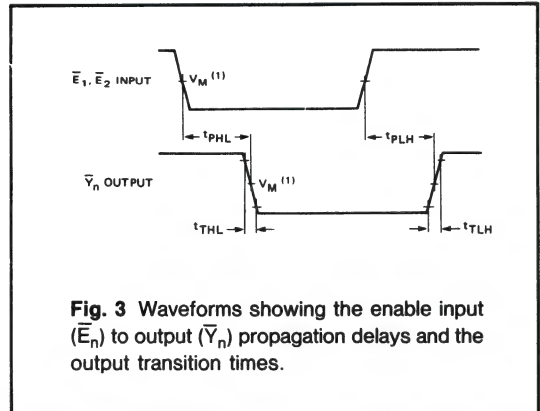
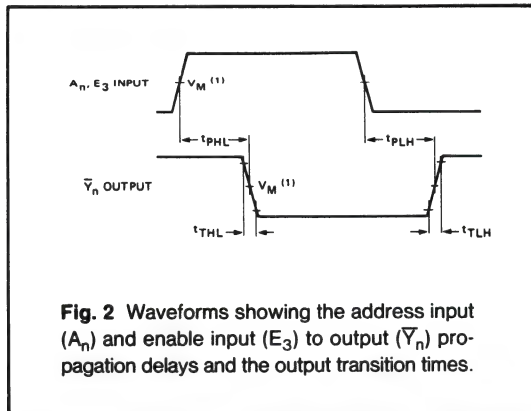
AC Characteristics for HC: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HC138		GD54HC138		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} / t_{PHL}	Propagation Delay Time A_n, E_3 to \bar{Y}_n	2.0 4.5 6.0		40 15 12	150 30 26		190 38 33		225 45 38	ns
t_{PLH} / t_{PHL}	Propagation Delay Time \bar{E}_1, \bar{E}_2 to \bar{Y}_n	2.0 4.5 6.0		40 15 12	150 34 32		190 38 33		225 45 38	ns
t_{TLH} / t_{THL}	Output Transition Time	2.0 4.5 6.0		19 7 6	75 15 13		95 19 16		110 22 19	ns

AC Characteristics for HCT: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HCT138		GD54HCT138		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} / t_{PHL}	Propagation Delay Time A_n, E_3 to \bar{Y}_n	4.5		19	34		43		52	ns
t_{PLH} / t_{PHL}	Propagation Delay Time \bar{E}_1, \bar{E}_2 to \bar{Y}_n	4.5		18	40		50		60	ns
t_{TLH} / t_{THL}	Output Transition Time	4.5		7	15		19		22	ns

AC Waveforms



Note to AC waveforms

- (1) HC : $V_M=50\%$; $V_I=\text{GND}$ to V_{CC} .
HCT : $V_M=1.3\text{V}$; $V_I=\text{GND}$ to 3V .

GD54/74HC139, GD54/74HCT139

DUAL 2-TO-4 LINE DECODER/DEMULTIPLEXER

General Description

These devices are identical in pinout to the 54/74LS139. They contain two independent 1-of-4 decoders each with a single active-low enable input. Each circuit decodes a 2-bit address to 1-of-4 active-low outputs. Data on the select inputs (A, B) cause one of the four normally high outputs to go low. These devices are characterized for operation over wide temperature ranges to meet industry and military specifications.

Features

- Low Power consumption characteristic of CMOS devices
- Output drive capability: 10 LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts
for HCT 4.5 to 5.5 volts
- Low input current: $1\mu\text{A}$ Max.
- Low quiescent current: $80\mu\text{A}$ Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs

Logic Diagram

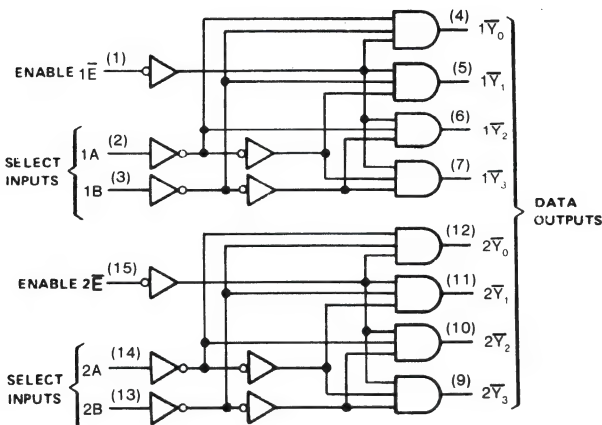
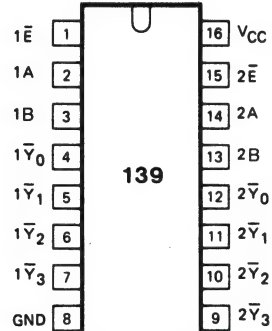


Fig. 1 Logic diagram.

Pin Configuration



Suffix-Blank : Plastic Dual In Line Package
 Suffix-J : Ceramic Dual In Line Package
 Suffix-D : Small Outline Package

Function Table

INPUTS			OUTPUTS			
$n\bar{E}$	nA	nB	$n\bar{Y}_0$	$n\bar{Y}_1$	$n\bar{Y}_2$	$n\bar{Y}_3$
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L

H = HIGH voltage level
 L = LOW voltage level
 X = don't care

Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC Supply voltage		-0.5	+7	V
I_{IK}, I_{OK}	DC input or output diode current	for $V_I < -0.5$ or $V_I > V_{CC} + 0.5V$		20	mA
I_O	DC output source or sink current	for $-0.5V < V_O < V_{CC} + 0.5V$		25	mA
I_{CC}	DC V_{CC} or GND current			50	mA
T_{sig}	Storage temperature range		-65	150	°C
P_D	Power dissipation per package	above +70°C: derate linearly with 8mW/K		500	mW
T_L	Lead temperature	At distance 1/16 ± 1/32 in. from case for 60 sec(CERAMIC) 10 sec(PLASTIC)		300 260	°C

Recommended Operating Conditions

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range V_{CC} : GD54/74HC Types GD54/74HCT Types	2 4.5	6 5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A : GD74 Types GD54 Types	-40 -55	+85 +125	°C
Input Rise and Fall times t_r, t_f : GD54/74HC Types at 2V at 4.5V at 6V GD54/74HCT Types at 4.5V		1000 500 400 500	ns

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HC139		GD54HC139		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2		1.5 3.15 4.2		V
V _{IL}	LOW level input voltage		2.0 4.5 6.0			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH} or V _{IL}									V
			I _{OH} =-20μA	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0	1.9 4.4 5.9		1.9 4.4 5.9		
			I _{OH} =-4mA I _{OH} =-5.2mA	4.5 6.0	3.98 5.48	4.3 5.2	3.84 5.34		3.7 5.2		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH} or V _{IL}									V
			I _{OL} =20μA	2.0 4.5 6.0			0.1 0.1 0.1		0.1 0.1 0.1		
			I _{OL} =4mA I _{OL} =5.2mA	4.5 6.0		0.17 0.15	0.26 0.26		0.33 0.33		
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	6.0			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	6.0			8		80		160	μA

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HCT139		GD54HCT139		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		4.5 to 5.0	2.0			2.0		2.0		V
V _{IL}	LOW level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH} or V _{IL}									V
			I _{OH} =-20μA	4.5	4.4	4.5	4.4		4.4		
			I _{OH} =-4mA	4.5	3.98	4.3	3.84		3.7		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH} or V _{IL}									V
			I _{OL} =20μA	4.5			0.1		0.1		
			I _{OL} =4mA	4.5		0.17	0.26		0.33		
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	5.5			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	5.5			8		80		160	μA

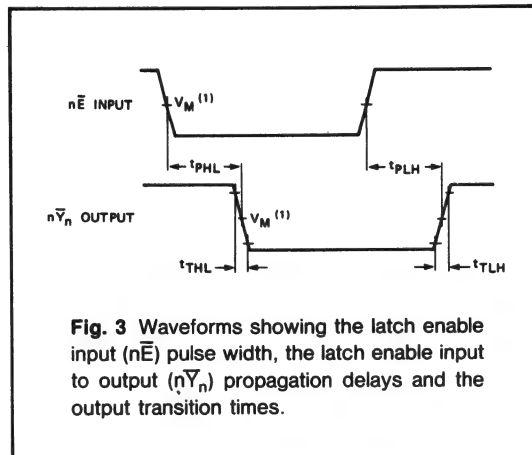
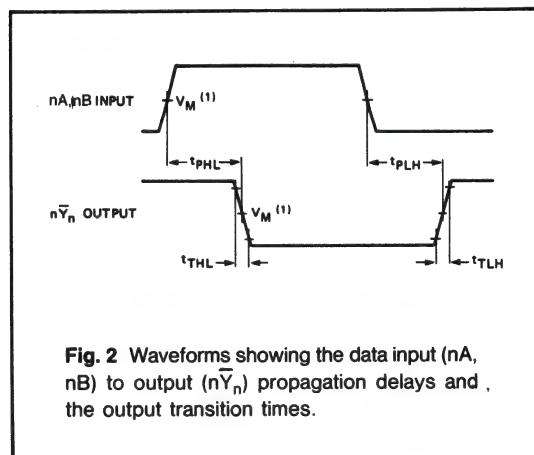
AC Characteristics for HC, $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HC139		GD54HC139		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} / t_{PHL}	Propagation Delay Time nA, nB to $n\bar{Y}_n$	2.0		38	145		180		220	ns
		4.5		13	29		36		44	
		6.0		10	25		31		38	
t_{PLH} / t_{PHL}	Propagation Delay Time $n\bar{E}$ to $n\bar{Y}_n$	2.0		33	135		170		205	ns
		4.5		12	27		34		41	
		6.0		10	23		29		35	
t_{TLH} / t_{THL}	Output Transition Time	2.0		19	75		95		110	ns
		4.5		7	15		19		22	
		6.0		6	13		16		19	

AC Characteristics for HCT: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HCT139		GD54HCT139		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} / t_{PHL}	Propagation Delay Time nA, nB to $n\bar{Y}_n$	4.5		16	34		43		51	ns
t_{PLH} / t_{PHL}	Propagation Delay Time $n\bar{E}$ to $n\bar{Y}_n$	4.5		16	34		43		51	ns
t_{TLH} / t_{THL}	Output Transition Time	4.5		7	15		19		22	ns

AC Waveforms



Note to AC waveforms

- (1) HC : $V_M=50\%$; $V_I=GND$ to V_{CC} .
HCT: $V_M=1.3V$; $V_I=GND$ to $3V$.

GD54/74HC147, GD54/74HCT147

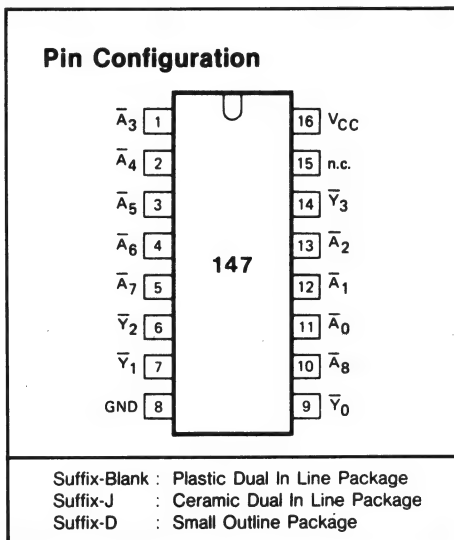
10-TO-4 LINE (DECIMAL-TO-BCD) PRIORITY ENCODER

General Description

These devices are identical in pinout to the 54/74LS147. This encoder features priority encoding of the inputs to ensure that only the highest input lines are encoded to a four active-low BCD coded when all nine data inputs are at a high logic level. The implied decimal zero condition is encoded when all nine data inputs are at a high logic level (inactive). These devices are characterized for operation over wide temperature ranges to meet industry and military specifications

Features

- Low Power consumption characteristic of CMOS devices
- Output drive capability: 10 LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts
for HCT 4.5 to 5.5 volts
- Low input current: $1\mu\text{A}$ Max.
- Low quiescent current: $80\mu\text{A}$ Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs



Function Table

INPUTS									OUTPUTS			
\bar{A}_0	\bar{A}_1	\bar{A}_2	\bar{A}_3	\bar{A}_4	\bar{A}_5	\bar{A}_6	\bar{A}_7	\bar{A}_8	\bar{Y}_3	\bar{Y}_2	\bar{Y}_1	\bar{Y}_0
H	H	H	H	H	H	H	H	H	H	H	H	H
X	X	X	X	X	X	X	X	L	L	H	H	L
X	X	X	X	X	X	X	L	H	L	H	H	H
X	X	X	X	X	X	L	H	H	H	L	L	L
X	X	X	X	X	L	H	H	H	H	L	L	H
X	X	X	X	L	H	H	H	H	H	L	H	L
X	X	X	L	H	H	H	H	H	H	L	H	L
X	X	L	H	H	H	H	H	H	H	H	L	L
X	L	H	H	H	H	H	H	H	H	H	L	H
L	H	H	H	H	H	H	H	H	H	H	H	L

H = HIGH voltage level
 L = LOW voltage level
 X = don't care

Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC Supply voltage		-0.5	+7	V
I_{IK}, I_{OK}	DC input or output diode current	for $V_I < -0.5$ or $V_I > V_{CC} + 0.5V$		20	mA
I_O	DC output source or sink current	for $-0.5V < V_O < V_{CC} + 0.5V$		25	mA
I_{CC}	DC V_{CC} or GND current			50	mA
T_{stg}	Storage temperature range		-65	150	°C
P_D	Power dissipation per package	above +70°C: derate linearly with 8mW/K		500	mW
T_L	Lead temperature	At distance 1/16 ± 1/32 in. from case for 60 sec(CERAMIC) 10 sec(PLASTIC)		300 260	°C

Recommended Operating Conditions

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range V_{CC} : GD54/74HC Types GD54/74HCT Types	2 4.5	6 5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A : GD74 Types GD54 Types	-40 -55	+85 +125	°C
Input Rise and Fall times t_r, t_f : GD54/74HC Types at 2V at 4.5V at 6V GD54/74HCT Types at 4.5V		1000 500 400 500	ns

Logic Diagram

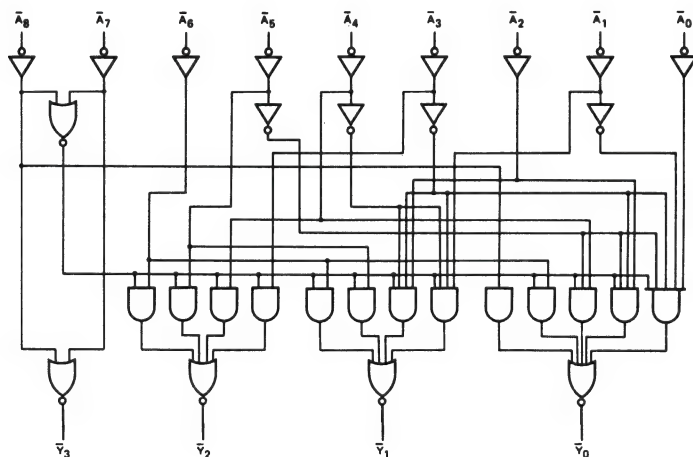


Fig. 1 Logic diagram

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A = 25°C			GD74HC147		GD54HC147		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2		1.5 3.15 4.2		V
V _{IL}	LOW level input voltage		2.0 4.5 6.0			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V
V _{OH}	HIGH level output voltage	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -20μA	2.0	1.9	2.0	1.9		1.9		V
				4.5	4.4	4.5	4.4		4.4		
			I _{OH} = -4mA I _{OH} = -5.2mA	6.0	5.9	6.0	5.9		5.9		
				4.5	3.98	4.3	3.84		3.7		
V _{OL}	LOW level output voltage	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 20μA	2.0			0.1		0.1		V
				4.5			0.1		0.1		
			I _{OL} = 4mA I _{OL} = 5.2mA	6.0			0.1		0.1		
				4.5	0.17	0.26	0.33		0.4		
I _{IN}	Input leakage Current	V _{IN} = V _{CC} or GND	6.0			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} = V _{CC} or GND I _{out} = 0μA	6.0			8		80		160	μA

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A = 25°C			GD74HCT147		GD54HCT147		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		4.5 to 5.0	2.0			2.0		2.0		V
V _{IL}	LOW level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V _{OH}	HIGH level output voltage	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -20μA	4.5	4.4	4.5	4.4		4.4		V
				4.5	3.98	4.3	3.84		3.7		
			I _{OH} = -4mA	4.5							
				4.5							
V _{OL}	LOW level output voltage	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 20μA	4.5			0.1		0.1		V
				4.5							
			I _{OL} = 4mA	4.5		0.17	0.26		0.33		
				4.5						0.4	
I _{IN}	Input leakage Current	V _{IN} = V _{CC} or GND	5.5			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} = V _{CC} or GND I _{out} = 0μA	5.5			8		80		160	μA

AC Characteristics for HC: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HC147		GD54HC147		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
$t_{PLH}/$ t_{PHL}	Propagation delay time \bar{A}_n to \bar{Y}_n	2.0 4.5 6.0		50 18 14	160 32 27		200 40 34		240 48 41	ns
$t_{TLH}/$ t_{THL}	Output transition time	2.0 4.5 6.0		19 7 6	75 15 13		95 19 16		110 22 19	ns

AC Characteristics for HCT: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HCT147		GD54HCT147		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
$t_{PLH}/$ t_{PHL}	Propagation delay time \bar{A}_n to \bar{Y}_n	4.5		20	35		44		53	ns
$t_{TLH}/$ t_{THL}	Output transition time	4.5		7	15		19		22	ns

AC Waveform

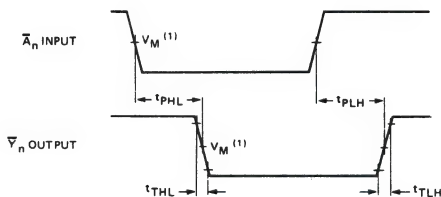


Fig. 2 Waveforms showing the decimal data inputs (\bar{A}_n) to output (\bar{Y}_n) propagation delays and the output transition times.

Note to AC waveform

(1) HC : $V_M=50\%$; $V_i=\text{GND}$ to V_{CC} .
HCT: $V_M=1.3\text{V}$; $V_i=\text{GND}$ to 3V .

GD54/74HC148, GD54/74HCT148

8-TO-3 LINE PRIORITY ENCODER

General Description

These devices are identical in pinout to the 54/74LS148. This encoder features priority encoding of the inputs to ensure that only the highest order data line is encoded. Eight active-low data input lines are encoded to three active-Low binary outputs (octal). Cascading circuitry (enable input EI & enable output EO) has been provided to allow octal expansion without the need for external circuitry.

Features

- Low Power consumption characteristic of CMOS devices
- Output drive capability: 10 LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts
for HCT 4.5 to 5.5 volts
- Low input current: $1\mu\text{A}$ Max.
- Low quiescent current: $80\mu\text{A}$ Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs

Logic Diagram

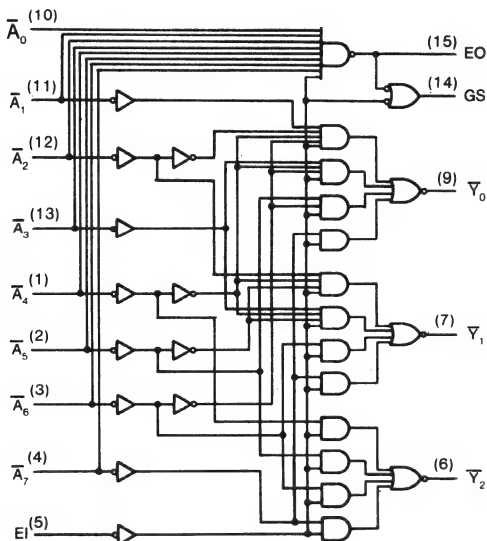
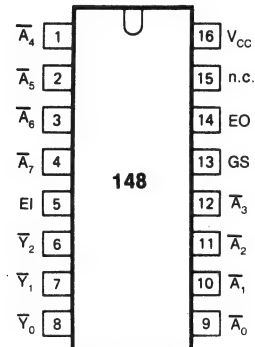


Fig. 1 Logic diagram

Pin Configuration



Suffix-Blank : Plastic Dual In Line Package
 Suffix-J : Ceramic Dual In Line Package
 Suffix-D : Small Outline Package

Function Table

INPUTS									OUTPUTS				
EI	\bar{A}_0	\bar{A}_1	\bar{A}_2	\bar{A}_3	\bar{A}_4	\bar{A}_5	\bar{A}_6	\bar{A}_7	\bar{Y}_2	\bar{Y}_1	\bar{Y}_0	GS	EO
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	L	H
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	L	H	H	L	H	L	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	H	L	L	L	H
L	X	X	L	H	H	H	H	H	H	L	L	L	H
L	X	L	H	H	H	H	H	H	H	H	L	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L	H

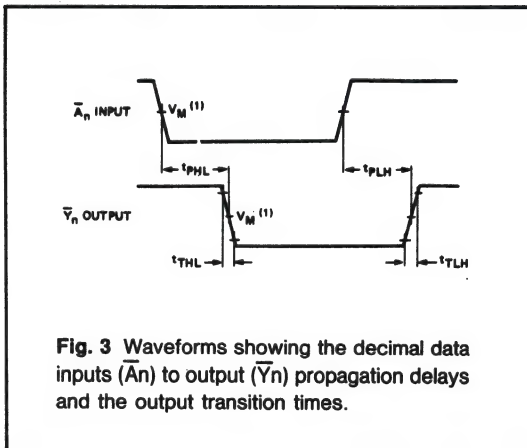
Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC Supply voltage		-0.5	+7	V
I_{IK}, I_{OK}	DC input or output diode current	for $V_I < -0.5$ or $V_I > V_{CC} + 0.5V$		20	mA
I_O	DC output source or sink current	for $-0.5V < V_O < V_{CC} + 0.5V$		25	mA
I_{CC}	DC V_{CC} or GND current			50	mA
T_{stg}	Storage temperature range		-65	150	°C
P_D	Power dissipation per package	above +70°C: derate linearly with 8mW/K		500	mW
T_L	Lead temperature	At distance $1/16 \pm 1/32$ in. from case for 60 sec(CERAMIC) 10 sec(PLASTIC)		300 260	°C

Recommended Operating Conditions

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range V_{CC} : GD54/74HC Types GD54/74HCT Types	2 4.5	6 5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A : GD74 Types GD54 Types	-40 -55	+85 +125	°C
Input Rise and Fall times t_r, t_f : GD54/74HC Types at 2V at 4.5V at 6V GD54/74HCT Types at 4.5 V		1000 500 400 500	ns

AC Waveform



Note to AC waveform

- (1) HC : $V_M = 50\%$; $V_I = \text{GND to } V_{CC}$.
HCT : $V_M = 1.3V$; $V_I = \text{GND to } 3V$.

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HC148		GD54HC148		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2		1.5 3.15 4.2		V
V _{IL}	LOW level input voltage		2.0 4.5 6.0			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH} or V _{IL}	I _{OH} =-20μA	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0	1.9 4.4 5.9		1.9 4.4 5.9		V
			I _{OH} =-4mA I _{OH} =-5.2mA	4.5 6.0	3.98 5.48	4.3 5.2	3.84 5.34		3.7 5.2		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH} or V _{IL}	I _{OL} =20μA	2.0 4.5 6.0			0.1 0.1 0.1	0.1 0.1 0.1		0.1 0.1 0.1	V
			I _{OL} =4mA I _{OL} =5.2mA	4.5 6.0		0.17 0.15	0.26 0.26	0.33 0.33		0.4 0.4	
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	6.0			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	6.0			8		80		160	μA

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HCT148		GD54HCT148		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		4.5 to 5.5	2.0			2.0		2.0		V
V _{IL}	LOW level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH} or V _{IL}	I _{OH} =-20μA	4.5	4.4	4.5	4.4		4.4		V
			I _{OH} =-4mA	4.5	3.98	4.3	3.84		3.7		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH} or V _{IL}	I _{OL} =20μA	4.5			0.1	0.1		0.1	V
			I _{OL} =4mA	4.5		0.17	0.26	0.33		0.4	
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	5.5			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	5.5			8		80		160	μA

AC Characteristics for HC: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HC148		GD54HC148		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
$t_{PLH}/$ t_{PHL}	Propagation Delay Time \bar{A}_n to \bar{Y}_n	2.0		50	160		210		250	ns
		4.5		20	34		43		50	
		6.0		17	29		36		41	
$t_{PLH}/$ t_{PHL}	Propagation Delay Time \bar{A}_n to EO	2.0		45	130		180		210	ns
		4.5		17	27		36		41	
		6.0		15	23		31		34	
$t_{PLH}/$ t_{PHL}	Propagation Delay Time \bar{A}_n to GS	2.0		60	180		230		270	ns
		4.5		22	36		46		54	
		6.0		18	30		39		45	
$t_{PLH}/$ t_{PHL}	Propagation Delay Time EI to $n\bar{Y}$	2.0		75	190		240		280	ns
		4.5		23	37		46		55	
		6.0		20	31		39		45	
$t_{PLH}/$ t_{PHL}	Propagation Delay Time EI to GS	2.0		45	130		180		210	ns
		4.5		17	27		36		41	
		6.0		15	23		31		34	
$t_{PLH}/$ t_{PHL}	Propagation Delay Time EI to EO	2.0		50	160		210		250	ns
		4.5		19	33		43		50	
		6.0		17	28		36		41	
$t_{TLH}/$ t_{THL}	Output Transition Time	2.0		28	75		95		110	ns
		4.5		7	15		19		22	
		6.0		6	13		16		19	

AC Characteristics for HCT: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HCT148		GD54HCT148		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
$t_{PLH}/$ t_{PHL}	Propagation Delay Time \bar{A}_n to \bar{Y}_n	4.5		24	36		46		54	ns
$t_{PLH}/$ t_{PHL}	Propagation Delay Time \bar{A}_n to EO	4.5		21	30		40		45	ns
$t_{PLH}/$ t_{PHL}	Propagation Delay Time \bar{A}_n to GS	4.5		26	40		50		58	ns
$t_{PLH}/$ t_{PHL}	Propagation Delay Time EI to $n\bar{Y}$	4.5		27	41		50		59	ns
$t_{PLH}/$ t_{PHL}	Propagation Delay Time EI to GS	4.5		21	31		40		45	ns
$t_{PLH}/$ t_{PHL}	Propagation Delay Time EI to EO	4.5		23	37		47		54	ns
$t_{TLH}/$ t_{THL}	Output Transition Time	4.5		7	15		19		22	ns

GD54/74HC151, GD54/74HCT151

8-TO-1 LINE DATA SELECTOR/MULTIPLEXER

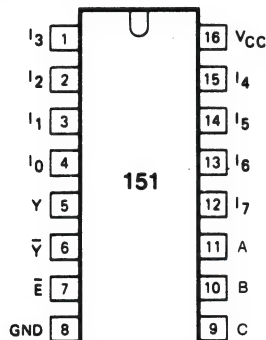
General Description

These devices are identical in pinout to the 54/74LS151. This circuit selects one of the 8 binary data inputs, depending on the address presented on the A, B, and C inputs. It features both true(Y) and complementary(\bar{Y}) outputs. The enable input must be at a low logic level to enable the multiplexing. A high logic level at the enable pin forces the Y output high and the \bar{Y} output low. The HC/HCT 151 is similar in function to the HC/HCT 251 which has 3-state outputs. These devices are characterized for operation over wide temperature ranges to meet industry and military specifications.

Features

- Low Power consumption characteristic of CMOS devices
- Output drive capability: 10 LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts
for HCT 4.5 to 5.5 volts
- Low input current: 1 μ A Max.
- Low quiescent current: 80 μ A Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs

Pin Configuration



Suffix-Blank : Plastic Dual In Line Package
 Suffix-J : Ceramic Dual In Line Package
 Suffix-D : Small Outline Package

Function Table

INPUTS													OUTPUTS	
E	C	B	A	I ₀	I ₁	I ₂	I ₃	I ₄	I ₅	I ₆	I ₇	Y	Y	
H	X	X	X	X	X	X	X	X	X	X	X	H	L	
L	L	L	L	L	X	X	X	X	X	X	X	H	L	
L	L	L	L	H	X	X	X	X	X	X	X	L	H	
L	L	L	H	X	L	X	X	X	X	X	X	H	L	
L	L	L	H	X	H	X	X	X	X	X	X	L	H	
L	L	H	L	X	X	L	X	X	X	X	X	H	L	
L	L	H	L	X	X	H	X	X	X	X	X	L	H	
L	L	H	H	X	X	X	L	X	X	X	X	H	L	
L	L	H	H	X	X	X	X	L	X	X	X	L	H	
L	L	H	H	X	X	X	X	H	X	X	X	H	L	
L	H	L	L	X	X	X	X	L	X	X	X	H	L	
L	H	L	L	X	X	X	X	H	X	X	X	L	H	
L	H	L	H	X	X	X	X	L	X	X	X	H	L	
L	H	L	H	X	X	X	X	H	X	X	X	L	H	
L	H	H	L	X	X	X	X	X	L	X	X	H	L	
L	H	H	L	X	X	X	X	X	H	X	X	L	H	
L	H	H	H	X	X	X	X	X	X	X	X	L	H	
L	H	H	H	X	X	X	X	X	X	X	H	L	H	

H = HIGH voltage level
 L = LOW voltage level
 X = don't care

Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC Supply voltage		-0.5	+7	V
I_{IK}, I_{OK}	DC input or output diode current	for $V_I < -0.5$ or $V_I > V_{CC} + 0.5V$		20	mA
I_O	DC output source or sink current	for $-0.5V < V_O < V_{CC} + 0.5V$		35	mA
I_{CC}	DC V_{CC} or GND current			30	mA
T_{stg}	Storage temperature range		-65	150	°C
P_D	Power dissipation per package	above +70°C: derate linearly with 8mW/K		500	mW
T_L	Lead temperature	At distance $1/16 \pm 1/32$ in. from case for 60 sec(CERAMIC) 10 sec(PLASTIC)		300 260	°C

Recommended Operating Conditions

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range V_{CC} : GD54/74HC Types GD54/74HCT Types	2 4.5	6 5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A : GD74 Types GD54 Types	-40 -55	+85 +125	°C
Input Rise and Fall times t_r, t_f : GD54/74HC Types at 2V at 4.5V at 6V GD54/74HCT Types at 4.5V		1000 500 400 500	ns

Logic Diagram

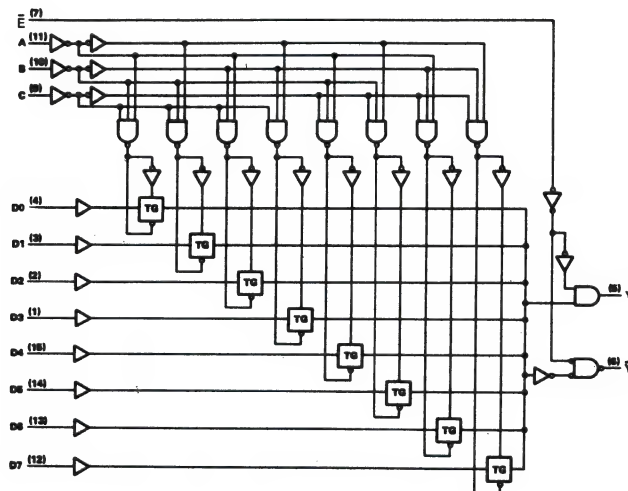


Fig. 1 Logic diagram

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HC151		GD54HC151		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2		1.5 3.15 4.2		V
V _{IL}	LOW level input voltage		2.0 4.5 6.0			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH}	I _{OH} =-20μA	2.0	1.9	2.0	1.9		1.9		V
				4.5	4.4	4.5	4.4		4.4		
		or V _{IL}	I _{OH} =-4mA I _{OH} =-5.2mA	6.0	5.9	6.0	5.9		5.9		
				4.5	3.98	4.3	3.84		3.7		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH}	I _{OL} =20μA	2.0			0.1		0.1		V
				4.5			0.1		0.1		
		or V _{IL}	I _{OL} =4mA I _{OL} =5.2mA	6.0			0.1		0.1		
				4.5		0.17	0.26		0.33		
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	6.0			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	6.0			8		80		160	μA

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HCT151		GD54HCT151		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		4.5 to 5.5	2.0			2.0		2.0		V
V _{IL}	LOW level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH}	I _{OH} =-20μA	4.5	4.4	4.5	4.4		4.4		V
		or V _{IL}	I _{OH} =-4mA	4.5	3.98	4.3	3.84		3.7		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH}	I _{OL} =20μA	4.5			0.1		0.1		V
		or V _{IL}	I _{OL} =4mA	4.5		0.17	0.26		0.33		
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	5.5			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	5.5			8		80		160	μA

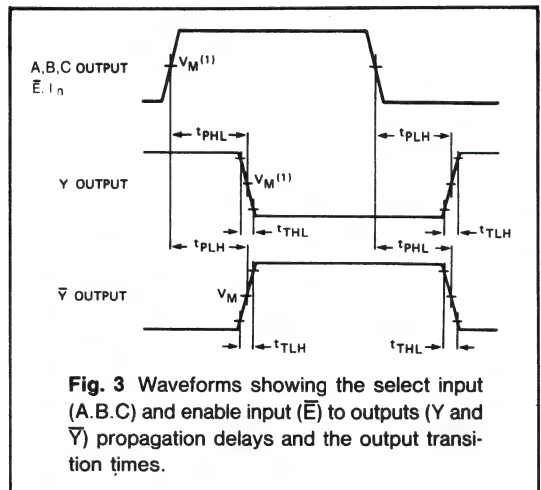
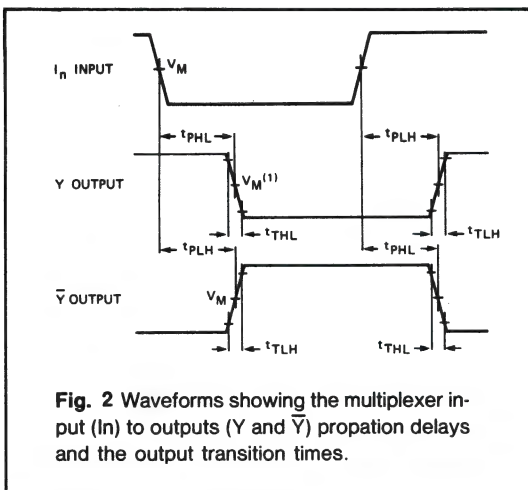
AC Characteristics for HC: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER V_{CC}	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HC151		GD54HC151		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
$t_{PLH}/$ t_{PHL}	Propagation Delay Time A,B,C to Y, \bar{Y}	2.0 4.5 6.0		52 19 15	170 34 29		215 43 37		255 51 43	ns
$t_{PLH}/$ t_{PHL}	Propagation Delay Time In to Y, \bar{Y}	2.0 4.5 6.0		52 19 15	170 34 29		215 43 37		225 51 43	ns
$t_{PLH}/$ t_{PHL}	Propagation Delay Time \bar{E} to Y, \bar{Y}	2.0 4.5 6.0		41 15 12	145 29 25		180 36 31		220 44 38	ns
$t_{TLH}/$ t_{THL}	Output Transition Time	2.0 4.5 6.0		19 7 6	75 15 13		95 19 16		110 22 19	ns

AC Characteristics for HCT: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HCT151		GD54HCT151		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
$t_{PLH}/$ t_{PHL}	Propagation Delay Time A,B,C to Y, \bar{Y}	4.5		20	38		48		57	ns
$t_{PLH}/$ t_{PHL}	Propagation Delay Time In to Y, \bar{Y}	4.5		20	38		44		57	ns
$t_{PLH}/$ t_{PHL}	Propagation Delay Time \bar{E} to Y, \bar{Y}	4.5		21	40		51		62	ns
$t_{TLH}/$ t_{THL}	Output Transition Time	4.5		7	15		19		22	ns

AC Waveforms



Note to AC waveforms

- (1) HC : $V_M=50\%$; $V_i=\text{GND to } V_{CC}$.
HCT : $V_M=1.3\text{V}$; $V_i=\text{GND to } 3\text{V}$.

GD54/74HC153, GD54/74HCT153

DUAL 4-TO-1 LINE SELECTORS/MULTIPLEXERS

General Description

These devices are identical in pinout to the 54/74LS153. They contain two multiplexers, where each multiplexer is selected by two-bit address. Each multiplexer has a select input which enables it when taken to a low logic level. When a high logic level is applied to a select input, the output of its associated multiplexer is taken low. The HC/HCT 153 is similar in function to the HC/HCT 253 which has 3-state outputs. These devices are characterized for operation over wide temperature ranges to meet industry and military specifications.

Features

- Low Power consumption characteristic of CMOS devices
- Output drive capability: 10 LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts
for HCT 4.5 to 5.5 volts
- Low input current: 1 μ A Max.
- Low quiescent current: 80 μ A Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs

Logic Diagram

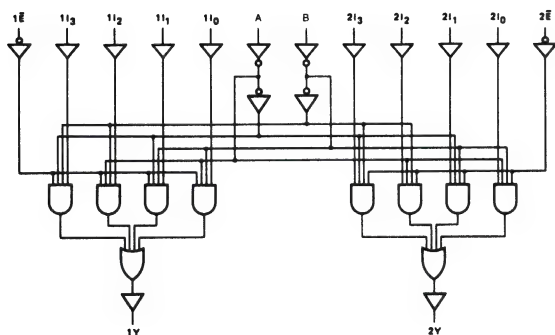
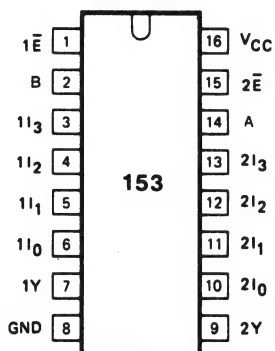


Fig. 1 Logic diagram

Pin Configuration



Suffix-Blank : Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package
Suffix-D : Small Outline Package

Function Table

SELECT INPUTS		DATA INPUTS				OUTPUT ENABLE	OUTPUT
A	B	nI ₀	nI ₁	nI ₂	nI ₃	n \bar{E}	nY
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
H	L	X	L	X	X	L	L
H	L	X	H	X	X	L	H
L	H	X	X	L	X	L	L
L	H	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

H=HIGH voltage level
L=LOW voltage level
X=don't care

Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC Supply voltage		-0.5	+7	V
I_{IK}, I_{OK}	DC input or output diode current	for $V_I < -0.5$ or $V_I > V_{CC} + 0.5V$		20	mA
I_O	DC output source or sink current	for $-0.5V < V_O < V_{CC} + 0.5V$		25	mA
I_{CC}	DC V_{CC} or GND current			50	mA
T_{stg}	Storage temperature range		-65	150	°C
P_D	Power dissipation per package	above +70°C: derate linearly with 8mW/K		500	mW
T_L	Lead temperature	At distance 1/16 ± 1/32 in. from case for 60 sec(CERAMIC) 10 sec(PLASTIC)		300 260	°C

Recommended Operating Conditions

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range V_{CC} : GD54/74HC Types GD54/74HCT Types	2 4.5	6 5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A : GD74 Types GD54 Types	-40 -55	+85 +125	°C
Input Rise and Fall times t_r, t_f : GD54/74HC Types at 2V at 4.5V at 6V GD54/74HCT Types at 4.5 V		1000 500 400 500	ns

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HC153		GD54HC153		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2		1.5 3.15 4.2		V
V _{IL}	LOW level input voltage		2.0 4.5 6.0			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH}	I _{OH} =-20μA	2.0	1.9	2.0		1.9		1.9	V
				4.5	4.4	4.5		4.4		4.4	
		or V _{IL}	I _{OH} =-4mA I _{OH} =-5.2mA	6.0	5.9	6.0		5.9		5.9	
				4.5	3.98	4.3		3.84		3.7	
V _{OL}	LOW level output voltage	V _{IN} =V _{IH}	I _{OL} =20μA	2.0			0.1	0.1		0.1	V
				4.5			0.1	0.1		0.1	
		or V _{IL}	I _{OL} =4mA I _{OL} =5.2mA	6.0			0.1	0.1		0.1	
				4.5		0.17	0.26	0.33		0.4	
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	6.0			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	6.0			8		80		160	μA

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HCT153		GD54HCT153		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		4.5 to 5.5	2.0			2.0		2.0		V
V _{IL}	LOW level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH}	I _{OH} =-20μA	4.5	4.4	4.5		4.4		4.4	V
				4.5	3.98	4.3		3.84		3.7	
		or V _{IL}	I _{OH} =-4mA	4.5							
				4.5							
V _{OL}	LOW level output voltage	V _{IN} =V _{IH}	I _{OL} =20μA	4.5			0.1	0.1		0.1	V
				4.5			0.1	0.1		0.1	
		or V _{IL}	I _{OL} =4mA	4.5		0.17	0.26	0.33		0.4	
				4.5		0.17	0.26	0.33		0.4	
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	5.5			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	5.5			8		80		160	μA

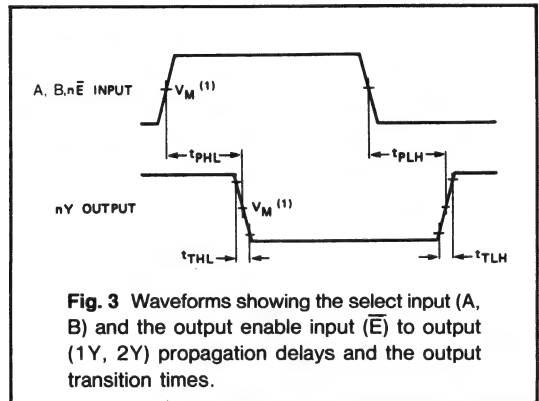
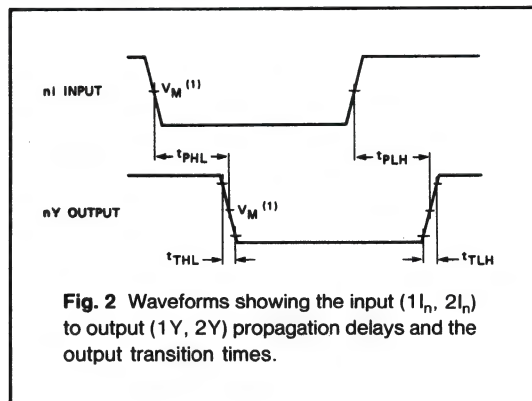
AC Characteristics for HC: $t_r=t_f=6\text{ns}$ $C_L=05\text{ pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HC153		GD54HC153		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} / t_{PHL}	Propagation Delay Time A or B to nY	2.0 4.5 6.0		50 18 14	150 30 26		190 38 33		225 45 38	ns
t_{PLH} / t_{PHL}	Propagation Delay Time Data (nI_n) to nY	2.0 4.5 6.0		47 17 14	145 29 26		180 36 31		220 44 38	ns
t_{PLH} / t_{PHL}	Propagation Delay Time \bar{E} to nY	2.0 4.5 6.0		33 12 10	100 20 17		125 25 21		150 30 26	ns
t_{TLH} / t_{THL}	Output Transition Time	2.0 4.5 6.0		19 7 6	75 15 13		95 19 16		110 22 19	ns

AC Characteristics for HCT: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HCT153		GD54HCT153		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} / t_{PHL}	Propagation Delay Time A or B to nY	4.5 5.5		18	34		43		51	ns
t_{PLH} / t_{PHL}	Propagation Delay Time Data (nI_n) to nY	4.5 5.5		16	34		43		51	ns
t_{PLH} / t_{PHL}	Propagation Delay Time \bar{E} to nY	4.5 5.5		14	27		34		41	ns
t_{TLH} / t_{THL}	Output Transition Time	4.5 5.5		7	15		19		22	ns

AC Waveforms



GD54/74HC154, GD54/74HCT154

4-TO-16 LINE DECODER/DEMULTIPLEXER

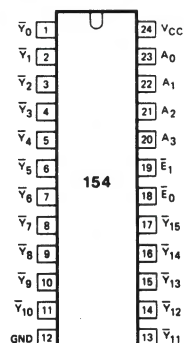
General Description

These devices are identical in pinout to the 54/74LS154. This circuit, when enabled, selects one of 16 active-low outputs according to 4 binary select inputs. Two active-low enables are provided to ease cascading of decoders with little or no external logic. These devices are characterized for operation over wide temperature ranges to meet industry and military specifications

Features

- Low Power consumption characteristic of CMOS devices
- Output drive capability: 10 LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts
for HCT 4.5 to 5.5 volts
- Low input current: 1 μ A Max.
- Low quiescent current: 80 μ A Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs

Pin Configuration



Suffix-Blank : Plastic Dual In Line Package
 Suffix-J : Ceramic Dual In Line Package
 Suffix-D : Small Outline Package

Function Table

		INPUTS				OUTPUTS															
\bar{E}_0	\bar{E}_1	A_0	A_1	A_2	A_3	\bar{Y}_0	\bar{Y}_1	\bar{Y}_2	\bar{Y}_3	\bar{Y}_4	\bar{Y}_5	\bar{Y}_6	\bar{Y}_7	\bar{Y}_8	\bar{Y}_9	\bar{Y}_{10}	\bar{Y}_{11}	\bar{Y}_{12}	\bar{Y}_{13}	\bar{Y}_{14}	\bar{Y}_{15}
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	L	L	L	L	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	L	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L

H=HIGH voltage level

L=LOW voltage level

X=don't care

Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC Supply voltage		-0.5	+7	V
$I_{IK} I_{OK}$	DC input or output diode current	for $V_I < -0.5$ or $V_I > V_{CC} + 0.5V$		20	mA
I_O	DC output source or sink current	for $-0.5V < V_O < V_{CC} + 0.5V$		25	mA
I_{CC}	DC V_{CC} or GND current			50	mA
T_{stg}	Storage temperature range		-65	150	°C
P_D	Power dissipation per package	above +70°C: derate linearly with 8mW/K		500	mW
T_L	Lead temperature	At distance 1/16 ± 1/32 in. from case for 60 sec(CERAMIC) 10 sec(PLASTIC)		300 260	°C

Recommended Operating Conditions

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range V_{CC} : GD54/74HC Types GD54/74HCT Types	2 4.5	6 5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A : GD74 Types GD54 Types	-40 -55	+85 +125	°C
Input Rise and Fall times t_r, t_f : GD54/74HC Types at 2V at 4.5V at 6V GD54/74HCT Types at 4.5V		1000 500 400 500	ns

Logic Diagram

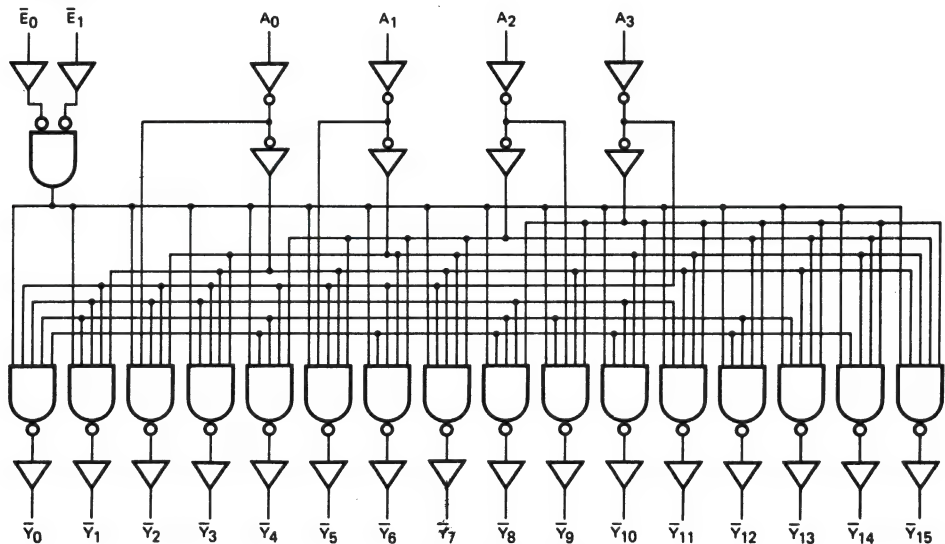


Fig. 1 Logic diagram

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HC154		GD54HC154		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2		1.5 3.15 4.2		V
V _{IL}	LOW level input voltage		2.0 4.5 6.0			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH} or V _{IL}	I _{OH} =-20μA	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0	1.9 4.4 5.9		1.9 4.4 5.9		V
			I _{OH} =-4mA I _{OH} =-5.2mA	4.5 6.0	3.98 5.48	4.3 5.2	3.84 5.34		3.7 5.2		V
V _{OL}	LOW level output voltage	V _{IN} =V _{IH} or V _{IL}	I _{OL} =20μA	2.0 4.5 6.0			0.1 0.1 0.1	0.1 0.1 0.1		0.1 0.1 0.1	V
			I _{OL} =4mA I _{OL} =5.2mA	4.5 6.0		0.17 0.15	0.26 0.26	0.33 0.33		0.4 0.4	V
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	6.0			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	6.0			8		80		160	μA

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HCT154		GD54HCT154		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		4.5 to 5.0	2.0			2.0		2.0		V
V _{IL}	LOW level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH} or V _{IL}	I _{OH} =-20μA	4.5	4.4	4.5	4.4		4.4		V
			I _{OH} =-4mA	4.5	3.98	4.3	3.84		3.7		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH} or V _{IL}	I _{OL} =20μA	4.5		0.1	0.1		0.1		V
			I _{OL} =4mA	4.5		0.17	0.26		0.33		
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	5.5			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	5.5			8		80		160	μA

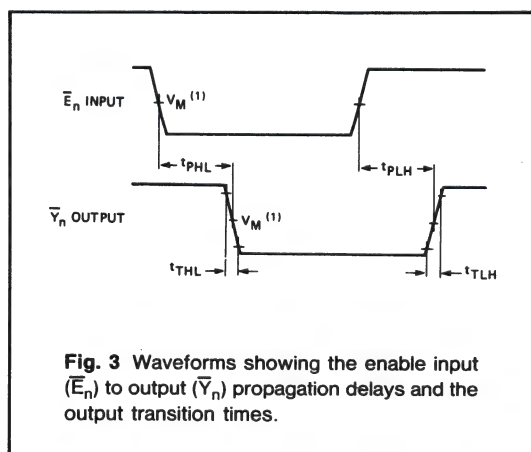
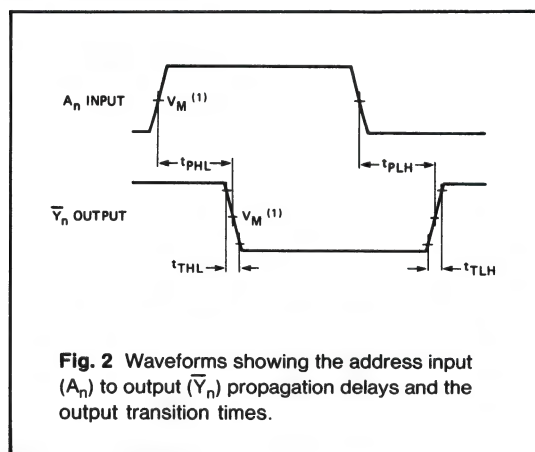
AC Characteristics for HC: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HC154		GD54HC154		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} / t_{PHL}	Propagation Delay Time A_n to \overline{Y}_n	2.0		56	150		190		225	ns
		4.5		18	34		40		47	
		6.0		16	32		36		41	
t_{PLH} / t_{PHL}	Propagation Delay Time \overline{E}_n to \overline{Y}_n	2.0		56	150		190		225	ns
		4.5		18	34		40		47	
		6.0		16	32		36		41	
t_{TLH} / t_{THL}	Output Transition Time	2.0		19	75		95		110	ns
		4.5		7	15		19		22	
		6.0		6	13		16		19	

AC Characteristics for HCT: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HCT154		GD54HCT154		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} / t_{PHL}	Propagation Delay Time A_n to \overline{Y}_n	4.5		22	38		44		51	ns
				22	38		44		51	
t_{PLH} / t_{PHL}	Propagation Delay Time \overline{E}_n to \overline{Y}_n	4.5		22	38		44		51	ns
				22	38		44		51	
t_{TLH} / t_{THL}	Output Transition Time	4.5		7	15		19		22	ns
				7	15		19		22	

AC Waveforms



Note to AC waveforms

- (1) HC : $V_M=50\%$; $V_I=GND$ to V_{CC} .
HCT : $V_M=1.3V$; $V_I=GND$ to $3V$.

GD54/74HC155, GD54/74HCT155

DUAL 2-TO-4 LINE DECODERS/DEMULTIPLEXERS

General Description

These devices are identical in pinout to the 54/74LS155. They contain two 1-to-4 line demultiplexers with individual enable inputs, individual DATA inputs, and common binary address inputs. When both sections are enabled by the enables, the common binary address inputs sequentially select and route associated input data to the appropriate output of each section. Data applied to input 1C is inverted at its outputs and data applied at 2C is not inverted thru its outputs. When two inputs and two enable inputs are connected with each other these circuits can be used as a 3-to-8 line decoder, or 1-to-8 line demultiplexer without external gating.

Features

- Low Power consumption characteristic of CMOS devices
- Output drive capability: 10 LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts
for HCT 4.5 to 5.5 volts
- Low input current: 1μA Max.
- Low quiescent current: 40μA Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs

Function Table

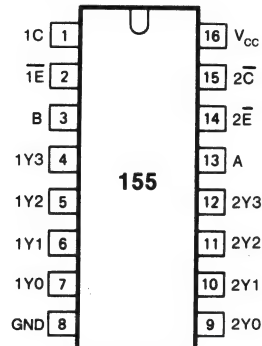
3-LINE-TO-3-LINE DECODER
OR 1-LINE-TO-3-LINE DEMULTIPLEXER

INPUTS		OUTPUTS							
SELECT	ENABLE OR DATA	(0)	(1)	(2)	(3)	(4)	(5)	(6)	(7)
C* B A	E**	2Y0	2Y1	2Y2	2Y3	1Y0	1Y1	1Y2	1Y3
X X X	H	H	H	H	H	H	H	H	H
L L L	L	L	H	H	H	H	H	H	H
L L H	L	H	L	H	H	H	H	H	H
L H L	L	H	H	L	H	H	H	H	H
L H H	L	H	H	H	L	H	H	H	H
H L L	L	H	H	H	H	L	H	H	H
H L H	L	H	H	H	H	H	L	H	H
H H L	L	H	H	H	H	H	H	L	H
H H H	L	H	H	H	H	H	H	H	L

C* = inputs 1C and 2C connected together

E** = inputs 1E and 2E connected together

Pin Configuration



Suffix-Blank : Plastic Dual In Line Package
 Suffix-J : Ceramic Dual In Line Package
 Suffix-D : Small Outline Package

2-LINE-TO-4-LINE DECODER
OR 1-LINE-TO-4-LINE DEMULTIPLEXER

INPUTS				OUTPUTS			
SELECT	ENABLE	DATA		1Y0	1Y1	1Y2	1Y3
B A	1E	1C					
X X	H	X		H	H	H	H
L L	L	H		L	H	H	H
L H	L	H		H	L	H	H
H L	L	H		H	H	L	H
H H	L	H		H	H	H	L
X X	X	L		H	H	H	H

INPUTS				OUTPUTS			
SELECT	ENABLE	DATA		2Y0	2Y1	2Y2	2Y3
B A	2E	2C					
X X	H	X		H	H	H	H
L L	L	L		L	H	H	H
L H	L	L		H	L	H	H
H L	L	L		H	H	L	H
H H	L	L		H	H	H	L
X X	X	H		H	H	H	H

Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC Supply voltage		-0.5	+7	V
I_{IK}, I_{OK}	DC input or output diode current	for $V_I < -0.5$ or $V_I > V_{CC} + 0.5V$		20	mA
I_O	DC output source or sink current	for $-0.5V < V_O < V_{CC} + 0.5V$		25	mA
I_{CC}	DC V_{CC} or GND current			50	mA
T_{stg}	Storage temperature range		-65	150	°C
P_D	Power dissipation per package	above +70°C: derate linearly with 8mW/K		500	mW
T_L	Lead temperature	At distance $1/16 \pm 1/32$ in. from case for 60 sec(CERAMIC) 10 sec(PLASTIC)		300 260	°C

Recommended Operating Conditions

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range V_{CC} : GD54/74HC Types GD54/74HCT Types	2 4.5	6 5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A : GD74 Types GD54 Types	-40 -55	+85 +125	°C
Input Rise and Fall times t_r, t_f : GD54/74HC Types at 2V at 4.5V at 6V GD54/74HCT Types at 4.5V		1000 500 400 500	ns

Logic Diagram

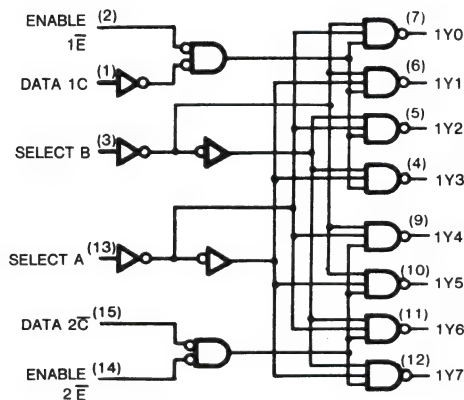


Fig. 1 Logic diagram

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HC155		GD54HC155		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2		1.5 3.15 4.2		V
V _{IL}	LOW level input voltage		2.0 4.5 6.0			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH} or V _{IL}	I _{OH} =-20μA I _{OH} =-4mA I _{OH} =-5.2mA	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0	1.9 4.4 5.9		1.9 4.4 5.9		V
				4.5 6.0	3.98 5.48	4.3 5.2	3.84 5.34		3.7 5.2		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH} or V _{IL}	I _{OL} =20μA I _{OL} =4mA I _{OL} =5.2mA	2.0 4.5 6.0			0.1 0.1 0.1	0.1 0.1 0.1		0.1 0.1 0.1	V
				4.5 6.0		0.17 0.15	0.26 0.26	0.33 0.33		0.4 0.4	
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	6.0			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	6.0			8		80		160	μA

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HCT155		GD54HCT155		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		4.5 to 5.0	2.0			2.0		2.0		V
V _{IL}	LOW level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH} or V _{IL}	I _{OH} =-20μA	4.5	4.4	4.5	4.4		4.4		V
			I _{OH} =-4mA	4.5	3.98	4.3	3.84		3.7		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH} or V _{IL}	I _{OL} =20μA	4.5		0.1	0.1		0.1		V
			I _{OL} =4mA	4.5		0.17	0.26	0.33		0.4	
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	5.5			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	5.5			8		80		160	μA

AC Characteristics for HC: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HC155		GD54HC155		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} / t_{PHL}	Propagation Delay Time A,B or $2\bar{C}$ to $1Y_n$, $2Y_n$	2.0		70	150		190		210	ns
		4.5		18	30		40		45	
		6.0		15	25		35		40	
t_{PLH} / t_{PHL}	Propagation Delay Time $n\bar{E}$, $1C$ to $1Y_n$, $2Y_n$	2.0		80	160		200		220	ns
		4.5		22	35		48		55	
		6.0		30	32		45		50	
t_{TLH} / t_{THL}	Output Transition Time	2.0		36	75		95		110	ns
		4.5		7	15		19		22	
		6.0		6	13		15		19	

AC Characteristics for HCT: $t_r=t_f=6\text{ns}$ $C_L=50\text{pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HCT155		GD54HCT155		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} / t_{PHL}	Propagation Delay Time A,B, or $2\bar{C}$ to $1Y_n$, $2Y_n$	4.5		22	35		42		47	ns
t_{PLH} / t_{PHL}	Propagation Delay Time $n\bar{E}$, $1C$ to $1Y_n$, $2Y_n$	4.5		25	40		52		60	ns
t_{TLH} / t_{THL}	Output Transition Time	4.5		7	15		19		22	ns

GD54/74HC157, GD54/74HCT157

QUAD 2-INPUT SELECTORS/MULTIPLEXERS WITH NONINVERTED OUTPUT

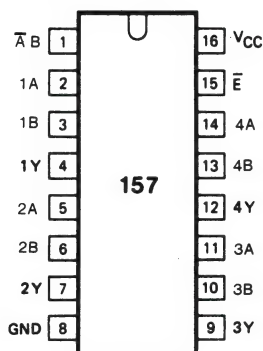
General Description

These devices are identical in pinout to the 54/74LS157. They consist of four 2-input multiplexers with common select and enable inputs, and noninverted outputs. When the enable input is low, the four outputs assume the value as selected from the inputs, when the enable input is high, the output become low regardless of any other inputs values. Select decoding is done internally resulting in a single select input only. The HC/HCT 158 operates in the same manner, except that its outputs are in inverted form. The HC/HCT 157 is similar in function to the HC/HCT 257 and 258 which have 3-state outputs. These devices are characterized for operation over wide temperature ranges to meet industry and military specifications.

Features

- Low Power consumption characteristic of CMOS devices
- Output drive capability: 10 LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts
for HCT 4.5 to 5.5 volts
- Low input current: $1\mu\text{A}$ Max.
- Low quiescent current: $80\mu\text{A}$ Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs

Pin Configuration



Suffix-Blank : Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package
Suffix-D : Small Outline Package

Function Table

INPUTS				OUTPUT
\bar{E}	\bar{A}/B	nA	nB	nY
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

H=HIGH voltage level

L=LOW voltage level

X=don't care

Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC Supply voltage		-0.5	+7	V
I_{IK}, I_{OK}	DC input or output diode current	for $V_I < -0.5$ or $V_I > V_{CC} + 0.5V$		20	mA
I_O	DC output source or sink current	for $-0.5V < V_O < V_{CC} + 0.5V$		25	mA
I_{CC}	DC V_{CC} or GND current			50	mA
T_{stg}	Storage temperature range		-65	150	°C
P_D	Power dissipation per package	above +70°C: derate linearly with 8mW/K		500	mW
T_L	Lead temperature	At distance 1/16±1/32 in. from case for 60 sec(CERAMIC) 10 sec(PLASTIC)		300 260	°C

Recommended Operating Conditions

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range V_{CC} : GD54/74HC Types GD54/74HCT Types	2 4.5	6 5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A : GD74 Types GD54 Types	-40 -55	+85 +125	°C
Input Rise and Fall times t_r, t_f : GD54/74HC Types at 2V at 4.5V at 6V GD54/74HCT Types at 4.5 V		1000 500 400 500	ns

Logic Diagram

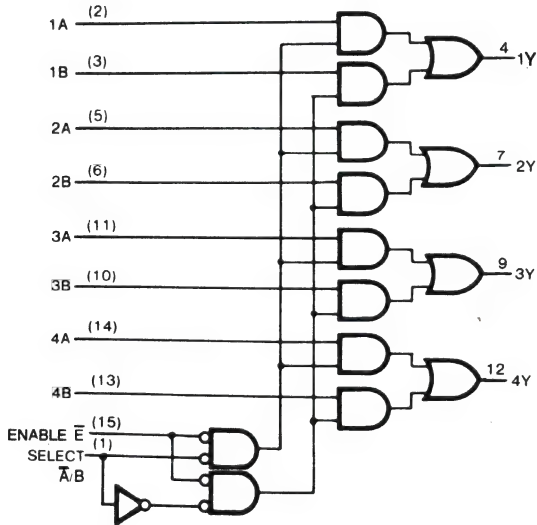


Fig. 1 Logic diagram

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HC157		GD54HC157		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2		1.5 3.15 4.2		V
V _{IL}	LOW level input voltage		2.0 4.5 6.0			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH}	I _{OH} =-20μA	2.0	1.9	2.0	1.9		1.9		V
				4.5	4.4	4.5	4.4		4.4		
		or V _{IL}	I _{OH} =-4mA I _{OH} =-5.2mA	6.0	5.9	6.0	5.9		5.9		
				4.5	3.98	4.3	3.84		3.7		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH}	I _{OL} =20μA	2.0			0.1		0.1		V
				4.5			0.1		0.1		
		or V _{IL}	I _{OL} =4mA I _{OL} =5.2mA	6.0			0.1		0.1		
				4.5		0.17	0.26		0.33		
				6.0		0.15	0.26		0.33		
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	6.0			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	6.0			8		80		160	μA

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HCT157		GD54HCT157		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		4.5 to 5.5	2.0			2.0		2.0		V
V _{IL}	LOW level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH}	I _{OH} =-20μA	4.5	4.4	4.5	4.4		4.4		V
		or V _{IL}	I _{OH} =-4mA	4.5	3.98	4.3	3.84		3.7		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH}	I _{OL} =20μA	4.5			0.1		0.1		V
		or V _{IL}	I _{OL} =4mA	4.5		0.17	0.26		0.33		
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	5.5			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	5.5			8		80		160	μA

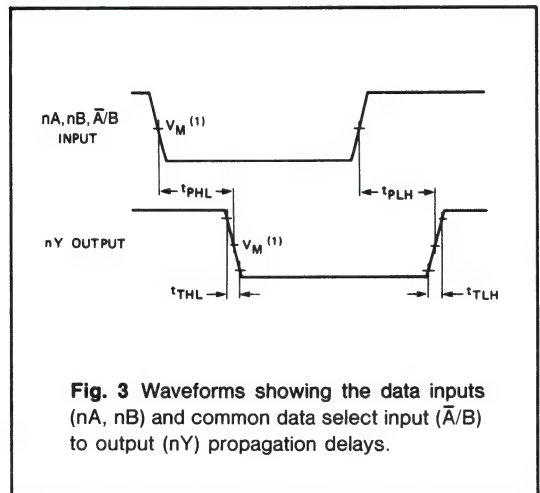
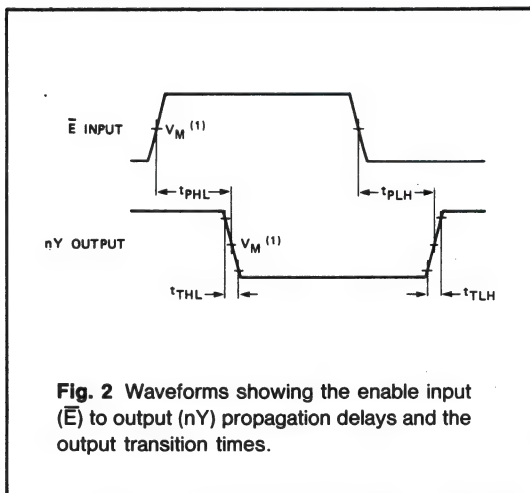
AC Characteristics for HC: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER V_{CC}	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HC157		GD54HC157		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
$t_{PLH}/$ t_{PHL}	Propagation Delay Time $n\bar{A}, nB$ to nY	2.0 4.5 6.0		36 13 10	125 25 21		155 31 26		190 38 32	ns
$t_{PLH}/$ t_{PHL}	Propagation Delay Time \bar{E} to nY	2.0 4.5 6.0		39 14 11	115 23 20		145 29 25		175 35 30	ns
$t_{PLH}/$ t_{PHL}	Propagation Delay Time Select \bar{A}/B to nY	2.0 4.5 6.0		47 17 14	145 29 25		180 36 31		220 44 38	ns
$t_{TLH}/$ t_{THL}	Output Transition Time	2.0 4.5 6.0		19 7 6	75 15 13		95 19 16		110 22 19	ns

AC Characteristics for HCT: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HCT157		GD54HCT157		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
$t_{PLH}/$ t_{PHL}	Propagation Delay Time nA, nB to nY	4.5		16	27		34		41	ns
$t_{PLH}/$ t_{PHL}	Propagation Delay Time \bar{E} to nY	4.5		15	26		33		39	ns
$t_{PLH}/$ t_{PHL}	Propagation Delay Time Select \bar{A}/B to nY	4.5		22	37		46		56	ns
$t_{TLH}/$ t_{THL}	Output Transition Time	4.5		7	15		19		22	ns

AC Waveforms



Note to AC waveforms

(1) HC : $V_M=50\%$; $V_I=GND$ to V_{CC} .

HCT: $V_M=1.3V$; $V_I=GND$ to $3V$.

GD54/74HC158, GD54/74HCT158

QUAD 2-INPUT SELECTORS/MULTIPLEXERS WITH INVERTED OUTPUT

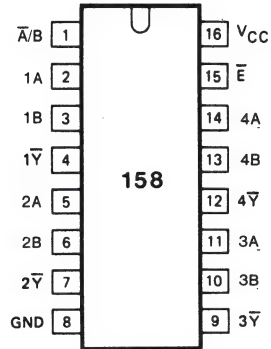
General Description

These devices are identical in pinout to the 54/74LS158. They consist of four 2-Input multiplexers with common select and enable inputs, and inverted outputs. When the enable input is low, the four outputs assume the value as selected from the inputs. When the enable input is high, the outputs become low regardless of any other inputs. Select decoding is done internally resulting in a single select input only. The HC/HCT157 operates in the same manner, except that its outputs are in noninverted form. The HC/HCT 158 is similar in function to the HC/HCT 257 and 258 which have 3-state outputs. These devices are characterized for operation over wide temperature ranges to meet industry and military specifications.

Features

- Low Power consumption characteristic of CMOS devices
- Output drive capability: 10 LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts
for HCT 4.5 to 5.5 volts
- Low input current: 1 μ A Max.
- Low quiescent current: 80 μ A Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs

Pin Configuration



Suffix-Blank : Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package
Suffix-D : Small Outline Package

Function Table

INPUTS				OUTPUT
\bar{E}	\bar{A}/B	nA	nB	nY
H	X	X	X	H
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

H=HIGH voltage level

L=LOW voltage level

X=don't care

Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC Supply voltage		-0.5	+7	V
I_{IK}, I_{OK}	DC input or output diode current	for $V_I < -0.5$ or $V_I > V_{CC} + 0.5V$		20	mA
I_O	DC output source or sink current	for $-0.5V < V_O < V_{CC} + 0.5V$		25	mA
I_{CC}	DC V_{CC} or GND current			50	mA
T_{stg}	Storage temperature range		-65	150	°C
P_D	Power dissipation per package	above +70°C: derate linearly with 8mW/K		500	mW
T_L	Lead temperature	At distance 1/16±1/32 in. from case for 60 sec(CERAMIC) 10 sec(PLASTIC)		300 260	°C

Recommended Operating Conditions

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range V_{CC} : GD54/74HC Types GD54/74HCT Types	2 4.5	6 5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A : GD74 Types GD54 Types	-40 -55	+85 +125	°C
Input Rise and Fall times t_r, t_f : GD54/74HC Types at 2V at 4.5V at 6V GD54/74HCT Types at 4.5 V		1000 500 400 500	ns

Logic Diagram

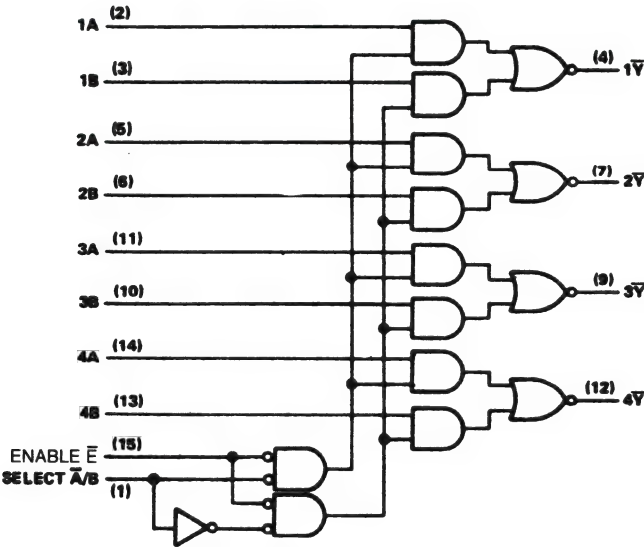


Fig. 1 Logic diagram

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HC158		GD54HC158		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2		1.5 3.15 4.2		V
V _{IL}	LOW level input voltage		2.0 4.5 6.0			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH}	I _{OH} =-20μA	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9	V
			I _{OH} =-4mA	4.5 6.0	3.98 5.48	4.3 5.2		3.84 5.34		3.7 5.2	
		or V _{IL}	I _{OH} =-5.2mA	4.5 6.0	3.98 5.48	4.3 5.2		3.84 5.34		3.7 5.2	
			I _{OH} =-5.2mA	4.5 6.0	3.98 5.48	4.3 5.2		3.84 5.34		3.7 5.2	
V _{OL}	LOW level output voltage	V _{IN} =V _{IH}	I _{OL} =20μA	2.0 4.5 6.0			0.1 0.1 0.1	0.1 0.1 0.1		0.1 0.1 0.1	V
			I _{OL} =4mA	4.5 6.0		0.17 0.15	0.26 0.26		0.33 0.33	0.4 0.4	
		or V _{IL}	I _{OL} =4mA	4.5 6.0		0.17 0.15	0.26 0.26		0.33 0.33	0.4 0.4	
			I _{OL} =5.2mA	4.5 6.0		0.17 0.15	0.26 0.26		0.33 0.33	0.4 0.4	
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	6.0			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	6.0			8		80		160	μA

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HCT158		GD54HCT158		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		4.5 to 5.5	2.0			2.0		2.0		V
V _{IL}	LOW level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH}	I _{OH} =-20μA	4.5	4.4	4.5		4.4		4.4	V
		or V _{IL}	I _{OH} =-4mA	4.5	3.98	4.3		3.84		3.7	
V _{OL}	LOW level output voltage	V _{IN} =V _{IH}	I _{OL} =20μA	4.5			0.1	0.1		0.1	V
		or V _{IL}	I _{OL} =4mA	4.5		0.17	0.26	0.33		0.4	
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	5.5			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	5.5			8		80		160	μA

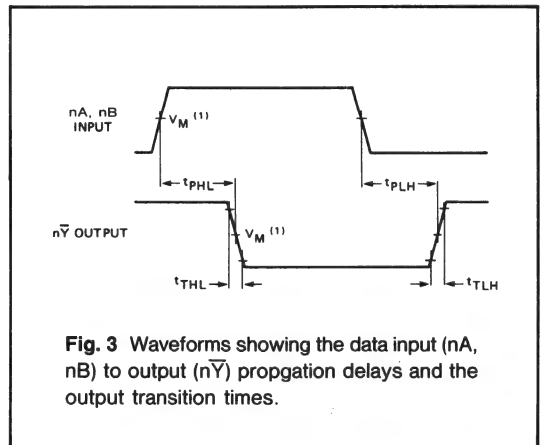
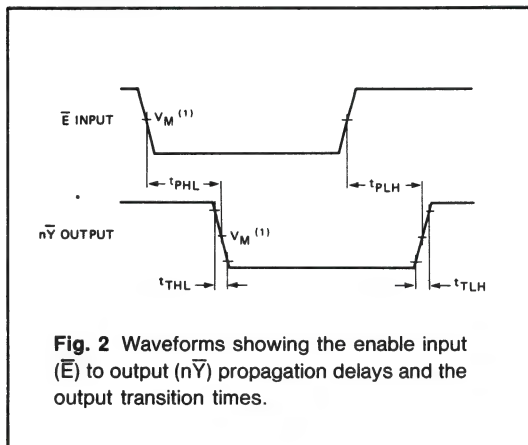
AC Characteristics for HC: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HC158		GD54HC158		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
$t_{PLH} /$ t_{PHL}	Propagation Delay Time nA, nB to $n\bar{Y}$	2.0 4.5 6.0		41 15 12	125 25 21		155 31 26		190 38 32	ns
$t_{PLH} /$ t_{PHL}	Propagation Delay Time \bar{E} to $n\bar{Y}$	2.0 4.5 6.0		47 17 14	145 29 25		180 36 31		220 44 38	ns
$t_{PLH} /$ t_{PHL}	Propagation Delay Time Select \bar{A}/\bar{B} to $n\bar{Y}$	2.0 4.5 6.0		47 17 14	145 29 25		180 36 31		220 44 38	ns
$t_{TLH} /$ t_{THL}	Output Transition Time	2.0 4.5 6.0		19 7 6	75 15 13		95 19 16		110 22 19	ns

AC Characteristics for HCT: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HCT158		GD54HCT158		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
$t_{PLH} /$ t_{PHL}	Propagation Delay Time nA, nB to $n\bar{Y}$	4.5		16	30		38		45	ns
$t_{PLH} /$ t_{PHL}	Propagation Delay Time \bar{E} to $n\bar{Y}$	4.5		19	35		44		53	ns
$t_{PLH} /$ t_{PHL}	Propagation Delay Time Select \bar{A}/\bar{B} to $n\bar{Y}$	4.5		19	35		44		53	ns
$t_{TLH} /$ t_{THL}	Output Transition Time	4.5		7	15		19		22	ns

AC Waveforms



Note to AC waveforms

- (1) HC : $V_M=50\%$; $V_I=\text{GND}$ to V_{CC} .
HCT : $V_M=1.3\text{V}$; $V_I=\text{GND}$ to 3V .

GD54/74HC160, GD54/74HCT160

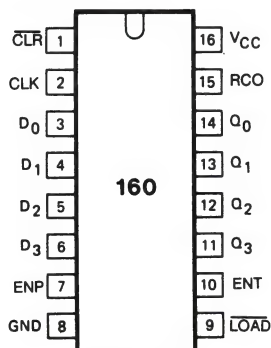
SYNCHRONOUS DECADE COUNTER

WITH ASYNCHRONOUS CLEAR

General Description

These devices are identical in pinout to the 54/74LS160. They contain a 4-bit decade counter consisting of four flip-flops. All flip-flops are clocked simultaneously on the positive edge of the clock input. Counters may be preset using the load input at the rising edge of clock. All the counters may be cleared asynchronously by utilizing the clear input. When the clear is taken low the counter is cleared immediately regardless of the clock. The HC/HCT 160 is similar in function to the HC/HCT 162 which is cleared synchronously. These devices are characterized for operation over wide temperature ranges to meet industry and military specifications

Pin Configuration



Suffix-Blank : Plastic Dual In Line Package
 Suffix-J : Ceramic Dual In Line Package
 Suffix-D : Small Outline Package

Features

- Low Power consumption characteristic of CMOS devices
- Output drive capability: 10 LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts
for HCT 4.5 to 5.5 volts
- Low input current: 1 μ A Max.
- Low quiescent current: 80 μ A Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs

Function Table

OPERATING MODE	INPUTS					OUTPUTS		
	CLR	CLK	ENP	ENT	LOAD	D _n	Q _n	RCO
reset (clear)	L	\uparrow	X	X	X	X	L	L
parallel load	H	\uparrow	X	X	L	L	L	L
	H	\uparrow	X	X	H	h	H	*
count	H	\uparrow	h	h	h	X	count	*
hold (do nothing)	H	X	L	X	h	X	q _n	*
	H	X	X	L	h	X	q _n	L

Note to function table

* The RCO outputs is HIGH when ENT is HIGH and the counter is at terminal count (HLLH)

H = HIGH voltage level

h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CLK transition

L = LOW voltage level

l = LOW voltage level one set-up time prior to the LOW-to-HIGH CLK transition

q = lower case letters indicate the state of the referenced output one set-up time prior to the LOW-to-HIGH CLK transition

X = don't care

\uparrow = LOW-to-HIGH CLK transition

Logic Diagram

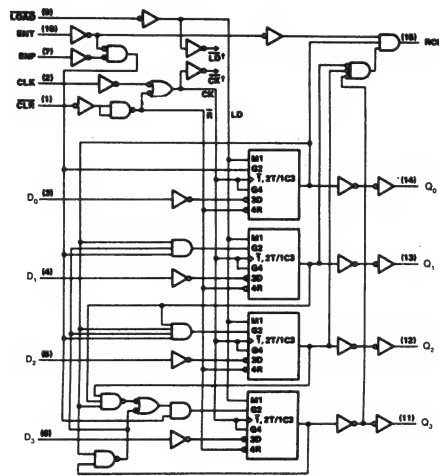


Fig. 1 Logic diagram

Output Sequence

Illustrated below is the following sequence:

1. Clear outputs to zero (HC/HCT 160 is asynchronous)
2. Preset to BCD seven
3. Count to eight, nine, zero, one, two, and three
4. Inhibit

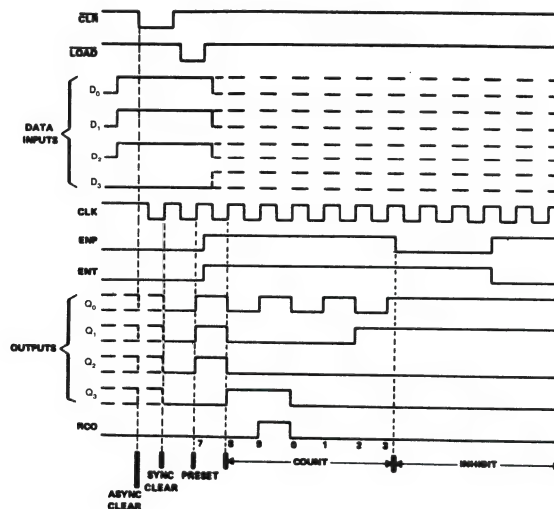


Fig. 2 Output sequence

Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC Supply voltage		-0.5	+7	V
I_{IK}, I_{OK}	DC input or output diode current	for $V_I < -0.5$ or $V_I > V_{CC} + 0.5V$		20	mA
I_O	DC output source or sink current	for $-0.5V < V_O < V_{CC} + 0.5V$		25	mA
I_{CC}	DC V_{CC} or GND current			50	mA
T_{stg}	Storage temperature range		-65	150	°C
P_D	Power dissipation per package	above +70°C: derate linearly with 8mW/K		500	mW
T_L	Lead temperature	At distance 1/16 ± 1/32 in. from case for 60 sec(CERAMIC) 10 sec(PLASTIC)		300 260	°C

Recommended Operating Conditions

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range V_{CC} : GD54/74HC Types GD54/74HCT Types	2 4.5	6 5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A : GD74 Types GD54 Types	-40 -55	+85 +125	°C
Input Rise and Fall times t_r, t_f : GD54/74HC Types at 2V at 4.5V at 6V GD54/74HCT Types at 4.5 V		1000 500 400 500	ns

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HC160		GD54HC160		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2		1.5 3.15 4.2		V
V _{IL}	LOW level input voltage		2.0 4.5 6.0			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH} I _{OH} =-20μA	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V
		or V _{IL} I _{OH} =-4mA I _{OH} =-5.2mA	4.5 6.0	3.98 5.48	4.3 5.2		3.84 5.34		3.7 5.2		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH} I _{OL} =20μA	2.0 4.5 6.0			0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V
		or V _{IL} I _{OL} =4mA I _{OL} =5.2mA	4.5 6.0		0.17 0.15	0.26 0.26		0.33 0.33		0.4 0.4	
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	6.0			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	6.0			8		80		160	μA

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HCT160		GD54HCT160		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		4.5 to 5.5	2.0			2.0		2.0		V
V _{IL}	LOW level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH} I _{OH} =-20μA	4.5	4.4	4.5		4.4		4.4		V
		or V _{IL} I _{OH} =-4mA	4.5	3.98	4.3		3.84		3.7		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH} I _{OL} =20μA	4.5			0.1		0.1		0.1	V
		or V _{IL} I _{OL} =4mA	4.5		0.17	0.26		0.33		0.4	
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	5.5			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	5.5			8		80		160	μA

Timing Requirements for HC: $t_r = t_f = 6\text{ns}$ $C_L = 50\text{ pF}$

SYMBOL	PARAMETER		V_{CC} (V)	$T_A = 25^\circ\text{C}$			GD74HC160		GD54HC160		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_w	Pulse width	$\overline{\text{CLR}}$ low, CLK	2.0 4.5 6.0	80 16 14			100 20 17		120 24 20		ns
t_{su}	Setup time	D_n to CLK	2.0 4.5 6.0	80 16 14			100 20 17		120 27 20		ns
		$\overline{\text{LOAD}}$ to CLK	2.0 4.5 6.0	135 25 22			170 31 29		205 40 35		ns
		ENP, ENT to CLK	2.0 4.5 6.0	135 27 23			250 50 43		300 60 51		ns
t_{rec}	Recovery time	$\overline{\text{CLR}}$ to CLK	2.0 4.5 6.0	100 20 17			125 25 21		150 30 26		ns
t_h	Hold time	All sync, input to CLK	2.0 4.5 6.0	0 0 0			0 0 0		0 0 0		ns

AC Characteristics for HC: $t_r = t_f = 6\text{ns}$ $C_L = 50\text{ pF}$

SYMBOL	PARAMETER		V_{CC} (V)	$T_A = 25^\circ\text{C}$			GD74HC160		GD54HC160		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
f_{max}	Maximum clock pulse frequency		2.0 4.5 6.0	6 31 36	14 40 44		5 25 29		4.2 21 25		MHz
$t_{PLH}/$ t_{PHL}	Propagation Delay Time	CLK to RCO	2.0 4.5 6.0		60 20 16	200 40 31		250 52 43		305 63 52	ns
$t_{PLH}/$ t_{PHL}	Propagation Delay Time	CLK to Qn	2.0 4.5 6.0		58 18 16	180 34 28		225 43 37		275 53 46	ns
$t_{PLH}/$ t_{PHL}	Propagation Delay Time	ENT to RCO	2.0 4.5 6.0		45 15 13	140 28 25		180 36 32		215 43 38	ns
$t_{PLH}/$ t_{PHL}	Propagation Delay Time	$\overline{\text{CLR}}$ to Qn	2.0 4.5 6.0		58 18 16	200 35 30		255 46 42		305 56 51	ns
$t_{PLH}/$ t_{PHL}	Propagation Delay Time	$\overline{\text{CLR}}$ to RCO	2.0 4.5 6.0		60 20 18	210 40 34		265 51 45		315 62 55	ns
$t_{TLH}/$ t_{THL}	Output Transition Time		2.0 4.5 6.0		38 7 6	75 15 13		95 19 16		110 22 19	ns

Timing Requirements for HCT: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER		V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HCT160		GD54HCT160		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_w	Pulse width	$\overline{\text{CLR}}$ low, CLK	4.5	20			24		28		ns
t_{su}	Setup time	D_n to CLK	4.5	20			24		28		ns
		$\overline{\text{LOAD}}$ to CLK	4.5	30			38		45		ns
		ENP, ENT to CLK	4.5	30			54		64		ns
t_{rec}	Recovery time	$\overline{\text{CLR}}$ to CLK	4.5	24			29		34		ns
t_h	Hold time	All sync, input to CLK	4.5	0			0		0		ns

AC Characteristics for HCT: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HCT160		GD54HCT160		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
f_{max}	Maximum clock pulse frequency	4.5	16	28		13		11		MHz
$t_{PLH}/$ t_{PHL}	Propagation Delay Time CLK to RCO	4.5		26		56		67		ns
$t_{PLH}/$ t_{PHL}	Propagation Delay Time CLK to Qn	4.5		24		47		57		ns
$t_{PLH}/$ t_{PHL}	Propagation Delay Time ENT to RCO	4.5		21		40		47		ns
$t_{PLH}/$ t_{PHL}	Propagation Delay Time $\overline{\text{CLR}}$ to Qn	4.5		24		50		60		ns
$t_{PLH}/$ t_{PHL}	Propagation Delay Time $\overline{\text{CLR}}$ to RCO	4.5		26		55		67		ns
$t_{TLH}/$ t_{THL}	Output Transition Time	4.5		7		19		22		ns

AC Waveforms

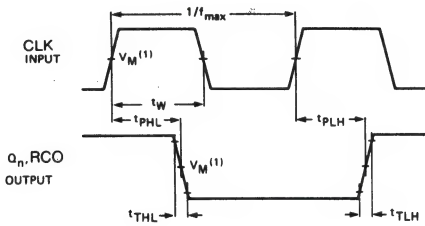


Fig. 3 Waveforms showing the clock (CLK) to outputs (Q_n , RCO) propagation delays, the clock pulse width, the output transition times and the maximum clock frequency.

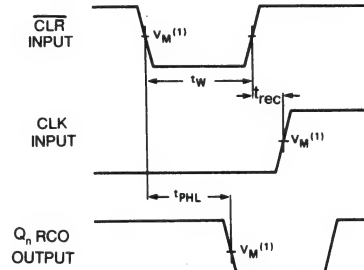


Fig. 4 Waveforms showing the master clear (CLR) pulse width, the master clear to output (Q_n , RCO) propagation delays and the master clear to clock (CLK) recovery time.

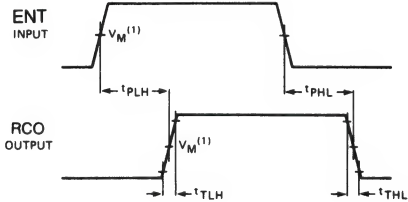


Fig. 5 Waveforms showing the input (ENT) to output (RCO) propagation delays and output transition times.

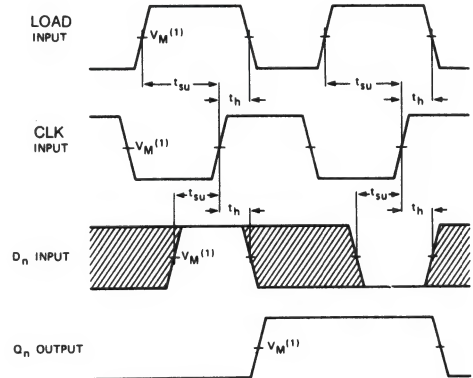


Fig. 6 Waveforms showing the set-up and hold times for the input (D_n) and parallel enable input (LOAD)

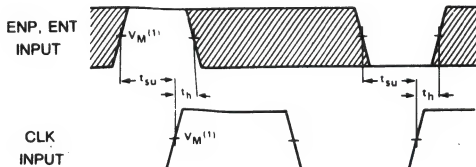


Fig. 7 Waveforms showing the ENP and ENT set-up and hold times.

Note to Figs 6 and 7

The shaded areas indicate when the input is permitted to change for predictable output performance.

Note to AC waveforms

- (1) HC : $V_M = 50\%$; $V_I = \text{GND to } V_{CC}$.
- HCT : $V_M = 1.3V$; $V_I = \text{GND to } 3V$.

GD54/74HC161, GD54/74HCT161

SYNCHRONOUS BINARY COUNTER WITH ASYNCHRONOUS CLEAR

General Description

These devices are identical in pinout to the 54/74LS161. They contain a 4-bit binary counter consisting of four flip-flops. All flip-flops are clocked simultaneously on the positive edge of the clock input. Counters may be preset using the load input at the rising edge of clock. All the counters may be cleared asynchronously by utilizing the clear input. When the clear is taken low the counter is cleared immediately regardless of the clock. The HC/HCT 161 is similar in function to the HC/HCT 163 which is cleared synchronously. These devices are characterized for operation over wide temperature ranges to meet industry and military specifications.

Features

- Low Power consumption characteristic of CMOS devices
- Output drive capability: 10 LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts
for HCT 4.5 to 5.5 volts
- Low input current: 1 μ A Max.
- Low quiescent current: 80 μ A Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs

Function Table

OPERATING MODE	INPUTS						OUTPUTS	
	CLR	CLK	ENP	ENT	LOAD	D _n	Q _n	RCO
reset (clear)	L	X	X	X	X	X	L	L
parallel load	H	↑	X	X	l	l	L	L
	H	↑	X	X	l	h	H	*
count	H	↑	h	h	h	X	count	*
hold (do nothing)	H	X	l	X	h	X	q _n	*
	H	X	X	l	h	X	q _n	L

Note to function table

* The RCO output is HIGH when ENT is HIGH and the counter is at terminal count (HHHH).

h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CLK transition

l = LOW voltage level one set-up time prior to the LOW-to-HIGH CLK transition

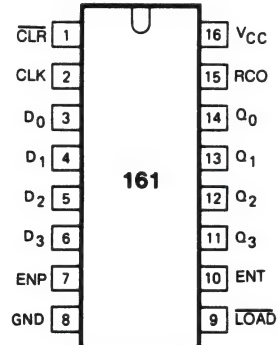
q = lower case letters indicate the state of the referenced output one set-up time prior to the LOW-to-HIGH

CLK transition

X = don't care

↑ = LOW-to-HIGH CLK transition

Pin Configuration



Suffix-Blank : Plastic Dual In Line Package
 Suffix-J : Ceramic Dual In Line Package
 Suffix-D : Small Outline Package

Logic Diagram

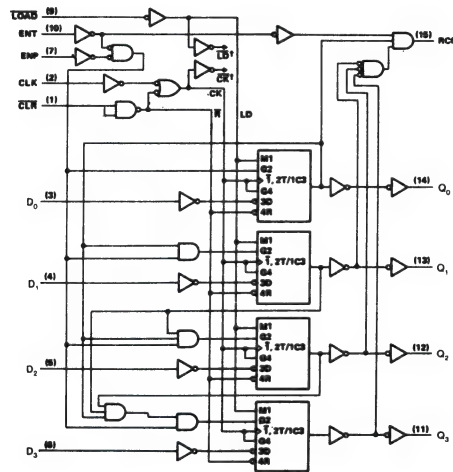


Fig. 1 Logic diagram

Output Sequence

Illustrated below is the following sequence:

1. Clear outputs to zero (HC/HCT 161 is asynchronous)
2. Preset to binary twelve
3. Count to thirteen, fourteen, zero, one, and two
4. Inhibit

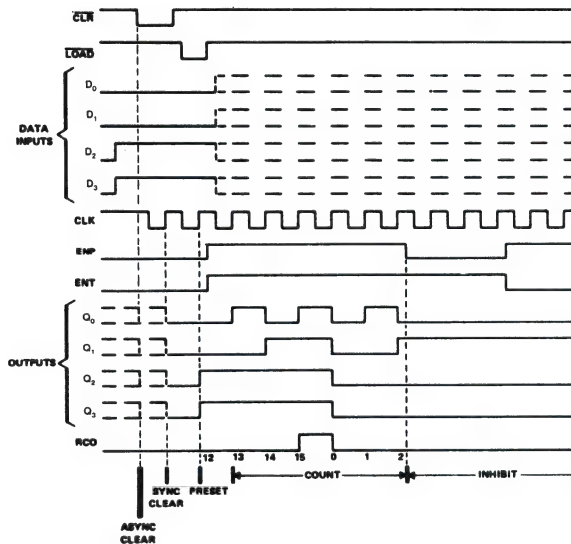


Fig. 2 Output sequence

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HC161		GD54HC161		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2		1.5 3.15 4.2		V
V _{IL}	LOW level input voltage		2.0 4.5 6.0			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH}	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V
		or V _{IL}									
V _{OL}	LOW level output voltage	V _{IN} =V _{IH}	2.0 4.5 6.0			0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V
		or V _{IL}									
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	6.0			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	6.0			8		80		160	μA

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HCT161		GD54HCT161		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		4.5 to 5.5	2.0			2.0		2.0		V
V _{IL}	LOW level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH}	4.5	4.4	4.5		4.4		4.4		V
		or V _{IL}									
V _{OL}	LOW level output voltage	V _{IN} =V _{IH}	4.5			0.1		0.1		0.1	V
		or V _{IL}									
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	5.5			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	5.5			8		80		160	μA

Timing Requirements for HC: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER		V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HC161		GD54HC161		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_w	Pulse width	$\overline{\text{CLR}}$ low, CLK	2.0 4.5 6.0	80 16 14	22 8 6		100 20 17		120 24 20		ns
t_{su}	Setup time	D_n to CLK	2.0 4.5 6.0	80 16 14			100 20 17		120 27 20		ns
		$\overline{\text{LOAD}}$ to CLK	2.0 4.5 6.0	135 25 22			170 31 29		205 40 35		ns
		ENP, ENT to CLK	2.0 4.5 6.0	135 27 23			250 50 43		300 60 51		ns
t_{rec}	Recovery time	$\overline{\text{CLR}}$ to CLK	2.0 4.5 6.0	100 20 17			125 25 21		150 30 26		ns
t_h	Hold time	All sync. input to CLK	2.0 4.5 6.0	0 0 0			0 0 0		0 0 0		ns

AC Characteristics for HC: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER		V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HC161		GD54HC161		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
f_{max}	Maximum clock pulse frequency		2.0 4.5 6.0	6 31 36	14 40 44		5 25 29		4.2 21 25		MHz
$t_{PLH}/$ t_{PHL}	Propagation Delay Time CLK to RCO		2.0 4.5 6.0		60 20 16	200 40 31		250 52 43		305 63 52	ns
$t_{PLH}/$ t_{PHL}	Propagation Delay Time CLK to Qn		2.0 4.5 6.0		58 19 17	180 34 28		225 43 37		275 53 46	ns
$t_{PLH}/$ t_{PHL}	Propagation Delay Time ENT to RCO		2.0 4.5 6.0		45 15 13	140 28 25		180 36 32		215 43 38	ns
$t_{PLH}/$ t_{PHL}	Propagation Delay Time $\overline{\text{CLR}}$ to Qn		2.0 4.5 6.0		58 18 16	200 35 30		255 46 42		305 56 51	ns
$t_{PLH}/$ t_{PHL}	Propagation Delay Time $\overline{\text{CLR}}$ to RCO		2.0 4.5 6.0		60 20 18	210 40 34		265 51 45		315 62 55	ns
$t_{TLH}/$ t_{THL}	Output Transition Time		2.0 4.5 6.0		38 7 6	75 15 13		95 19 16		110 22 19	ns

Timing Requirements for HCT: $t_r = t_f = 6\text{ns}$ $C_L = 50\text{ pF}$

SYMBOL	PARAMETER		V_{CC} (V)	$T_A = 25^\circ\text{C}$			GD74HCT161		GD54HCT161		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_w	Pulse width	$\overline{\text{CLR}}$ low, CLK	4.5	20			24		28		ns
t_{su}	Setup time	D_n to CLK	4.5	20			24		28		ns
		$\overline{\text{LOAD}}$ to CLK	4.5	30			38		45		ns
		ENP, ENT to CLK	4.5	30			54		64		ns
t_{rec}	Recovery time	$\overline{\text{CLR}}$ to CLK	4.5	24			29		34		ns
t_h	Hold time	All sync, input to CLK	4.5	0			0		0		ns

AC Characteristics for HCT: $t_r = t_f = 6\text{ns}$ $C_L = 50\text{ pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A = 25^\circ\text{C}$			GD74HCT161		GD54HCT161		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
f_{max}	Maximum clock pulse frequency	4.5	16	28		13		11		MHz
$t_{PLH}/$ t_{PHL}	Propagation Delay Time CLK to RCO	4.5		26		56		67		ns
$t_{PLH}/$ t_{PHL}	Propagation Delay Time CLK to Qn	4.5		24		47		57		ns
$t_{PLH}/$ t_{PHL}	Propagation Delay Time ENT to RCO	4.5		21		40		47		ns
$t_{PLH}/$ t_{PHL}	Propagation Delay Time $\overline{\text{CLR}}$ to Qn	4.5		24		50		60		ns
$t_{PLH}/$ t_{PHL}	Propagation Delay Time $\overline{\text{CLR}}$ to RCO	4.5		26		55		67		ns
$t_{TLH}/$ t_{THL}	Output Transition Time	4.5		7		19		22		ns

AC Waveforms

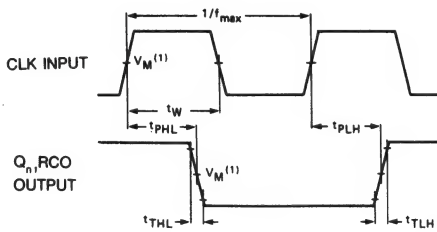


Fig. 4 Waveforms showing the clock (CLK) to outputs (Q_n , RCO) propagation delays, the clock pulse width, the output transition times and the maximum clock frequency.

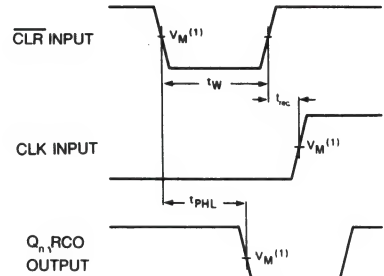


Fig. 5 Waveforms showing the master clear (\overline{CLR}) pulse width, the master clear to output (Q_n , RCO) propagation delays and the master clear to clock (CLK) recovery time.

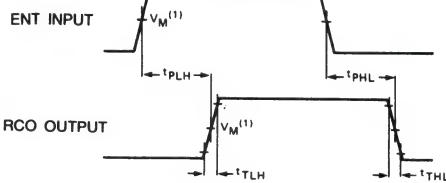


Fig. 6 Waveforms showing the input (ENT) to output (RCO) propagation delays and output transition times.

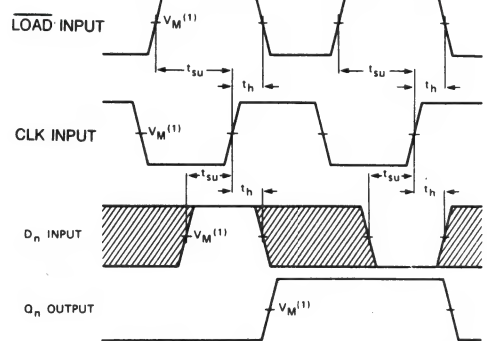


Fig. 7 Waveforms showing the set-up and hold times for the input (D_n) and parallel enable input (\overline{LOAD})

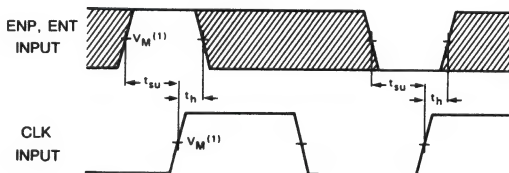


Fig. 8 Waveforms showing the ENP and ENT set-up and hold times.

Note to Figs 7 and 8

The shaded areas indicate when the input is permitted to change for predictable output performance.

Note to AC waveforms

- (1) HC : $V_M = 50\%$; $V_i = GND$ to V_{CC} ;
HCT : $V_M = 1.3V$; $V_i = GND$ to $3V$.

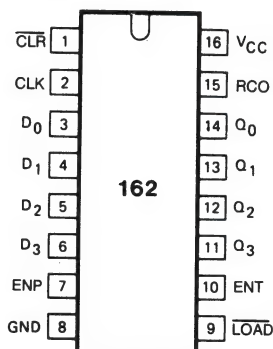
GD54/74HC162, GD54/74HCT162

SYNCHRONOUS DECADE COUNTER WITH SYNCHRONOUS CLEAR

General Description

These devices are identical in pinout to the 54/74LS162. They contain a 4-Bit decade counter consisting of four flip-flops. All flip-flops are clocked simultaneously on the positive edge of the clock input. Counters may be PRESET using the load input at the rising edge of clock. All the counters may be cleared synchronously by utilizing the clear input. That is, the counters are cleared on the positive edge of the clock while the clear input is held LOW. The HC/HCT 162 is similar in function to the HC/HCT 160 which is cleared asynchronously. These devices are characterized for operation over wide temperature ranges to meet industry and military specifications

Pin Configuration



Suffix-Blank : Plastic Dual In Line Package
 Suffix-J : Ceramic Dual In Line Package
 Suffix-D : Small Outline Package

Features

- Low Power consumption characteristic of CMOS devices
- Output drive capability: 10 LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts
for HCT 4.5 to 5.5 volts
- Low input current: 1 μ A Max.
- Low quiescent current: 80 μ A Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs

Function Table

OPERATING MODE	INPUTS					OUTPUTS		
	CLR	CLK	ENP	ENT	LOAD	D _n	Q _n	RCO
reset (clear)	1	\uparrow	X	X	X	X	L	L
parallel load	h	\uparrow	X	X	1	1	L	L
	h	\uparrow	X	X	1	h	H	*
count	h	\uparrow	h	h	h	X	count	*
hold (do nothing)	h	X	1	X	h	X	q _n	*
	h	X	X	1	h	X	q _n	L

Note to function table

* The RCO output is HIGH when ENT is HIGH and the counter is at terminal count (HLLH).

1 = LOW voltage level one set-up time prior to the LOW-to-HIGH CLK transition

q = lower case letters indicate the state of the referenced output one set-up time prior to the LOW-to-HIGH CLK transition

h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CLK transition.

Logic Diagram

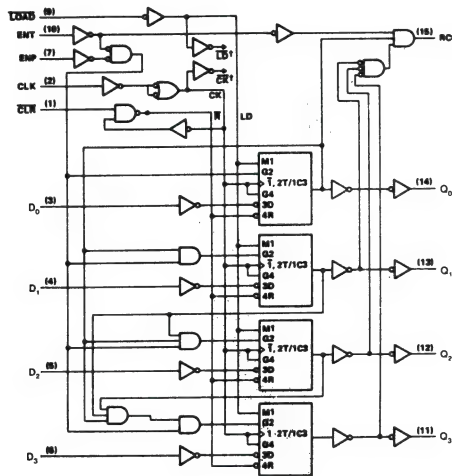


Fig. 1 Logic diagram

Output Sequence

Illustrated below is the following sequence:

1. Clear outputs to zero (HC/HCT 162 are synchronous)
2. Preset to BCD seven
3. Count to eight, nine, zero, one, two and three
4. Inhibit

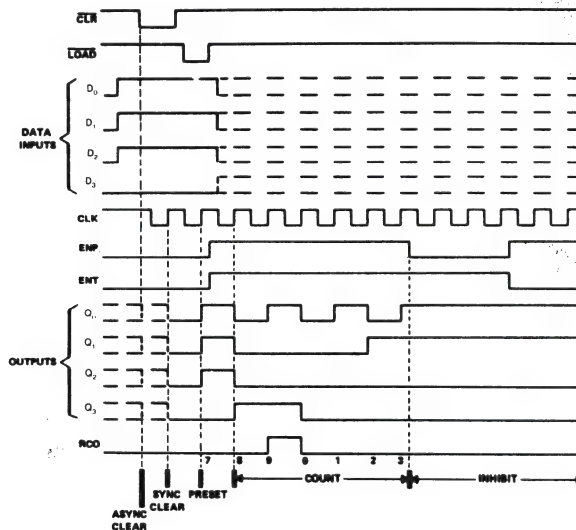


Fig. 2 Output Sequence

Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC Supply voltage		-0.5	+7	V
I_{IK}, I_{OK}	DC input or output diode current	for $V_I < -0.5$ or $V_I > V_{CC} + 0.5V$		20	mA
I_O	DC output source or sink current	for $-0.5V < V_O < V_{CC} + 0.5V$		25	mA
I_{CC}	DC V_{CC} or GND current			50	mA
T_{stg}	Storage temperature range		-65	150	°C
P_D	Power dissipation per package	above +70°C: derate linearly with 8mW/K		500	mW
T_L	Lead temperature	At distance 1/16 ± 1/32 in. from case for 60 sec(CERAMIC) 10 sec(PLASTIC)		300 260	°C

Recommended Operating Conditions

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range V_{CC} : GD54/74HC Types GD54/74HCT Types	2 4.5	6 5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A : GD74 Types GD54 Types	-40 -55	+85 +125	°C
Input Rise and Fall times t_r, t_f : GD54/74HC Types at 2V at 4.5V at 6V GD54/74HCT Types at 4.5V		1000 500 400 500	ns

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HC162		GD54HC162		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2		1.5 3.15 4.2		V
V _{IL}	LOW level input voltage		2.0 4.5 6.0			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH}	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V
		or V _{IL}	I _{OH} =-20μA I _{OH} =-4mA I _{OH} =-5.2mA	4.5 3.98 5.48	4.3 5.2		3.84 5.34		3.7 5.2		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH}	2.0 4.5 6.0			0.1 0.1 0.1	0.1 0.1 0.1		0.1 0.1 0.1		V
		or V _{IL}	I _{OL} =20μA I _{OL} =4mA I _{OL} =5.2mA	4.5 0.17 0.15	0.26 0.26		0.33 0.33		0.4 0.4		
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	6.0			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	6.0			8		80		160	μA

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HCT162		GD54HCT162		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		4.5 to 5.5	2.0			2.0		2.0		V
V _{IL}	LOW level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH}	4.5	4.4	4.5		4.4		4.4		V
		or V _{IL}	I _{OH} =-20μA I _{OH} =-4mA	3.98	4.3		3.84		3.7		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH}	4.5			0.1		0.1		0.1	V
		or V _{IL}	I _{OL} =20μA I _{OL} =4mA		0.17	0.26		0.33		0.4	
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	5.5			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	5.5			8		80		160	μA

Timing Requirements for HC: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER		V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HC162		GD54HC162		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_w	Pulse width	CLK high or low	2.0	80	22		100		120		ns
			4.5	16	8		20		24		
			6.0	14	6		17		20		
t_{su}	Setup time	D_n to CLK	2.0	100	28		125		150		ns
			4.5	20	10		25		30		
			6.0	17	8		21		26		
		$\overline{\text{LOAD}}$ to CLK	2.0	135	39		170		205		ns
			4.5	27	14		34		41		
			6.0	23	11		29		35		
		ENP, ENT to CLK	2.0	170	58		220		265		ns
			4.5	34	21		44		53		
			6.0	29	17		37		45		
		$\overline{\text{CLR}}$ to CLK	2.0	100	28		125		150		ns
			4.5	20	10		25		30		
			6.0	17	8		21		26		
t_{rec}	Recovery time	$\overline{\text{CLR}}$ to CLK	2.0	160	58		200		240		ns
			4.5	32	20		40		48		
			6.0	27	17		34		41		
t_h	Hold time	All sync, input to CLK	2.0	0			0		0		ns
			4.5	0			0		0		
			6.0	0			0		0		

AC Characteristics for HC: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER		V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HC162		GD54HC162		UNIT
				MIN.	TPY.	MAX.	MIN.	MAX.	MIN.	MAX.	
f_{max}	Maximum clock pulse frequency		2.0	6	14		5		4.2		MHz
			4.5	31	40		21		21		
			6.0	36	44		25		25		
$t_{PLH}/$ t_{PHL}	Propagation Delay Time CLK to RCO		2.0		60	200		270		315	ns
			4.5		21	41		54		65	
			6.0		17	35		46		55	
$t_{PLH}/$ t_{PHL}	Propagation Delay Time CLK to Qn		2.0		58	190		240		285	ns
			4.5		19	36		48		57	
			6.0		17	30		41		43	
$t_{PLH}/$ t_{PHL}	Propagation Delay Time ENT to RCO		2.0		39	150		190		225	ns
			4.5		14	30		38		48	
			6.0		11	26		33		38	
$t_{TLH}/$ t_{THL}	Output Transition Time		2.0		19	75		95		110	ns
			4.5		7	15		19		22	
			6.0		6	13		16		19	

Timing Requirements for HCT: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER		V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HCT162		GD54HCT162		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_w	Pulse width	CLK high or low	4.5	31	8		39		47		ns
t_{su}	Setup time	D_n to CLK	4.5	20	10		25		30		ns
		$\overline{\text{LOAD}}$ to CLK	4.5	35	16		44		53		ns
		ENP, ENT to CLK	4.5	40	23		50		60		ns
		$\overline{\text{CLR}}$ to CLK	4.5	20	12		25		30		ns
t_{rec}	Recovery time	$\overline{\text{CLR}}$ to CLK	4.5	32	20		41		50		ns
t_h	Hold time	All sync, input to CLK	4.5	0			0		0		ns

AC Characteristics for HCT: $t_r=t_f=6\text{ns}$ $C_L=50$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HCT162		GD54HCT162		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
f_{max}	Maximum clock pulse frequency	4.5	16	28		13		11		MHz
$t_{PLH}/$ t_{PHL}	Propagation Delay Time CLK to RCO	4.5		26	51		64		77	ns
$t_{PLH}/$ t_{PHL}	Propagation Delay Time CLK to Qn	4.5		24	43		54		65	ns
$t_{PLH}/$ t_{PHL}	Propagation Delay Time ENT to RCO	4.5		20	45		56		68	ns
$t_{TLH}/$ t_{THL}	Output Transition Time	4.5		7	15		19		22	ns

AC Waveforms

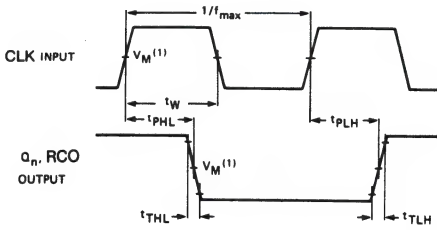


Fig. 3 Waveforms showing the clock (CLK) to outputs (Q_n , RCO) propagation delays, the clock pulse width, the output transition times and the maximum clock frequency.

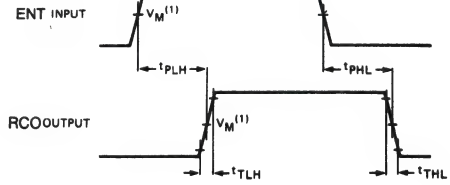


Fig. 4 Waveforms showing the input (ENT) to output (RCO) propagation delays and output transition times.

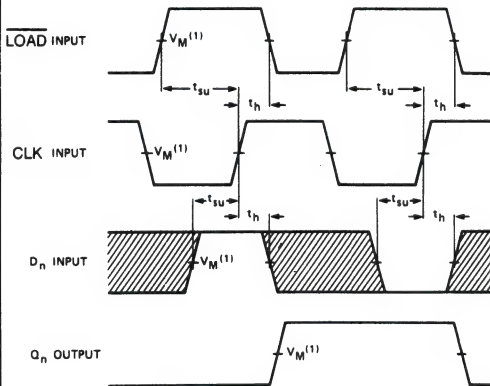


Fig. 5 Waveforms showing the set-up and hold times for the input (D_n) and parallel enable input (\overline{LOAD}).

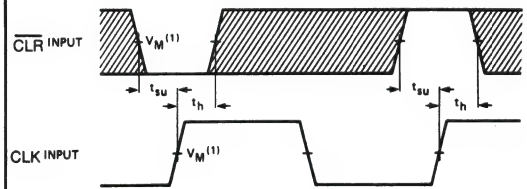


Fig. 6 Waveforms showing the \overline{CLR} set-up and hold times.

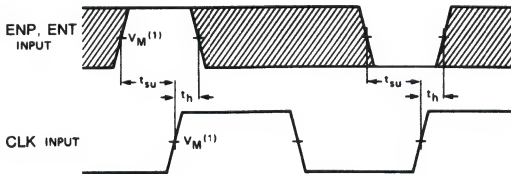


Fig. 7 Waveforms showing the ENP and ENT set-up and hold times.

Note to Figs 5, 6 and 7

The shaded areas indicate when the input is permitted to change for predictable output performance.

Note to AC waveforms

- (1) HC : $V_M=50\%$; $V_I=GND$ to V_{CC} ;
HCT : $V_M=1.3V$; $V_I=GND$ to $3V$.

GD54/74HC163, GD54/74HCT163

SYNCHRONOUS BINARY COUNTER WITH SYNCHRONOUS CLEAR

General Description

These devices are identical in pinout to the 54/74LS163. They contain a 4-bit binary counter consisting of four flip-flops. All flip-flops are clocked simultaneously on the positive edge of the clock input. Counters may be preset using the load input at the rising edge of clock. All the counters may be cleared synchronously by utilizing the clear input. That is, the counters are cleared on the positive edge of the clock while the clear input is held low. The HC/HCT 163 is similar in function to the HC/HCT 161 which is cleared asynchronously. These devices are characterized for operation over wide temperature ranges to meet industry and military specifications.

Features

- Low Power consumption characteristic of CMOS devices
- Output drive capability: 10 LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts
for HCT 4.5 to 5.5 volts
- Low input current: $1\mu\text{A}$ Max.
- Low quiescent current: $80\mu\text{A}$ Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs

Function Table

OPERATING MODE	INPUTS					OUTPUTS		
	$\overline{\text{CLR}}$	CLK	ENP	ENT	LOAD	D_n	Q_n	RCO
reset (clear)	l	\uparrow	X	X	X	X	L	L
parallel load	h	\uparrow	X	X	l	l	L	L
	h	\uparrow	X	X	l	h	H	*
count	h	\uparrow	h	h	h	X	count	*
hold (do nothing)	h	X	l	X	h	X	q_n	*
	h	X	X	l	h	X	q_n	L

Note to function table

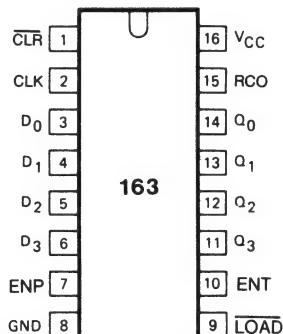
* The RCO output is HIGH when ENT is HIGH and the counter is at terminal count (HHHH).

h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CLK transition

l = LOW voltage level one set-up time prior to the LOW-to-HIGH CLK transition

q = lower case letters indicate the state of the referenced output one set-up time prior to the LOW-to-HIGH CLK transition

Pin Configuration



Suffix-Blank : Plastic Dual In Line Package
 Suffix-J : Ceramic Dual In Line Package
 Suffix-D : Small Outline Package

Logic Diagram

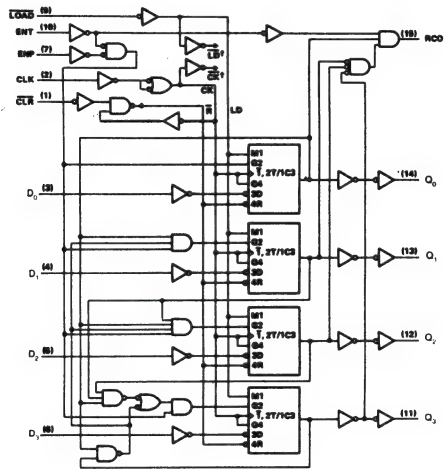


Fig. 1 Logic diagram

Output Sequence

- Illustrated below is the following sequence:
1. Clear outputs to zero (HC/HCT 163 is asynchronous)
 2. Preset to binary twelve
 3. Count to thirteen, fourteen, zero, one, and two
 4. Inhibit

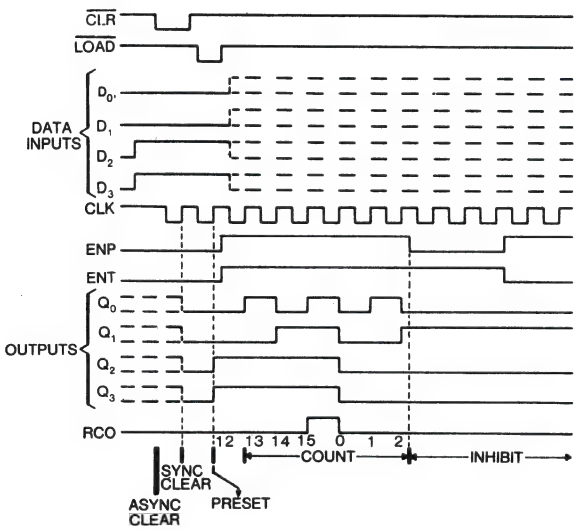


Fig. 2 Output Sequence

Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC Supply voltage		-0.5	+7	V
I_{IK}, I_{OK}	DC input or output diode current	for $V_I < -0.5$ or $V_I > V_{CC} + 0.5V$		[20]	mA
I_O	DC output source or sink current	for $-0.5V < V_O < V_{CC} + 0.5V$		[25]	mA
I_{CC}	DC V_{CC} or GND current			[50]	mA
T_{stg}	Storage temperature range		-65	150	°C
P_D	Power dissipation per package	above +70°C: derate linearly with 8mW/K		500	mW
T_L	Lead temperature	At distance 1/16±1/32 in. from case for 60 sec(CERAMIC) 10 sec(PLASTIC)		300 260	°C

Recommended Operating Conditions

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range V_{CC} : GD54/74HC Types GD54/74HCT Types	2 4.5	6 5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A : GD74 Types GD54 Types	-40 -55	+85 +125	°C
Input Rise and Fall times t_r, t_f : GD54/74HC Types at 2V at 4.5V at 6V GD54/74HCT Types at 4.5V		1000 500 400 500	ns

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HC163		GD54HC163		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2		1.5 3.15 4.2		V
V _{IL}	LOW level input voltage		2.0 4.5 6.0			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH}	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V
		or V _{IL}									
V _{OL}	LOW level output voltage	V _{IN} =V _{IH}	2.0 4.5 6.0			0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V
		or V _{IL}									
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	6.0			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	6.0			8		80		160	μA

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HCT163		GD54HCT163		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		4.5 to 5.5	2.0			2.0		2.0		V
V _{IL}	LOW level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH}	4.5	4.4	4.5		4.4		4.4		V
		or V _{IL}	4.5	3.98	4.3		3.84		3.7		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH}	4.5			0.1		0.1		0.1	V
		or V _{IL}	4.5		0.17	0.26		0.33		0.4	
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	5.5			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	5.5			8		80		160	μA

Timing Requirements for HC: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER		V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HC163		GD54HC163		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_w	Pulse width	CLK high or low	2.0	80	22		100		120		ns
			4.5	16	8		20		24		
			6.0	14	6		17		20		
t_{su}	Setup time	D_n to CLK	2.0	100	28		125		150		ns
			4.5	20	10		25		30		
			6.0	17	8		21		26		
		\overline{LOAD} to CLK	2.0	135	39		170		205		ns
			4.5	27	14		34		41		
			6.0	23	11		29		35		
		ENP, ENT to CLK	2.0	170	58		220		265		ns
			4.5	34	21		44		53		
			6.0	29	17		37		45		
		\overline{CLR} to CLK	2.0	100	28		125		150		ns
			4.5	20	10		25		30		
			6.0	17	8		21		26		
t_{rec}	Recovery time	\overline{CLR} to CLK	2.0	180	58		200		240		ns
			4.5	32	20		40		48		
			6.0	27	17		34		41		
t_h	Hold time	All sync, input to CLK	2.0	0			0		0		ns
			4.5	0			0		0		
			6.0	0			0		0		

AC Characteristics for HC: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER		V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HC163		GD54HC163		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
f_{max}	Maximum clock pulse frequency		2.0	6	14		5		4.2		MHz
			4.5	31	40		21		21		
			6.0	36	44		25		25		
t_{PLH}/t_{PHL}	Propagation Delay Time CLK to RCO		2.0		60	200		270		315	ns
			4.5		21	41		54		65	
			6.0		17	35		46		55	
t_{PLH}/t_{PHL}	Propagation Delay Time CLK to Qn		2.0		58	190		240		285	ns
			4.5		19	36		48		57	
			6.0		17	30		41		48	
t_{PLH}/t_{PHL}	Propagation Delay Time ENT to RCO		2.0		39	150		190		225	ns
			4.5		14	30		38		45	
			6.0		11	26		33		38	
t_{TLH}/t_{THL}	Output Transition Time		2.0		19	75		95		110	ns
			4.5		7	15		19		22	
			6.0		6	13		16		19	

Timing Requirements for HCT: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER		V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HCT163		GD54HCT163		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_w	Pulse width	CLK high or low	4.5	31	8		39		47		ns
t_{su}	Setup time	D_n to CLK	4.5	20	10		25		30		ns
		$\overline{\text{LOAD}}$ to CLK	4.5	35	16		44		53		ns
		ENP, ENT to CLK	4.5	40	23		50		60		ns
		$\overline{\text{CLR}}$ to CLK	4.5	20	12		25		30		ns
t_{rec}	Recovery time	$\overline{\text{CLR}}$ to CLK	4.5	32	20		41		50		ns
t_h	Hold time	All sync. input to CLK	4.5	0			0		0		ns

AC Characteristics for HCT: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HCT163		GD54HCT163		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
f_{max}	Maximum clock pulse frequency	4.5 5.5	16	28		13		11		MHz
$t_{PLH}/$ t_{PHL}	Propagation Delay Time CLK to RCO	4.5 5.5		26	51		64		77	ns
$t_{PLH}/$ t_{PHL}	Propagation Delay Time CLK to Qn	4.5 5.5		24	43		54		65	ns
$t_{PLH}/$ t_{PHL}	Propagation Delay Time ENT to RCO	4.5 5.5		20	45		56		68	ns
$t_{TLH}/$ t_{THL}	Output Transition Time	4.5 5.5		7	15		19		22	ns

AC Waveforms

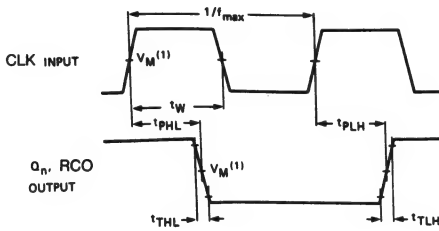


Fig. 3 Waveforms showing the clock (CLK) to outputs (Q_n , RCO) propagation delays, the clock pulse width, the output transition times and the maximum clock frequency.

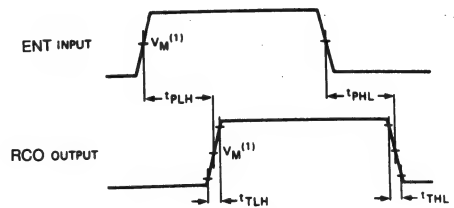


Fig. 4 Waveforms showing the input (ENT) to output (RCO) propagation delays and output transition times.

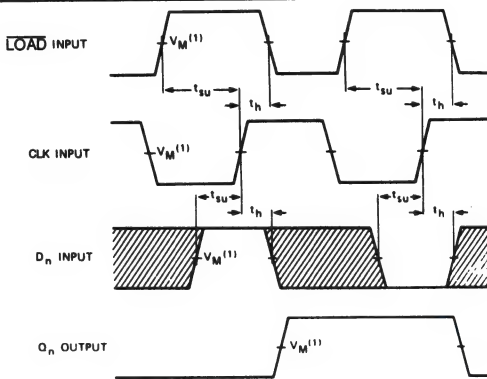


Fig. 5 Waveforms showing the set-up and hold times for the input (D_n) and parallel enable input (LOAD).

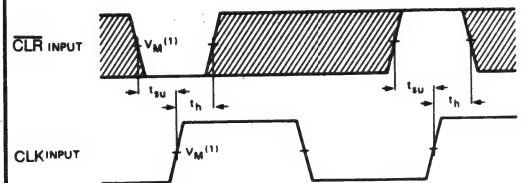


Fig. 6 Waveforms showing the \overline{CLR} set-up and hold times.

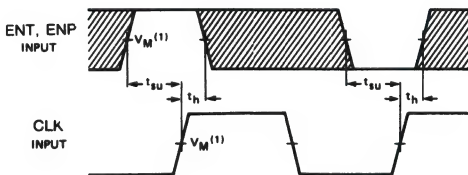


Fig. 7 Waveforms showing the ENT and ENP set-up and hold times.

Note to Figs 5, 6 and 7

The shaded areas indicate when the input is permitted to change for predictable output performance.

Note to AC waveforms

- (1) HC : $V_M = 50\%$; $V_I = \text{GND to } V_{CC}$.
HCT : $V_M = 1.3V$; $V_I = \text{GND to } 3V$.

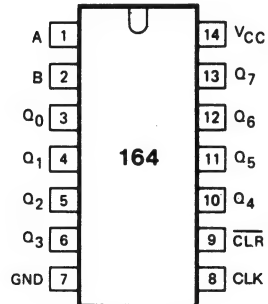
GD54/74HC164, GD54/74HCT164

8 BIT SERIAL-IN/PARALLEL-OUT SHIFT REGISTER

General Description

These devices are identical in pinout to the 54/74LS164. This circuit is an 8-bit, serial-input to parallel-output shift-register. Two serial data inputs are provided so that one input may be used as a data enable. Data at the serial inputs may be changed while the clock, is high or low, but only information meeting the setup and hold time requirements will be entered. Data is serially shifted in and out of the 8-bit register at the rising edge of the clock pulse, where each register is a D-type master/slave flip-flop. An asynchronous clear is provided, which is activated when a low level is present at its input. Clear is independent of the clock and accomplished by a low level at the clear input. These devices are characterized for operation over wide temperature ranges to meet industry and military specifications.

Pin Configuration



Suffix-Blank : Plastic Dual In Line Package
 Suffix-J : Ceramic Dual In Line Package
 Suffix-D : Small Outline Package

Features

- Low Power consumption characteristic of CMOS devices
- Output drive capability: 10 LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts
for HCT 4.5 to 5.5 volts
- Low input current: 1μA Max.
- Low quiescent current: 80μA Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs

Function Table

OPERATING MODES	INPUTS				OUTPUTS	
	CLR	CLK	A	B	Q ₀	Q ₁ —Q ₇
reset (clear)	L	X	X	X	L	L—L
shift	H	↑	l	l	L	q ₀ —q ₆
	H	↑	l	h	l	q ₀ —q ₀
	H	↑	h	l	L	q ₀ —q ₆
	H	↑	h	h	H	q ₀ —q ₀

h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition

l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition

q = lower case letters indicate the state of the referenced input one set-up time prior to the LOW-to-HIGH clock transition

Logic Diagram

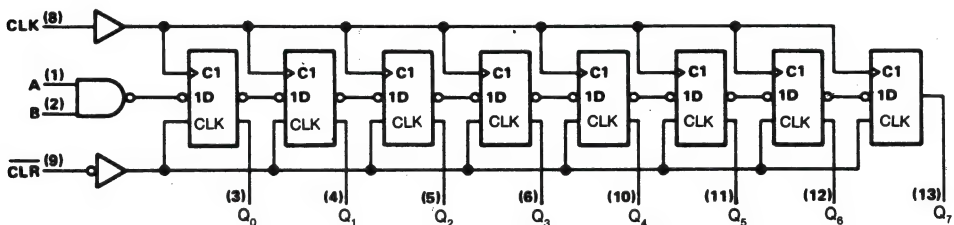


Fig. 1 Logic diagram

Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC Supply voltage		-0.5	+7	V
I_{IK}, I_{OK}	DC input or output diode current	for $V_I < -0.5$ or $V_I > V_{CC} + 0.5V$		20	mA
I_O	DC output source or sink current	for $-0.5V < V_O < V_{CC} + 0.5V$		25	mA
I_{CC}	DC V_{CC} or GND current			50	mA
T_{stg}	Storage temperature range		-65	150	°C
P_D	Power dissipation per package	above +70°C: derate linearly with 8mW/K		500	mW
T_L	Lead temperature	At distance 1/16 ± 1/32 in. from case for 60 sec(CERAMIC) 10 sec(PLASTIC)		300 260	°C

Recommended Operating Conditions

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range V_{CC} : GD54/74HC Types GD54/74HCT Types	2 4.5	6 5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A : GD74 Types GD54 Types	-40 -55	+85 +125	°C
Input Rise and Fall times t_r, t_f : GD54/74HC Types at 2V at 4.5V at 6V GD54/74HCT Types at 4.5 V		1000 500 400 500	ns

Typical Clear, Shift, and Clear Sequences

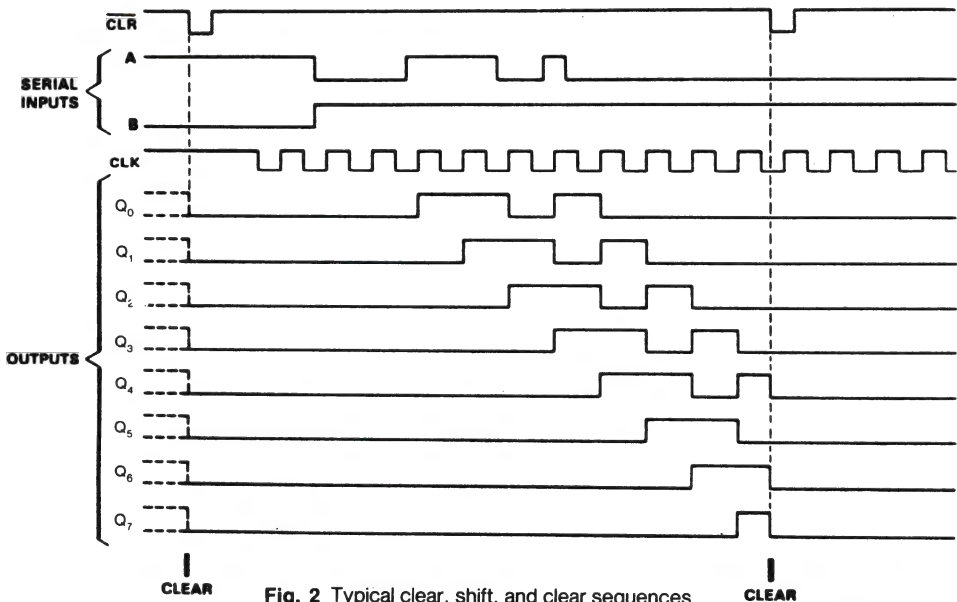


Fig. 2 Typical clear, shift, and clear sequences

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HC164		GD54HC164		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2		1.5 3.15 4.2		V
V _{IL}	LOW level input voltage		2.0 4.5 6.0			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH}	I _{OH} =-20μA	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0	1.9 4.4 5.9		1.9 4.4 5.9		V
			I _{OH} =-4mA	4.5 6.0	3.98 5.48	4.3 5.2	3.84 5.34		3.7 5.2		
		or V _{IL}	I _{OH} =-5.2mA	4.5 6.0	3.98 5.48	4.3 5.2	3.84 5.34		3.7 5.2		
			I _{OH} =-5.2mA	4.5 6.0	3.98 5.48	4.3 5.2	3.84 5.34		3.7 5.2		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH}	I _{OL} =20μA	2.0 4.5 6.0			0.1 0.1 0.1	0.1 0.1 0.1		0.1 0.1 0.1	V
			I _{OL} =4mA	4.5 6.0		0.17 0.15	0.26 0.26	0.33 0.33		0.4 0.4	
		or V _{IL}	I _{OL} =4mA	4.5 6.0		0.17 0.15	0.26 0.26	0.33 0.33		0.4 0.4	
			I _{OL} =5.2mA	4.5 6.0		0.17 0.15	0.26 0.26	0.33 0.33		0.4 0.4	
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	6.0			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	6.0			8		80		160	μA

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HCT164		GD54HCT164		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		4.5 to 5.5	2.0			2.0		2.0		V
V _{IL}	LOW level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH}	I _{OH} =-20μA	4.5	4.4	4.5	4.4		4.4		V
		or V _{IL}	I _{OH} =-4mA	4.5	3.98	4.3	3.84		3.7		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH}	I _{OL} =20μA	4.5			0.1	0.1		0.1	V
		or V _{IL}	I _{OL} =4mA	4.5		0.17	0.26	0.33		0.4	
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	5.5			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	5.5			8		80		160	μA

Timing Requirements for HC: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER		V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HC164		GD54HC164		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_w	Pulse width	$\overline{\text{CLR}}$ low	2.0	60			75		90		ns
			4.5	12			15		18		
			6.0	10			13		15		
		CLK high or low	2.0	80			100		120		ns
			4.5	16			20		24		
			6.0	14			17		20		
t_{su}	Setup time	A,B to CLK	2.0	60			75		90		ns
			4.5	12			15		18		
			6.0	10			13		15		
t_{rec}	Recovery time	$\overline{\text{CLR}}$ to CLK	2.0	60			75		90		ns
			4.5	12			15		18		
			6.0	10			13		15		
t_h	Hold time	A,B to CLK	2.0	5			5		5		ns
			4.5	5			5		5		
			6.0	5			5		5		

AC Characteristics for HC: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER		V_{CC}	$T_A=25^\circ\text{C}$			GD54HC164		GD74HC164		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
f_{max}	Maximum Clock Pulse Frequency		2.0	6	10		5		42		MHz
			4.5	31	54		25		21		
			6.0	36	62		28		25		
t_{PLH} / t_{PHL}	Propagation Delay Time $\overline{\text{CLR}}$ to Q_n		2.0		39	140		215		210	ns
			4.5		14	28		43		42	
			6.0		11	24		37		36	
t_{PLH} / t_{PHL}	Propagation Delay Time CLK to Q_n		2.0		41	170		175		110	ns
			4.5		15	34		35		22	
			6.0		12	29		30		19	
t_{TLH} / t_{THL}	Output Transition Time		2.0		19	75		95		100	ns
			4.5		7	15		19		22	
			6.0		6	13		16		18	

Timing Requirements for HCT : $t_r = t_f = 6\text{ns}$ $C_L = 50\text{ pF}$

SYMBOL	PARAMETER		V_{CC} (V)	$T_A = 25^\circ\text{C}$			GD74HCT164		GD54HCT164		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_w	Pulse width	$\overline{\text{CLR}}$ low	4.5	18			23		27		ns
		CLK high or low	4.5	18			23		27		ns
t_{su}	Setup time	A,B to CLK	4.5	16			20		24		ns
t_{rec}	Recovery time	$\overline{\text{CLR}}$ to CLK	4.5	16			20		24		ns
t_h	Hold time	A,B to CLK	4.5	5			5		5		ns

AC Characteristics for HCT : $t_r = t_f = 6\text{ns}$ $C_L = 50\text{ pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A = 25^\circ\text{C}$			GD74HCT164		GD54HCT164		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
f_{max}	Maximum Clock Pulse Frequency	4.5	27	55		22		18		MHz
$t_{PLH} /$ t_{PHL}	Propagation Delay Time $\overline{\text{CLR}}$ to Q_n	4.5		19	38		48		57	ns
$t_{PLH} /$ t_{PHL}	Propagation Delay Time CLK to Q_n	4.5		17	36		45		54	ns
$t_{TLH} /$ t_{THL}	Output Transition Time	4.5		7	15		19		22	ns

AC Waveforms

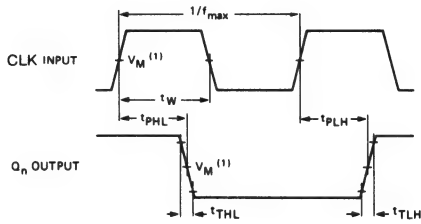


Fig. 3 Waveforms showing the clock (CLK) to output (Q_n) propagation delays, the clock pulse width, the output transition times and the maximum clock frequency.

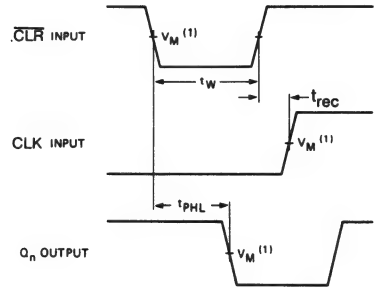


Fig. 4 Waveforms showing the master clear (\overline{CLR}) pulse width, the master clear, to output (Q_n) propagation delays and the master clear to clock (CLK) recovery time.

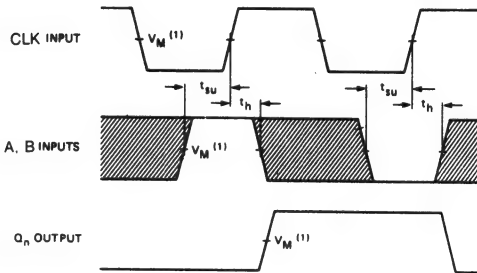


Fig. 5 Waveforms showing the data set-up and hold times for A,B inputs.

Note to AC waveforms

- (1) HC : $V_M = 50\%$; $V_I = \text{GND to } V_{CC}$.
HCT : $V_M = 1.3V$; $V_I = \text{GND to } 3V$.

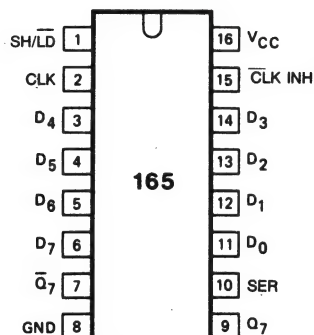
GD54/74HC165, GD54/74HCT165

8-BIT PARALLEL-IN/SERIAL-OUT SHIFT REGISTER

General Description

These devices are identical in pinout to the 54/74LS165. This circuit is an 8-bit, parallel-input to serial-output shift register with complementary outputs from the last stage. Data may be loaded into the register either in parallel or in serial form. When the serial shift/parallel load input is low, the data is loaded asynchronously in parallel. When it is high, the data is loaded serially on the rising edge of either clock 1 or clock 2. Clocking is accomplished through a 2-input NOR gate permitting one input to be used as a clock inhibit function. These devices are characterized for operation over wide temperature ranges to meet industry and military specifications.

Pin Configuration



Suffix-Blank : Plastic Dual In Line Package
 Suffix-J : Ceramic Dual In Line Package
 Suffix-D : Small Outline Package

Features

- Low Power consumption characteristic of CMOS devices
- Output drive capability: 10 LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts
for HCT 4.5 to 5.5 volts
- Low input current: 1μA Max.
- Low quiescent current: 80μA Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs

Function Table

OPERATING MODES	INPUTS					Q _n REGISTERS			OUTPUTS	
	SH/LD	CLK INH	CLK	SER	D _n	Q ₀	Q ₁ -Q ₆	Q ₇	Q ₇	Q ₇
parallel load	L	X	X	X	L	L	L-L	L	L	H
	L	X	X	X	H	H	H-H	H	H	L
serial shift	H	L	↑	l	X	L	q ₀ -q ₅	q ₆	q ₆	q ₆
	H	L	↑	h	X	H	q ₀ -q ₅	q ₆	q ₆	q ₆
hold "do nothing"	H	H	X	X	X	q ₀	q ₁ -q ₆	q ₇	q ₇	q ₇

H = HIGH voltage level
 h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CLK transition
 L = LOW voltage level
 l = LOW voltage level one set-up time prior to the LOW-to-HIGH CLK transition
 q = lower case letters indicate the state of the referenced output one set-up time prior to the LOW-to-HIGH CLK transition
 X = don't care
 ↑ = LOW-to-HIGH CLK transition

Logic Diagram

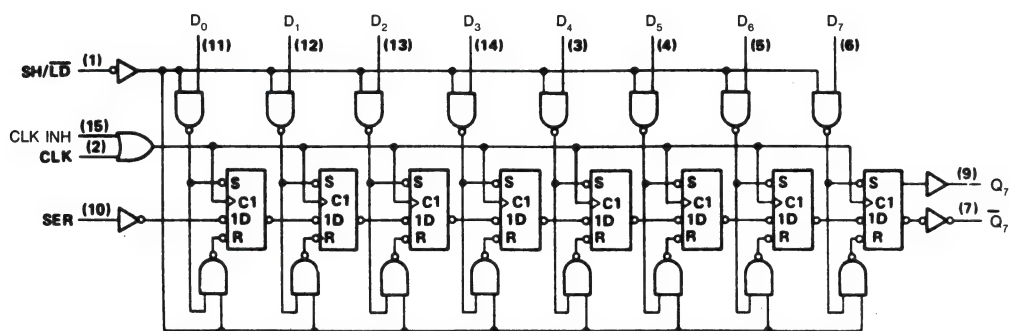


Fig. 1 Logic diagram

Typical Shift, Load, and Inhibit Sequences

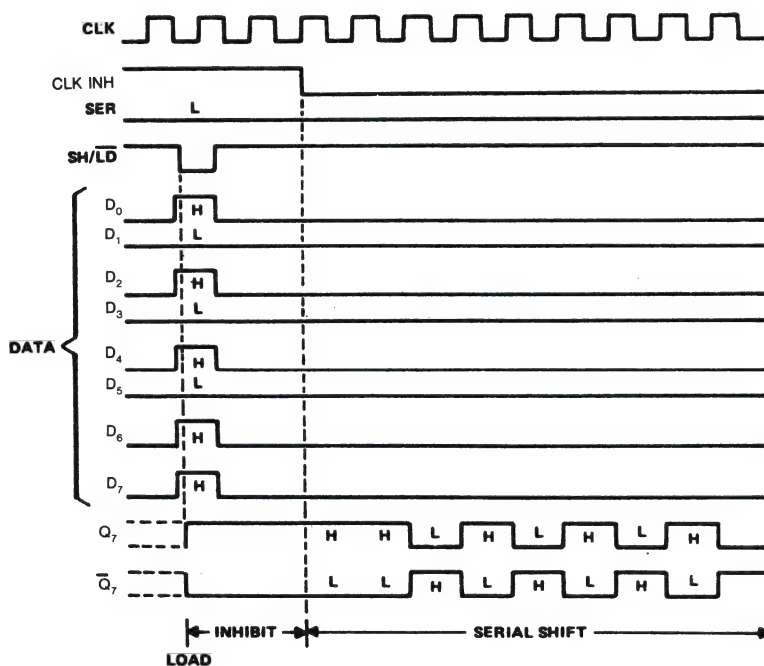


Fig. 2 Typical shift, load, and inhibit sequences

Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC Supply voltage		-0.5	+7	V
I_{IK}, I_{OK}	DC input or output diode current	for $V_I < -0.5$ or $V_I > V_{CC} + 0.5V$		20	mA
I_O	DC output source or sink current	for $-0.5V < V_O < V_{CC} + 0.5V$		25	mA
I_{CC}	DC V_{CC} or GND current			50	mA
T_{stg}	Storage temperature range		-65	150	°C
P_D	Power dissipation per package	above +70°C: derate linearly with 8mW/K		500	mW
T_L	Lead temperature	At distance 1/16 ± 1/32 in. from case for 60 sec(CERAMIC) 10 sec(PLASTIC)		300 260	°C

Recommended Operating Conditions

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range V_{CC} : GD54/74HC Types GD54/74HCT Types	2 4.5	6 5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A : GD74 Types GD54 Types	-40 -55	+85 +125	°C
Input Rise and Fall times t_r, t_f : GD54/74HC Types at 2V at 4.5V at 6V GD54/74HCT Types at 4.5 V		1000 500 400 500	ns

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HC165		GD54HC165		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2		1.5 3.15 4.2		V
V _{IL}	LOW level input voltage		2.0 4.5 6.0			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH}	I _{OH} =-20μA	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0	1.9 4.4 5.9		1.9 4.4 5.9		V
			I _{OH} =-4mA	4.5 6.0	3.98 5.48	4.3 5.2	3.84 5.34		3.7 5.2		
		or V _{IL}	I _{OH} =-5.2mA	4.5 6.0	3.98 5.48	4.3 5.2	3.84 5.34		3.7 5.2		
			I _{OH} =-5.2mA	4.5 6.0	3.98 5.48	4.3 5.2	3.84 5.34		3.7 5.2		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH}	I _{OL} =20μA	2.0 4.5 6.0			0.1 0.1 0.1	0.1 0.1 0.1		0.1 0.1 0.1	V
			I _{OL} =4mA	4.5 6.0		0.17 0.15	0.26 0.26	0.33 0.33		0.4 0.4	
		or V _{IL}	I _{OL} =4mA	4.5 6.0		0.17 0.15	0.26 0.26	0.33 0.33		0.4 0.4	
			I _{OL} =5.2mA	4.5 6.0		0.17 0.15	0.26 0.26	0.33 0.33		0.4 0.4	
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	6.0			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	6.0			8		80		160	μA

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HCT165		GD54HCT165		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		4.5 to 5.5	2.0			2.0		2.0		V
V _{IL}	LOW level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH}	I _{OH} =-20μA	4.5	4.4	4.5	4.4		4.4		V
		or V _{IL}	I _{OH} =-4mA	4.5	3.98	4.3	3.84		3.7		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH}	I _{OL} =20μA	4.5		0.1	0.1	0.1		0.1	V
		or V _{IL}	I _{OL} =4mA	4.5		0.17	0.26	0.33		0.4	
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	5.5			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	5.5			8		80		160	μA

Timing Requirements for HC: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER		V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HC165		GD54HC165		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_w	Pulse width	SH/ $\overline{\text{LD}}$ low, CLK	2.0 4.5 6.0	80 16 14			100 20 17		120 24 21		ns
t_{su}	Setup time	SH/ $\overline{\text{LD}}$ to CLK	2.0 4.5 6.0	80 16 14			100 20 17		120 24 20		ns
		SER to CLK	2.0 4.5 6.0	40 8 7			50 10 9		60 12 10		ns
		CLK INH low before CLK \uparrow	2.0 4.5 6.0	100 20 17			125 25 21		150 30 25		ns
		CLK INH high before CLK \downarrow	2.0 4.5 6.0	40 8 7			50 10 9		60 12 10		ns
		D_n to SH/ $\overline{\text{LD}}$	2.0 4.5 6.0	100 20 17			125 25 21		150 30 25		ns
t_h	Hold time	SER to CLK D_n to SH/ $\overline{\text{LD}}$	2.0 4.5 6.0	5 5 5			5 5 5		5 5 5		ns

AC Characteristics for HC: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER		V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HC165		GD54HC165		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
f_{max}	Maximum Clock Pulse Frequency		2.0 4.5 6.0	6 31 36	13 50 62		5 25 29		4.2 21 25		MHz
$t_{PLH}/$ t_{PHL}	Propagation Delay Time SH/ $\overline{\text{LD}}$ to Q_7 or \overline{Q}_7		2.0 4.5 6.0		50 18 14	165 33 28		205 41 35		250 50 43	ns
$t_{PLH}/$ t_{PHL}	Propagation Delay Time CLK to Q_7 or \overline{Q}_7		2.0 4.5 6.0		52 19 15	165 33 28		205 41 35		250 50 23	ns
$t_{PLH}/$ t_{PHL}	Propagation Delay Time D_7 to Q_7 or \overline{Q}_7		2.0 4.5 6.0		36 13 10	120 24 20		150 30 26		180 86 31	ns
$t_{TLH}/$ t_{THL}	Output Transition Time		2.0 4.5 6.0		19 7 6	75 15 13		95 19 16		110 22 19	ns

Timing Requirements for HCT: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER		V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HCT165		GD54HCT165		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_w	Pulse width	SH/ $\overline{\text{LD}}$ low, CLK	4.5	20			24		28		ns
t_{su}	Setup time	SH/ $\overline{\text{LD}}$ to CLK	4.5	20			24		28		ns
		SER to CLK	4.5	10			14		16		ns
		CLK INH low before CLK \uparrow	4.5	20			29		34		ns
		CLK INH high before CLK \downarrow	4.5	10			14		16		ns
		D_n to SH/ $\overline{\text{LD}}$	4.5	20			24		28		ns
t_h	Hold time	SER to CLK D_n to SH/ $\overline{\text{LD}}$	4.5	5			5		5		ns

AC Characteristics for HCT: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HCT165		GD54HCT165		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
f_{max}	Maximum Clock Pulse Frequency	4.5	27	45		21		18		MHz
$t_{\text{PLH}}/$ t_{PHL}	Propagation Delay Time SH/ $\overline{\text{LD}}$ to Q_7 or \overline{Q}_7	4.5		20	40		50		60	ns
$t_{\text{PLH}}/$ t_{PHL}	Propagation Delay Time CLK to Q_7 or \overline{Q}_7	4.5		17	34		43		51	ns
$t_{\text{PLH}}/$ t_{PHL}	Propagation Delay Time D_7 to Q_7 or \overline{Q}_7	4.5		14	28		35		42	ns
$t_{\text{TLH}}/$ t_{THL}	Output Transition Time	4.5		7	15		79		22	ns

AC Waveforms

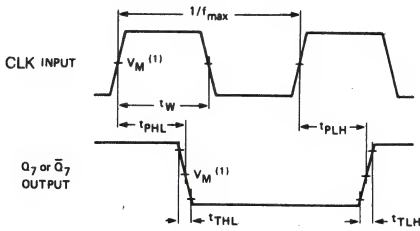


Fig. 3 Waveforms showing the clock (CLK) to output (Q_7 or \bar{Q}_7) propagation delays, the clock pulse width, the output transition times and the maximum clock frequency.

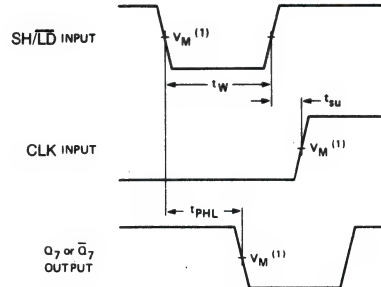


Fig. 4 Waveforms showing the parallel load (SH/LD) pulse width, the parallel load to output (Q_7 or \bar{Q}_7) propagation delays and the parallel load to clock (CLK) set-up time.

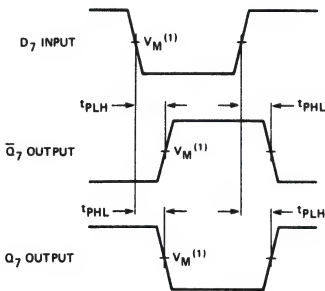


Fig. 5 Waveforms showing the data input (D_n) to output (Q_7 or \bar{Q}_7) propagation delays when (SH/LD) is LOW.

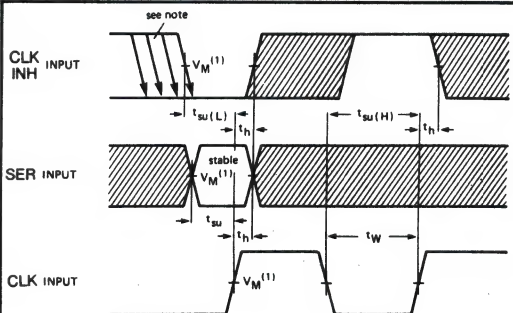


Fig. 6. Waveforms showing the set-up and hold times from the serial data input (SER) to the clock (CLK), from the clock enable input (LOW CLK INH) to the clock (CLK) and from the clock enable input CLK INH to the clock (CLK).

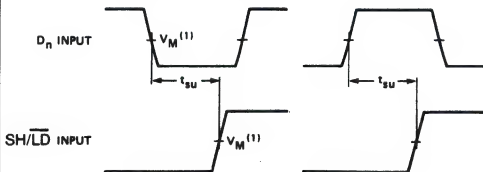


Fig. 7 Waveforms showing the set-up and hold times from the data inputs D_5 and D_7 to the parallel load input (SH/LD)

Note to Figs 3 and 4

The changing to output assumes internal Q_6 opposite state from Q_7 .

Note to Fig. 6

(CLK INH) may change only from HIGH-to-LOW while CLK is LOW.

The shaded areas indicate when the input is permitted to change for predictable output performance.

Note to AC waveforms

(1) HC : $V_M = 50\%$; $V_I = GND$ to V_{CC} .

HCT : $V_M = 1.3V$; $V_I = GND$ to $3V$.

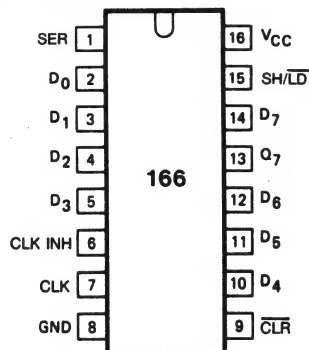
GD54/74HC166, GD54/74HCT166

8-BIT SERIAL OR PARALLEL-INPUT/SERIAL-OUTPUT SHIFT REGISTER WITH CLEAR

General Description

These devices are identical in pinout to the 54/74LS166. This circuit is an 8-bit shift register with an output from the last stage. Data may be loaded into the register in either parallel or serial form. When the shift/load input is low, the data is loaded asynchronously in parallel. When it is high, the data is loaded serially on the rising edge of either clock1 or clock2. Clear is asynchronous and active-low. Clocking is accomplished through a 2-input NOR gate permitting one input to be used as a clock inhibit function. These devices are characterized for operation over wide temperature ranges to meet industry and military specifications.

Pin Configuration



Suffix-Blank : Plastic Dual In Line Package
 Suffix-J : Ceramic Dual In Line Package
 Suffix-D : Small Outline Package

Features

- Low Power consumption characteristic of CMOS devices
- Output drive capability: 10 LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts
for HCT 4.5 to 5.5 volts
- Low input current: 1 μ A Max.
- Low quiescent current: 80 μ A Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs

Function Table

OPERATING MODES	INPUTS				Q _n REGISTER			OUTPUT
	SH/LD	CLK INH	CLK	SER	D _n	Q ₀	Q ₁ -Q ₆	
parallel load	L	L	↑	X	L-H	L	L-L	L
	L	L	↑	X	h-h	H	H-H	H
serial shift	h	L	↑	L	X-X	L	q ₀ -q ₅	q ₆
	h	L	↑	h	X-X	H	q ₀ -q ₆	q ₆
hold "do nothing"	X	h	X	X	X-X	q ₀	q ₁ -q ₆	q ₇

H = HIGH voltage level
 h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CLK transition
 L = LOW voltage level
 l = LOW voltage level one set-up time prior to the LOW-to-HIGH CLK transition
 q = lower case letters indicate the state of the referenced output one set-up time prior to the LOW-to-HIGH CLK transition
 X = don't care
 ↑ = LOW-to-HIGH CLK transition

Logic Diagram

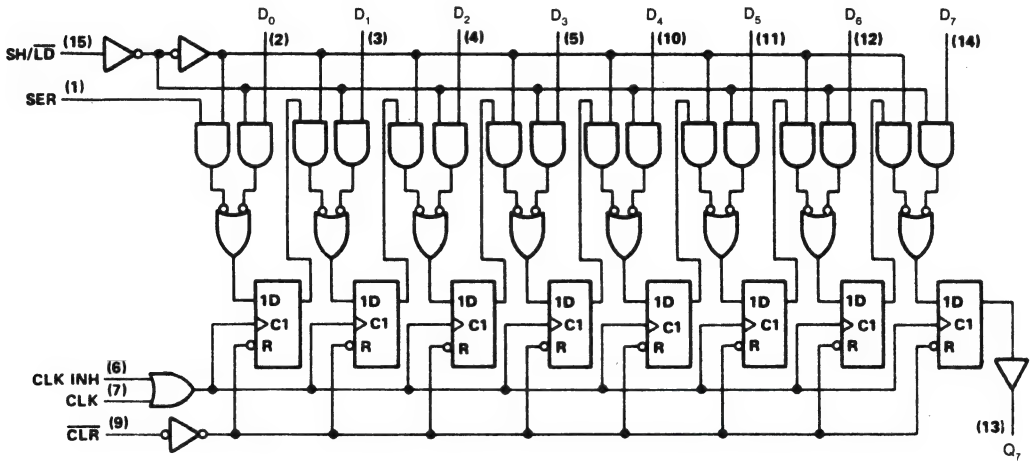


Fig. 1 Logic diagram

Typical Clear Shift, Load, Inhibit, and Shift Sequences

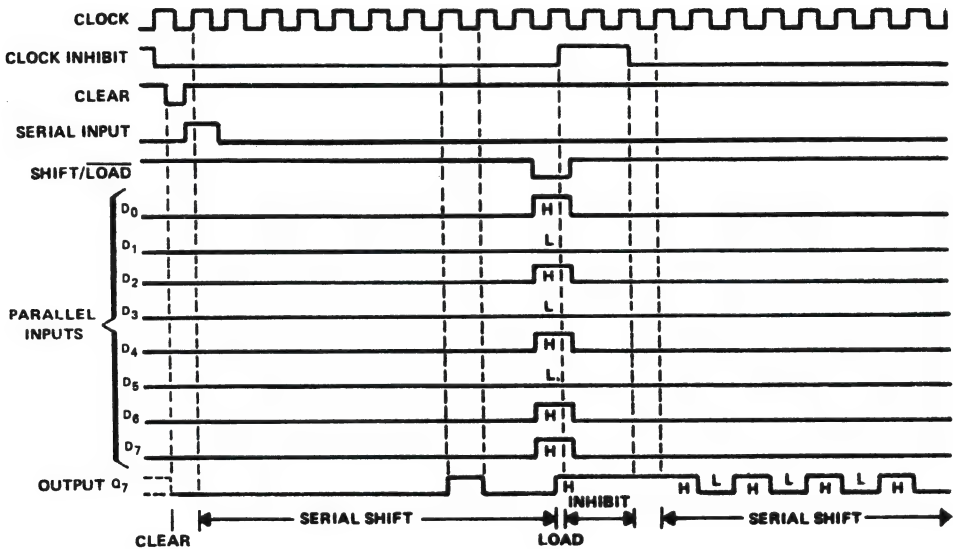


Fig. 2 Typical clear shift, load, inhibit, and shift sequences

Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC Supply voltage		-0.5	+7	V
I_{IK}, I_{OK}	DC input or output diode current	for $V_I < -0.5$ or $V_I > V_{CC} + 0.5V$		20	mA
I_O	DC output source or sink current	for $-0.5V < V_O < V_{CC} + 0.5V$		25	mA
I_{CC}	DC V_{CC} or GND current			50	mA
T_{stg}	Storage temperature range		-65	150	°C
P_D	Power dissipation per package	above +70°C: derate linearly with 8mW/K		500	mW
T_L	Lead temperature	At distance 1/16±1/32 in. from case for 60 sec(CERAMIC) 10 sec(PLASTIC)		300 260	°C

Recommended Operating Conditions

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range V_{CC} : GD54/74HC Types GD54/74HCT Types	2 4.5	6 5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A : GD74 Types GD54 Types	-40 -55	+85 +125	°C
Input Rise and Fall times t_r, t_f : GD54/74HC Types at 2V at 4.5V at 6V GD54/74HCT Types at 4.5 V		1000 500 400 500	ns

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HC166		GD54HC166		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2		1.5 3.15 4.2		V
V _{IL}	LOW level input voltage		2.0 4.5 6.0			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH}	I _{OH} =-20μA	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9	V
			I _{OH} =-4mA I _{OH} =-5.2mA	4.5 6.0	3.98 5.48	4.3 5.2		3.84 5.34		3.7 5.2	
		or V _{IL}	I _{OL} =20μA	2.0 4.5 6.0			0.1 0.1 0.1	0.1 0.1 0.1		0.1 0.1 0.1	
			I _{OL} =4mA I _{OL} =5.2mA	4.5 6.0		0.17 0.15	0.26 0.26	0.33 0.33		0.4 0.4	
V _{OL}	LOW level output voltage	V _{IN} =V _{IH} or V _{IL}	I _{OL} =20μA I _{OL} =4mA I _{OL} =5.2mA	2.0 4.5 6.0 4.5 6.0			0.1 0.1 0.1 0.17 0.15	0.1 0.1 0.1 0.33 0.33		0.1 0.1 0.1 0.4 0.4	V
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND		6.0			0.1	1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA		6.0		8		80		160	μA

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HCT166		GD54HCT166		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		4.5 to 5.5	2.0			2.0		2.0		V
V _{IL}	LOW level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH}	I _{OH} =-20μA	4.5	4.4	4.5		4.4		4.4	V
		or V _{IL}	I _{OH} =-4mA	4.5	3.98	4.3		3.84		3.7	
V _{OL}	LOW level output voltage	V _{IN} =V _{IH}	I _{OL} =20μA	4.5			0.1	0.1		0.1	V
		or V _{IL}	I _{OL} =4mA	4.5		0.17	0.26	0.33		0.4	
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND		5.5			0.1	1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA		5.5		8		80		160	μA

Timing Requirements for HC : $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER		V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HC166		GD54HC166		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_w	Pulse width	$\overline{\text{CLR}}$ low	2.0 4.5 6.0	100 20 17			125 25 21		150 30 26		ns
		CLK high or low	2.0 4.5 6.0	80 16 14			100 20 17		120 24 20		ns
t_{su}	Setup time	SH/ $\overline{\text{LD}}$ to CLK	2.0 4.5 6.0	120 25 21			160 31 26		200 40 34		ns
		SER to CLK	2.0 4.5 6.0	80 16 14			100 20 17		120 24 20		ns
		CLK INH low before CLK \uparrow	2.0 4.5 6.0	100 20 17			125 25 21		150 30 26		ns
		D_n to SH/ $\overline{\text{LD}}$	2.0 4.5 6.0	80 16 14			100 20 17		120 24 20		ns
t_{rec}	Recovery time	$\overline{\text{CLR}}$ to CLK	2.0 4.5 6.0	40 8 7			50 10 9		60 12 10		ns
t_h	Hold time	SH/ $\overline{\text{LD}}$ to CLK	2.0 4.5 6.0	0 0 0			0 0 0		0 0 0		ns
		SER to CLK	2.0 4.5 6.0	5 5 5			5 5 5		5 5 5		ns
		CLK INH after CLK \uparrow	2.0 4.5 6.0	0 0 0			0 0 0		0 0 0		ns
		D_n to SH/ $\overline{\text{LD}}$	2.0 4.5 6.0	5 5 5			5 5 5		5 5 5		ns
		$\overline{\text{CLR}}$ active after CLK \uparrow	2.0 4.5 6.0	0 0 0			0 0 0		0 0 0		ns

AC Characteristics for HC: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HC166		GD54HC166		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
f_{max}	Maximum Clock Pulse Frequency	2.0 4.5 6.0	6 31 36	18 50 60		5 25 29		4.2 21 25		MHz
t_{PLH}/t_{PHL}	Propagation Delay Time $\overline{\text{CLR}}$ to Q_7	2.0 4.5 6.0		47 16 12	120 24 20		150 30 26		180 36 31	ns
t_{PLH}/t_{PHL}	Propagation Delay Time CLK to Q_7	2.0 4.5 6.0		50 14 12	125 30 26		190 38 32		225 45 38	ns
t_{TLH}/t_{THL}	Output Transition Time	2.0 4.5 6.0		19 7 6	75 15 13		95 19 16		110 22 19	ns

Timing Requirements for HCT: $t_r = t_f = 6\text{ns}$ $C_L = 50\text{ pF}$

SYMBOL	PARAMETER		V_{CC} (V)	$T_A = 25^\circ\text{C}$			GD74HCT166		GD54HCT166		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_w	Pulse width	$\overline{\text{CLR}}$ low	4.5	22			27		32		ns
		CLK high or low	4.5	18			22		26		ns
t_{su}	Setup time	SH/ $\overline{\text{LD}}$ to CLK	4.5	27			32		40		ns
		SER to CLK	4.5	18			22		26		ns
		CLK INH low to CLK	4.5	22			27		32		ns
		Data before SH/ $\overline{\text{LD}}$ \uparrow	4.5	18			22		26		ns
t_{rec}	Recovery time	$\overline{\text{CLR}}$ to CLK	4.5	10			12		14		ns
t_h	Hold time	SH/ $\overline{\text{LD}}$ to CLK	4.5	0			0		0		ns
		SER to CLK	4.5	5			5		5		ns
		CLK INH to CLK	4.5	0			0		0		ns
		Data after SH/ $\overline{\text{LD}}$ \uparrow	4.5	5			5		5		ns
		$\overline{\text{CLR}}$ inactive after CLK \uparrow	4.5	0			0		0		ns

AC Characteristics for HCT: $t_r = t_f = 6\text{ns}$ $C_L = 50\text{ pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A = 25^\circ\text{C}$			GD74HCT166		GD54HCT166		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
f_{max}	Maximum Clock Pulse Frequency	4.5	29	45		23		19		MHz
$t_{PLH}/$ t_{PHL}	Propagation Delay Time $\overline{\text{CLR}}$ to Q_7	4.5		20	28		34		38	ns
$t_{PLH}/$ t_{PHL}	Propagation Delay Time CLK to Q_7	4.5		18	32		38		45	ns
$t_{TLH}/$ t_{THL}	Output Transition Time	4.5		7	15		19		22	ns

AC Waveforms

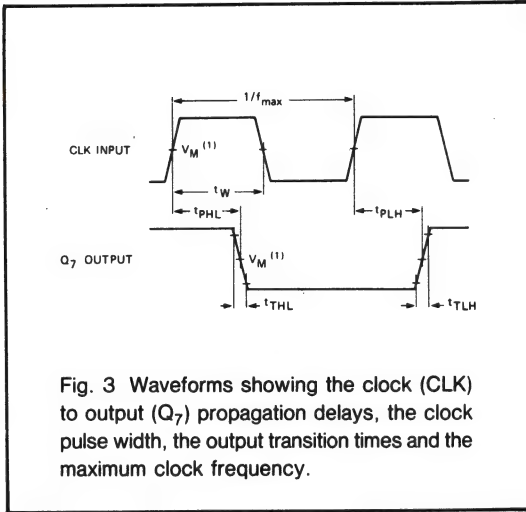


Fig. 3 Waveforms showing the clock (CLK) to output (Q₇) propagation delays, the clock pulse width, the output transition times and the maximum clock frequency.

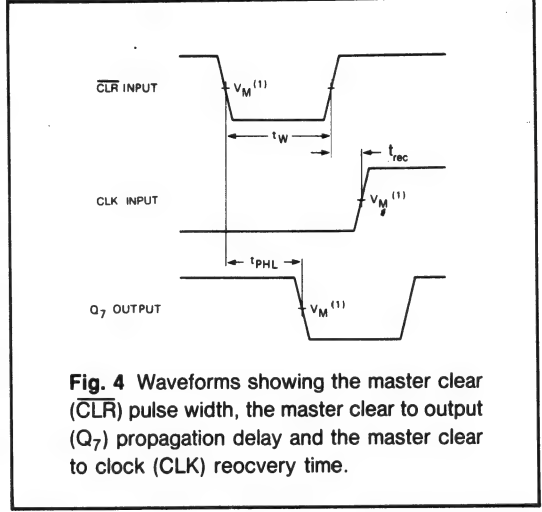


Fig. 4 Waveforms showing the master clear (\overline{CLR}) pulse width, the master clear to output (Q₇) propagation delay and the master clear to clock (CLK) recovery time.

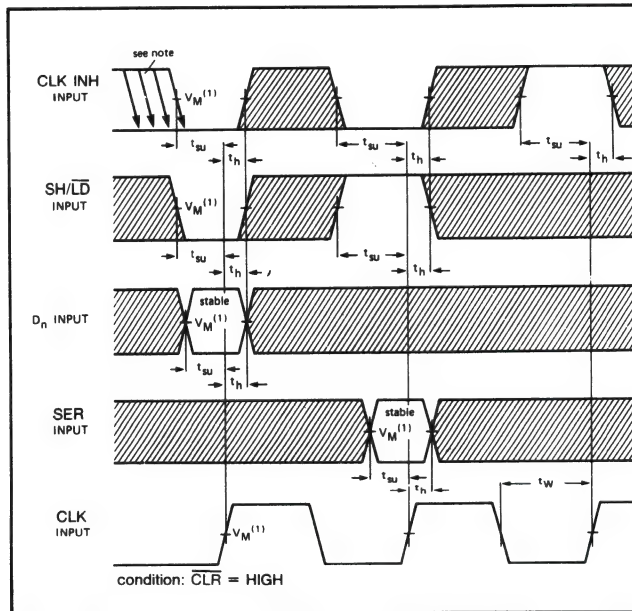


Fig. 5 Waveforms showing the set-up and hold times from the serial data input (SER), the data inputs (D_n), the clock enable input (LOW CLK INH), the clock enable input CLK INH and the parallel enable input to the clock (CLK).

Note to Fig. 3

The changing to output assumes internal Q₆ opposite state from Q₇.

Note to Figs 3, 4 and 5

The number of clock pulse required between the t_{PLH} and t_{PHL} measurements can be determined from the function table.

Note to Fig. 5

CLK INH may change only from HIGH-to-LOW while CLK is LOW.

The shaded areas indicate when the input is permitted to change for predictable output performance.

Note to AC waveforms

- (1) HC : $V_M = 50\%$; $V_I = \text{GND}$ to V_{CC} .
HCT : $V_M = 1.3V$; $V_I = \text{GND}$ to $3V$.

GD54/74HC173, GD54/74HCT173

QUAD 3-STATE D-TYPE FLIP-FLOPS WITH COMMON CLOCK & CLEAR

General Description

These devices are identical in pinout to the 54/74LS173. They consist of four D-type flip-flops operating synchronously from a common Clock and clear. Data, when enabled, are clocked into the four D-type flip-flops on the rising edge of the common clock. When either or both of the output enable controls is high, the outputs are in a high-impedance state. The clear feature is asynchronous and active-high. These devices are characterized for operation over wide temperature ranges to meet industry and military specifications.

Features

- Low Power consumption characteristic of CMOS devices
- Output drive capability: 15 LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts
for HCT 4.5 to 5.5 volts
- Low input current: 1 μ A Max.
- Low quiescent current: 80 μ A Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs

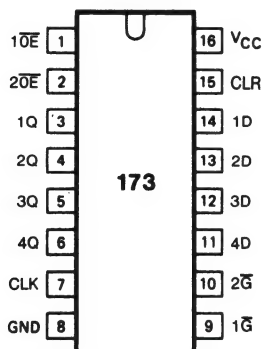
Function Table

REGISTER OPERATING MODES	INPUTS					OUTPUTS
	CLR	CLK	1 \bar{G}	2 \bar{G}	nD	nQ (register)
clear	H	X	X	X	X	L
parallel load	L	\uparrow	L	L	L	L
	L	\uparrow	L	L	H	H
hold (no change)	L	X	h	X	X	q _n
	L	X	X	h	X	q _n

3-STATE BUFFER OPERATING MODES	INPUTS			OUTPUTS			
	nQ (register)	1OE	2OE	1Q	2Q	3Q	4Q
read	L	L	L	L	L	L	L
	H	L	L	H	H	H	H
disabled	X	H	X	Z	Z	Z	Z
	X	X	H	Z	Z	Z	Z

H = HIGH voltage level
 h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CLK transition
 L = LOW voltage level
 l = LOW voltage level one set-up time prior to the LOW-to-HIGH CLK transition
 q = lower case letters indicate the state of the referenced input (or output) one set-up time prior to the LOW-to-HIGH CLK transition
 X = don't care
 Z = high impedance OFF-state
 \uparrow = LOW-to-HIGH CLK transition

Pin Configuration



Suffix-Blank : Plastic Dual In Line Package
 Suffix-J : Ceramic Dual In Line Package
 Suffix-D : Small Outline Package

Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC Supply voltage		-0.5	+7	V
I_{IK}, I_{OK}	DC input or output diode current	for $V_I < -0.5$ or $V_I > V_{CC} + 0.5V$		20	mA
I_O	DC output source or sink current	for $-0.5V < V_O < V_{CC} + 0.5V$		35	mA
I_{CC}	DC V_{CC} or GND current			70	mA
T_{stg}	Storage temperature range		-65	150	°C
P_D	Power dissipation per package	above +70°C: derate linearly with 8mW/K		500	mW
T_L	Lead temperature	At distance $1/16 \pm 1/32$ in. from case for 60 sec(CERAMIC) 10 sec(PLASTIC)		300 260	°C

Recommended Operating Conditions

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range V_{CC} : GD54/74HC Types GD54/74HCT Types	2 4.5	6 5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A : GD74 Types GD54 Types	-40 -55	+85 +125	°C
Input Rise and Fall times t_r, t_f : GD54/74HC Types at 2V at 4.5V at 6V GD54/74HCT Types at 4.5V		1000 500 400 500	ns

Logic Diagram

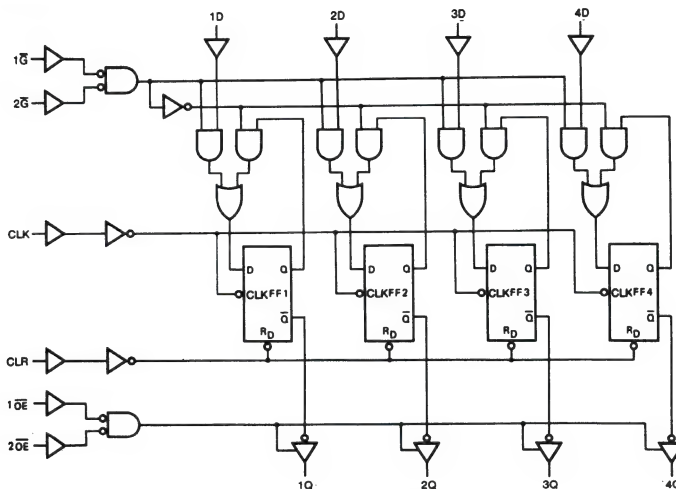


Fig. 1 Logic symbol

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION		V _{CC} (V)	T _A =25°C			GD74HC173		GD54HC173		UNIT	
					MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.		
V _{IH}	HIGH level input Voltage			2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2		1.5 3.15 4.2		V	
V _{IL}	LOW level input voltage			2.0 4.5 6.0			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V	
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH}	I _{OH} =-20μA	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V	
			or V _{IL}	I _{OH} =-6mA I _{OH} =-7.8mA	4.5 6.0	3.98 5.48	4.3 5.2		3.84 5.34		3.7 5.2		
		or V _{IL}		I _{OL} =20μA	2.0 4.5 6.0			0.1 0.1 0.1		0.1 0.1 0.1			0.1 0.1 0.1
			I _{OL} =6mA I _{OL} =7.8mA	4.5 6.0		0.17 0.15	0.26 0.26		0.33 0.33		0.4 0.4		
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND		6.0			0.1		1.0		1.0	μA	
I _{OZ}	Three-State leakage current	V _{IN} =V _{IH} or V _{IL}	V _O =V _{CC} or GND	6.0		0.01	0.5		5.0		10.0	μA	
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA		6.0			8		80		160	μA	

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION		V _{CC} (V)	T _A =25°C			GD74HCT173		GD54HCT173		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage			4.5 to 5.5	2.0			2.0		2.0		V
V _{IL}	LOW level input voltage			4.5 to 5.5			0.8		0.8		0.8	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH}	I _{OH} =-20μA	4.5	4.4	4.5		4.4		4.4		V
		or V _{IL}	I _{OH} =-6mA	4.5	3.98	4.3		3.84		3.7		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH}	I _{OL} =20μA	4.5			0.1		0.1		0.1	V
		or V _{IL}	I _{OL} =6mA	4.5		0.17	0.26		0.33		0.4	
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND		5.5			0.1		1.0		1.0	μA
I _{OZ}	Three-State leakage current	V _{IN} =V _{IH} or V _{IL}	V _O =V _{CC} or GND	5.5		0.01	0.5		5.0		10.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA		5.5		0.01	8		80		160	μA

Timing Requirements for HC: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER		V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HC173		GD54HC173		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_w	Pulse width	CLR	2.0	80	30		100		120		ns
			4.5	16	10		20		25		
			6.0	14	8		18		22		
		CLK	2.0	80	30		100		120		ns
			4.5	16	10		20		25		
			6.0	14	8		18		22		
t_{su}	Set up time, before CLK \uparrow	Data to CLK	2.0	60	30		80		100		ns
			4.5	15	10		18		20		
			6.0	14	8		16		18		
		$\overline{P}R$ or \overline{CLR} to CLK	2.0	5	0		5		5		ns
			4.5	5	0		5		5		
			6.0	5	0		5		5		
t_h	Hold time	CLK to Data	2.0	3	0		3		3		ns
			4.5	3	0		3		3		
			6.0	3	0		3		3		

AC Characteristics for HC: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER		V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HC173		GD54HC173		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
f_{max}	Maximum Clock Pulse Frequency		2.0	6	20		5		4		MHz
			4.5	30	65		25		20		
			6.0	35	75		30		25		
$t_{PLH} /$ t_{PHL}	Propagation Delay time CLK to nQ		2.0		65	170		220		300	ns
			4.5		17	34		42		55	
			6.0		16	32		38		50	
$t_{PLH} /$ t_{PHL}	Propagation Delay time \overline{CLR} to nQ		2.0		55	160		210		260	ns
			4.5		16	32		40		50	
			6.0		15	26		32		38	
$t_{PZH} /$ t_{PZL}	3-state Output Enable Time n \overline{OE} to nQ		2.0		50	150		190		230	ns
			4.5		16	30		38		45	
			6.0		15	26		32		38	
$t_{PHZ} /$ t_{PLZ}	3-state Output Disable Time n \overline{OE} to nQ		2.0		50	150		190		220	ns
			4.5		16	30		38		45	
			6.8		15	26		32		38	
$t_{TLH} /$ t_{2THL}	Output Transition time		2.0		15	60		75		90	ns
			4.5		6	12		15		22	
			6.0		6	13		13		12	

Timing Requirements for HCT: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER		V_{CC}	$T_A=25^\circ\text{C}$			GD74HCT173		GD54HCT173		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_w	Pulse width	$\overline{\text{CLR}}$	4.5	18	10		20		25		ns
		CLK	4.5	10	10		20		25		ns
t_{su}	Setup time	Data to CLK	4.5	15	10		18		20		ns
t_{rec}	Recovery time	$\overline{\text{PR}}$ or $\overline{\text{CLR}}$ to CLK	4.5	5	0		5		5		ns
t_h	Hold time	CLK to Data	4.5	3	0		3		3		ns

AC Characteristics for HCT: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER	V_{CC}	$T_A=25^\circ\text{C}$			GD74HCT173		GD54HCT173		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
f_{max}	Maximum Clock Pulse Frequency	4.5	27	54		22		18		MHz
t_{PLH} / t_{PHL}	Propagation Delay time CLK to nQ	4.5		18	36		44		56	ns
t_{PLH} / t_{PHL}	Propagation Delay time $\overline{\text{CLR}}$ to nQ	4.5		17	34		42		52	ns
t_{PZH} / t_{PZL}	3-state Output Enable Time nOE to nQ	4.5		17	32		40		40	ns
t_{PHZ} / t_{PLZ}	3-state Output Disable Time nOE to nQ	4.5		17	32		40		40	ns
t_{TLH} / t_{THL}	Output Transition time	4.5		7	12		15		18	ns

AC Waveforms

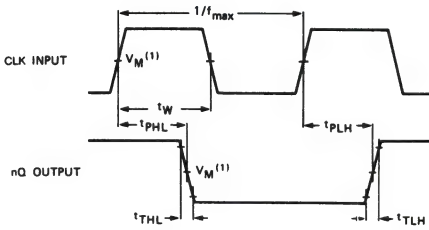


Fig. 2 Waveforms showing the clock (CLK) to output (nQ) propagation delays, the clock pulse width, the output transition times and the maximum clock pulse frequency.

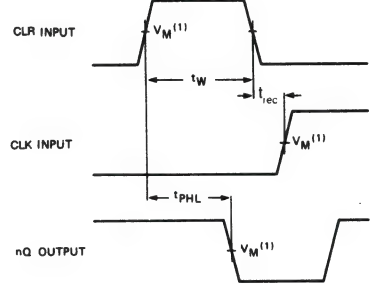


Fig. 3 Waveforms showing the master clear (CLR) pulse width, the master clear to output (nQ) propagation delays and the master clear to clock (CLK) recovery time.

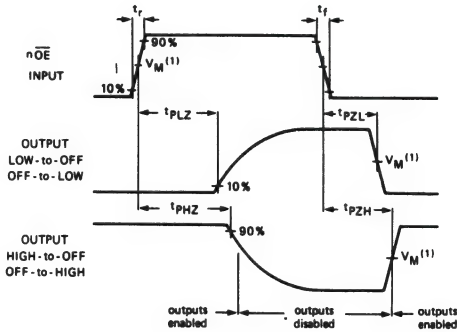


Fig. 4 Waveforms showing the 3-state enable and disable times.

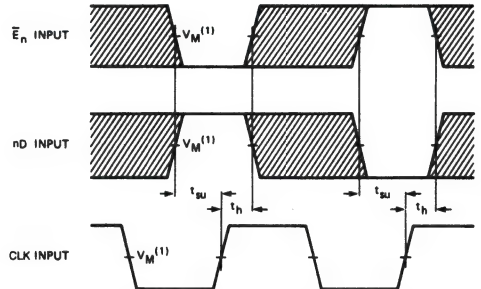


Fig. 5 Waveforms showing the data set-up and hold times from input (nG, nD) to clock (CLK).

Note to Fig. 5

The shaded areas indicate when the input is permitted to change for predictable output performance

Note to AC waveforms

(1) HC $V_M = 50\%$; $V_I = \text{GND to } V_{CC}$
HCT: $V_M = 1.3V$; $V_I = \text{GND to } 3V$.

GD54/74HC174, GD54/74HCT174

HEX D-TYPE FLIP-FLOPS WITH COMMON CLOCK & CLEAR

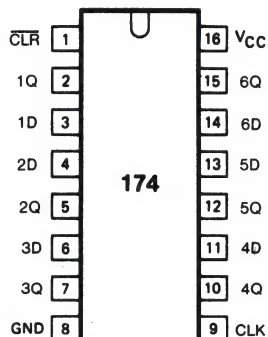
General Description

These devices are identical in pinout to the 54/74LS174. They contain six D-type flip-flops with common clock and clear inputs. Data on the D inputs having the specified setup and hold times are transferred to the outputs on the rising edge of the clock pulse. Clear is asynchronous and active-low. The clear input when low, sets all outputs to a low state. These devices are characterized for operation over wide temperature ranges to meet industry and military specifications.

Features

- Low Power consumption characteristic of CMOS devices
- Output drive capability: 10 LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts
for HCT 4.5 to 5.5 volts
- Low input current: 1 μ A Max.
- Low quiescent current: 80 μ A Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs

Pin Configuration



Suffix-Blank : Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package
Suffix-D : Small Outline Package

Function Table

OPERATING MODES	INPUTS			OUTPUTS
	$\overline{\text{CLR}}$	CLK	nD	nQ
clear	L	X	X	L
load "1"	H	\uparrow	h	H
load "0"	H	\uparrow	l	L

H = HIGH voltage level

h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CLK transition

L = LOW voltage level

l = LOW voltage level one set-up time prior to the LOW-to-HIGH CLK transition

X = don't care

\uparrow = LOW-to-HIGH CLK transition

Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC Supply voltage		-0.5	+7	V
I_{IK}, I_{OK}	DC input or output diode current	for $V_I < -0.5$ or $V_I > V_{CC} + 0.5V$		20	mA
I_O	DC output source or sink current	for $-0.5V < V_O < V_{CC} + 0.5V$		25	mA
I_{CC}	DC V_{CC} or GND current			50	mA
T_{stg}	Storage temperature range		-65	150	°C
P_D	Power dissipation per package	above +70°C: derate linearly with 8mW/K		500	mW
T_L	Lead temperature	At distance $1/16 \pm 1/32$ in. from case for 60 sec(CERAMIC) 10 sec(PLASTIC)		300 260	°C

Recommended Operating Conditions

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range V_{CC} : GD54/74HC Types GD54/74HCT Types	2 4.5	6 5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A : GD74 Types GD54 Types	-40 -55	+85 +125	°C
Input Rise and Fall times t_r, t_f : GD54/74HC Types at 2V at 4.5V at 6V GD54/74HCT Types at 4.5 V		1000 500 400 500	ns

Logic Diagram

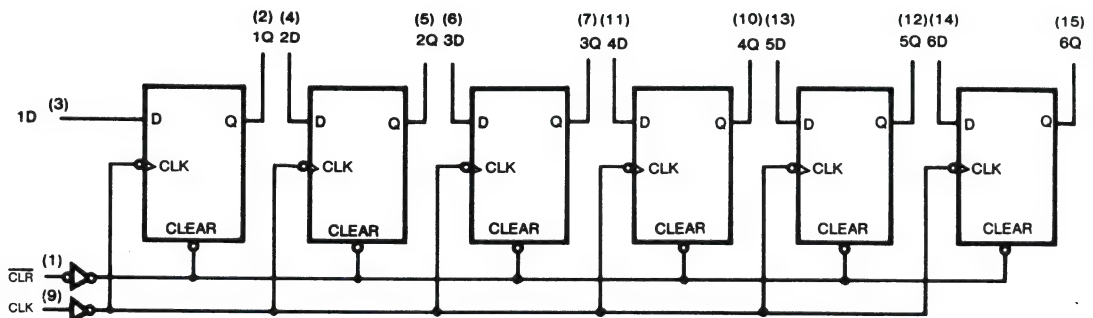


Fig. 1 Logic diagram

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HC174		GD54HC174		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2		1.5 3.15 4.2		V
V _{IL}	LOW level input voltage		2.0 4.5 6.0			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH}	I _{OH} =-20μA	2.0	1.9	2.0	1.9		1.9		V
				4.5	4.4	4.5	4.4		4.4		
		or V _{IL}	I _{OH} =-4mA I _{OH} =-5.2mA	6.0	5.9	6.0	5.9		5.9		
				4.5	3.98	4.3	3.84		3.7		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH}	I _{OL} =20μA	2.0			0.1		0.1		V
				4.5			0.1		0.1		
		or V _{IL}	I _{OL} =4mA I _{OL} =5.2mA	6.0			0.1		0.1		
				4.5		0.17	0.26		0.33		
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	6.0			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	6.0			8		80		160	μA

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HCT174		GD54HCT174		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		4.5 to 5.5	2.0			2.0		2.0		V
V _{IL}	LOW level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH}	I _{OH} =-20μA	4.5	4.4	4.5	4.4		4.4		V
		or V _{IL}	I _{OH} =-4mA	4.5	3.98	4.3	3.84		3.7		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH}	I _{OL} =20μA	4.5			0.1		0.1		V
		or V _{IL}	I _{OL} =4mA	4.5		0.17	0.26		0.33		
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	5.5			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	5.5			8		80		160	μA

Timing Requirements for HC: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER		V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HC174		GD54HC174		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_w	Pulse width	$\overline{\text{CLR}}$	2.0	80	30		100		120		ns
			4.5	16	10		20		25		
			6.0	14	8		18		22		
		CLK	2.0	80	30		100		120		ns
			4.5	16	10		20		25		
			6.0	14	8		18		22		
t_{su}	Setup time	Data to CLK	2.0	60	30		80		100		ns
			4.5	15	10		18		22		
			6.0	14	8		16		18		
t_{rec}	Recovery time	$\overline{\text{PR}}$ or $\overline{\text{CLR}}$ to CLK	2.0	5	0		5		5		ns
			4.5	5	0		5		5		
			6.0	5	0		5		5		
t_h	Hold time	CLK to Data	2.0	3	0		3		3		ns
			4.5	3	0		3		3		
			6.0	3	0		3		3		

AC Characteristics for HC: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER		V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HC174		GD54HC174		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
f_{max}	Maximum Clock Pulse Frequency		2.0	6	20		5		4		MHz
			4.5	30	65		25		20		
			6.0	35	75		30		25		
$t_{PLH}/$ t_{PHL}	Propagation Delay Time CLK to nQ,		2.0		46	160		200		250	ns
			4.5		15	30		40		50	
			6.0		14	28		35		45	
$t_{PLH}/$ t_{PHL}	Propagation Delay Time $\overline{\text{CLR}}$ to nQ,		2.0		45	155		190		230	ns
			4.5		15	28		38		45	
			6.0		14	26		34		40	
$t_{TLH}/$ t_{THL}	Output Transition Time		2.0		25	70		85		100	ns
			4.5		8	15		18		22	
			6.0		7	13		16		19	

Timing Requirements for HCT: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER		V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HCT174		GD54HCT174		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_w	Pulse width	$\overline{\text{CLR}}$	4.5	18	10		20		25		ns
		CLK	4.5	10	10		20		25		ns
t_{su}	Setup time	Data to CLK	4.5	15	10		18		20		ns
t_{rec}	Recovery time	$\overline{\text{PR}}$ or $\overline{\text{CLR}}$ to CLK	4.5	5	0		5		5		ns
t_h	Hold time	CLK to Data	4.5	3	0		3		3		ns

AC Characteristics for HCT: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HCT174		GD54HCT174		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
f_{max}	Maximum Clock Pulse Frequency	4.5	27	54		22		18		MHz
t_{PLH} / t_{PHL}	Propagation Delay time CLK to nQ	4.5		16	30		40		50	ns
t_{PLH} / t_{PHL}	Propagation Delay time $\overline{\text{CLR}}$ to nQ	4.5		16	30		40		50	ns
t_{TLH} / t_{THL}	Output Transition time	4.5		8	15		18		22	ns

AC Waveforms

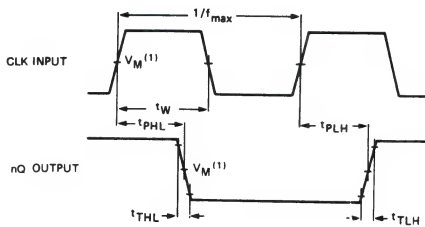


Fig. 2 Waveforms showing the clock (CLK) to output (nQ) propagation delays, the clock pulse width, the output transition times and the maximum clock pulse frequency.

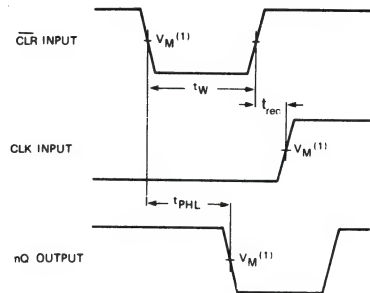


Fig. 3 Waveforms showing the master clear (CLR) pulse width, the master clear to output (nQ) propagation delays and the master clear to clock (CLK) recovery time.

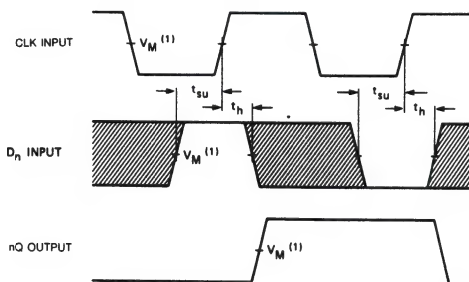


Fig. 4 Waveforms showing the data set-up and hold times for the data input (nD).

Note to Fig. 4

The shaded areas indicate when the input is permitted to change for predictable output performance.

Note to AC waveforms

- (1) HC : $V_M = 50\%$; $V_I = \text{GND to } V_{CC}$.
HCT : $V_M = 1.3V$; $V_I = \text{GND to } 3V$.

GD54/74HC175, GD54/74HCT175

QUAD D-TYPE FLIP-FLOPS WITH COMMON CLOCK & CLEAR

General Description

These devices are identical in pinout to the 54/74LS175. They contain four D-type flip-flops with common clock and clear inputs, and separate data inputs. Information at a data input is transferred to the Q and \bar{Q} outputs on the rising edge of the clock pulse. Both true and complementary outputs from each flip-flop are externally available. clear is asynchronous and active-low. These devices are characterized for operation over wide temperature ranges to meet industry and military specifications.

Features

- Low Power consumption characteristic of CMOS devices
- Output drive capability: 10 LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts
for HCT 4.5 to 5.5 volts
- Low input current: 1 μ A Max.
- Low quiescent current: 80 μ A Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs

Function Table

OPERATING MODES	INPUTS			OUTPUTS	
	\bar{CLR}	CLK	nD	nQ	\bar{nQ}
clear	L	X	X	L	H
load "1"	H	\uparrow	h	H	L
load "0"	H	\uparrow	l	L	H

H = HIGH voltage level

h = HIGH voltage level one set-up time prior to the
LOW-to-HIGH CLK transition

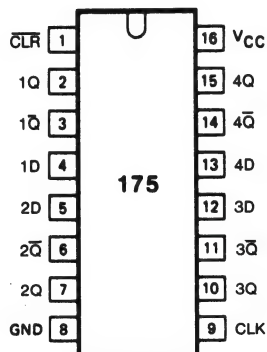
L = LOW voltage level

l = LOW voltage level on set-up time prior to the
LOW-to-HIGH CLK transition

\uparrow = LOW-to-HIGH CLK transition

X = don't care

Pin Configuration



Suffix-Blank : Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package
Suffix-D : Small Outline Package

Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC Supply voltage		-0.5	+7	V
I_{IK}, I_{OK}	DC input or output diode current	for $V_I < -0.5$ or $V_I > V_{CC} + 0.5V$		20	mA
I_O	DC output source or sink current	for $-0.5V < V_O < V_{CC} + 0.5V$		25	mA
I_{CC}	DC V_{CC} or GND current			50	mA
T_{stg}	Storage temperature range		-65	150	°C
P_D	Power dissipation per package	above +70°C: derate linearly with 8mW/K		500	mW
T_L	Lead temperature	At distance 1/16 ± 1/32 in. from case for 60 sec(CERAMIC) 10 sec(PLASTIC)		300 260	°C

Recommended Operating Conditions

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range V_{CC} : GD54/74HC Types GD54/74HCT Types	2 4.5	6 5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A : GD74 Types GD54 Types	-40 -55	+85 +125	°C
Input Rise and Fall times t_r, t_f : GD54/74HC Types at 2V at 4.5V at 6V GD54/74HCT Types at 4.5 V		1000 500 400 500	ns

Logic Diagram

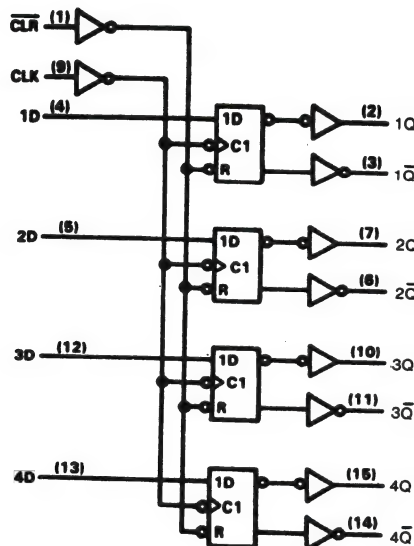


Fig. 1 Logic diagram

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HC175		GD54HC175		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2		1.5 3.15 4.2		V
V _{IL}	LOW level input voltage		2.0 4.5 6.0			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH}	I _{OH} =-20μA	2.0	1.9	2.0			1.9		V
				4.5	4.4	4.5			4.4		
		or V _{IL}	I _{OH} =-4mA I _{OH} =-5.2mA	6.0	5.9	6.0			5.9		
				4.5	3.98	4.3			3.7		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH}	I _{OL} =20μA	2.0			0.1	0.1		0.1	V
				4.5			0.1	0.1		0.1	
		or V _{IL}	I _{OL} =4mA I _{OL} =5.2mA	6.0							
				4.5		0.17	0.26	0.33		0.4	
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	6.0			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	6.0			8		80		160	μA

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HCT175		GD54HCT175		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		4.5 to 5.5	2.0			2.0		2.0		V
V _{IL}	LOW level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH}	I _{OH} =-20μA	4.5	4.4	4.5		4.4		4.4	V
		or V _{IL}	I _{OH} =-4mA	4.5	3.98	4.3		3.84		3.7	
V _{OL}	LOW level output voltage	V _{IN} =V _{IH}	I _{OL} =20μA	4.5			0.1	0.1		0.1	V
		or V _{IL}	I _{OL} =4mA	4.5		0.17	0.26	0.33		0.4	
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	5.5			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	5.5			8		80		160	μA

Timing Requirements for HC: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER		V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HC175		GD54HC175		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_w	Pulse width	$\overline{\text{CLR}}$ low	2.0	80	30		100		120		ns
			4.5	16	10		20		25		
			6.0	14	8		18		22		
		CLK high or low	2.0	80	30		100		120		ns
			4.5	16	10		20		25		
			6.0	14	8		18		22		
t_{su}	Setup time	nD to CLK	2.0	60	30		80		100		ns
			4.5	15	10		18		22		
			6.0	14	8		16		18		
t_{rec}	Recovery time	$\overline{\text{CLR}}$ to CLK	2.0	5	0		5		5		ns
			4.5	5	0		5		5		
			6.0	5	0		5		5		
t_h	Hold time	CLK to nD	2.0	3	0		3		3		ns
			4.5	3	0		3		3		
			6.0	3	0		3		3		

AC Characteristics for HC: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HC175		GD54HC175		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
f_{max}	Maximum Clock Pulse Frequency	2.0	6	20		5		4		Mhz
		4.5	30	65		25		20		
		6.0	35	75		30		25		
$t_{PLH}/$ t_{PHL}	Propagation Delay Time CLK to nQ, $n\overline{Q}$	2.0		50	160		200		240	ns
		4.5		17	30		40		50	
		6.0		16	28		35		45	
$t_{PLH}/$ t_{PHL}	Propagation Delay Time $\overline{\text{CLR}}$ to nQ, $n\overline{Q}$	2.0		46	160		200		240	ns
		4.5		16	30		40		50	
		6.0		15	28		35		45	
$t_{TLH}/$ t_{THL}	Output Transition Time	2.0		25	7		85		100	ns
		4.5		8	15		18		22	
		6.0		7	13		16		19	

Timing Requirements for HCT: $t_r = t_f = 6\text{ns}$ $C_L = 50\text{ pF}$

SYMBOL	PARAMETER		V_{CC} (V)	$T_A = 25^\circ\text{C}$			GD74HCT175		GD54HCT175		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_w	Pulse width	$\overline{\text{CLR}}$ low	4.5	18	10		20		25		ns
		CLK high or low	4.5	16	10		20		25		ns
t_{su}	Setup time	$\sim nD$ to CLK	4.5	15	10		18		22		ns
t_{rec}	Recovery time	$\overline{\text{CLR}}$ to CLK	4.5	5	0		5		5		ns
t_h	Hold time	CLK to nD	4.5	3	0		3		3		ns

AC Characteristics for HCT: $t_r = t_f = 6\text{ns}$ $C_L = 50\text{ pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A = 25^\circ\text{C}$			GD74HCT175		GD54HCT175		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
f_{max}	Maximum Clock Pulse Frequency	4.5	27	54		22		18		MHz
$t_{PLH}/$ t_{PHL}	Propagation Delay Time CLK to nQ , $n\overline{Q}$	4.5		18	31		42		54	ns
$t_{PLH}/$ t_{PHL}	Propagation Delay Time $\overline{\text{CLR}}$ to nQ , $n\overline{Q}$	4.5		17	30		40		50	ns
$t_{TLH}/$ t_{THL}	Output Transition Time	4.5		8	15		18		22	ns

AC Waveforms

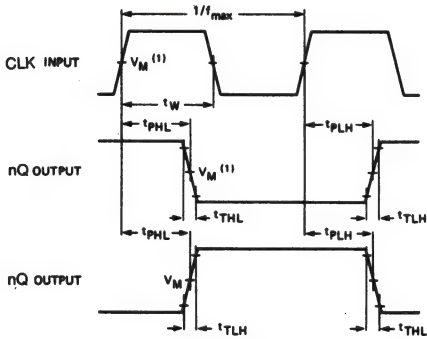


Fig. 2 Waveforms showing the clock (CLK) to outputs (nQ, nQ̄) propagation delays, the clock pulse width, output transition times and the maximum clock pulse frequency.

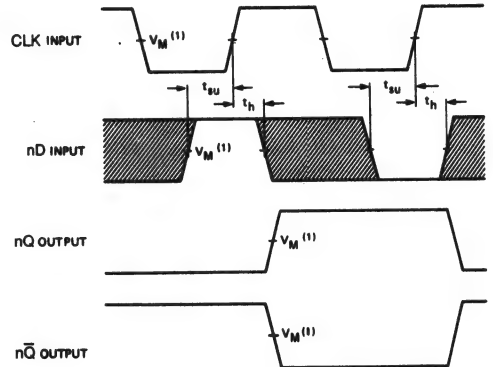


Fig. 3 Waveforms showing the data set-up and hold times for the data input (nD).

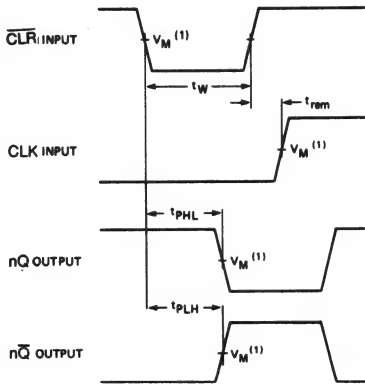


Fig. 4 Waveforms showing the master clear (CLR) pulse width, the master clear to outputs (nQ, nQ̄) propagation delays and the master clear to clock (CLK) recovery time.

Note to Fig. 3

The shaded areas indicate when the input is permitted to change for predictable output performance.

Note to AC waveforms

- (1) HC : $V_M = 50\%$; $V_I = \text{GND to } V_{CC}$.
- HCT : $V_M = 1.3V$; $V_I = \text{GND to } 3V$.

GD54/74HC190, GD54/74HCT190

SYNCHRONOUS DECADE UP/DOWN COUNTER WITH MODE CONTROL

General Description

These devices are identical in pinout to the 54/74LS190. This synchronous, reversible, up/down BCD counter can be preset by applying the desired value in BCD to the preset inputs and then bringing the load input low. Counting is achieved on the rising edge of the clock when the load input is high, the count enable is low, and the count up/down is either low (Up counting) or high (Down counting). Two outputs have been made available to perform the cascading function: ripple clock and carry out. The ripple clock produces a low level output pulse when the counter overflows or underflows. Ripple clock can be used for cascading and carry out can be used for look-aheading.

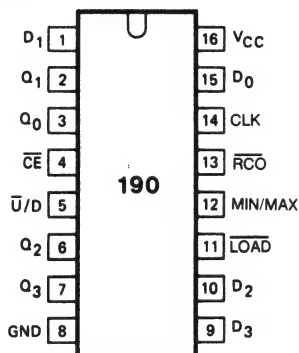
Features

- Low Power consumption characteristic of CMOS devices
- Output drive capability: 10 LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts
for HCT 4.5 to 5.5 volts
- Low input current: $1\mu\text{A}$ Max.
- Low quiescent current: $80\mu\text{A}$ Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs

Function Table

OPERATING MODE	INPUTS					OUTPUTS
	LOAD	\bar{U}/D	\bar{CE}	CLR	D_n	Q_n
parallel load	L	X	X	X	L	L
	L	X	X	X	H	H
count up	H	L	I	\uparrow	X	count up
count down	H	H	I	\uparrow	X	count down
hold (do nothing)	H	X	H	X	X	no change

Pin Configuration



Suffix-Blank : Plastic Dual In Line Package
 Suffix-J : Ceramic Dual In Line Package
 Suffix-D : Small Outline Package

MIN/MAX and \bar{RCO} Function Table

INPUTS			TERMINAL COUNT STATE				OUTPUTS	
\bar{U}/D	\bar{CE}	CLK	Q_0	Q_1	Q_2	Q_3	MIN/MAX	\bar{RCO}
H	H	X	H	X	X	H	L	H
L	H	X	H	X	X	H	H	H
L	L	\downarrow	H	X	X	H	\downarrow	\downarrow
L	H	X	L	L	L	L	L	H
H	H	X	L	L	L	L	H	H
H	L	\downarrow	L	L	L	L	\downarrow	\downarrow

I = LOW voltage level one set-up time prior to the LOW-to-HIGH CLK transition

\downarrow = one LOW level pulse

\downarrow = MIN/MAX goes LOW on a LOW-to-HIGH CLK transition

Logic Diagram

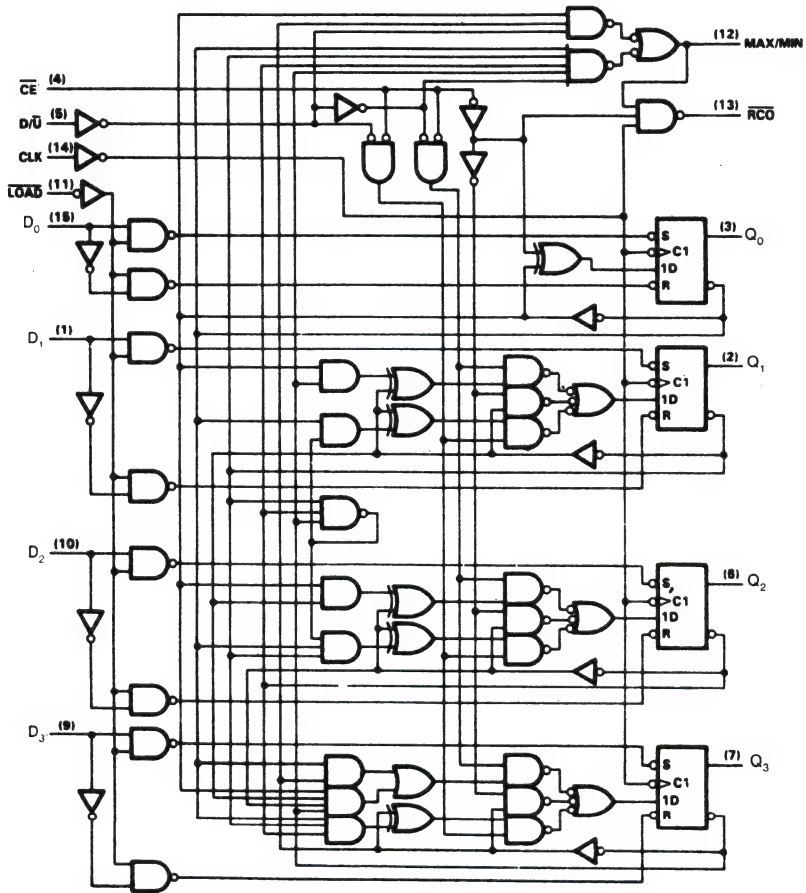


Fig. 1 Logic diagram

Typical Load, Count, and Inhibit Sequences

Illustrated below is the following sequence:

1. Load (preset) to BCD seven.
2. Count up to eight, nine (maximum), zero, one, and two.
3. Inhibit.
4. Count down to one, zero (minimum), nine, eight, and seven.

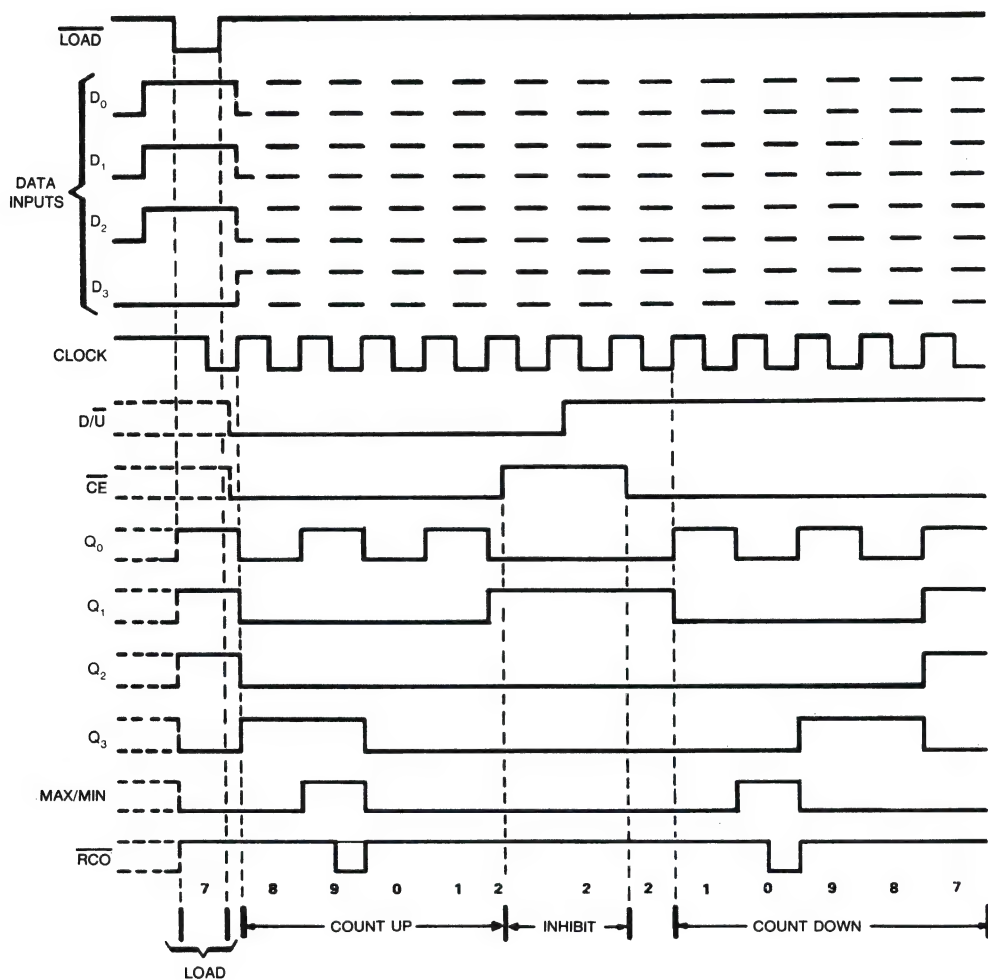


Fig. 2 Typical load, count, and inhibit sequences

Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC Supply voltage		-0.5	+7	V
$I_{IK} I_{OK}$	DC input or output diode current	for $V_I < -0.5$ or $V_I > V_{CC} + 0.5V$		20	mA
I_O	DC output source or sink current	for $-0.5V < V_O < V_{CC} + 0.5V$		25	mA
I_{CC}	DC V_{CC} or GND current			50	mA
T_{stg}	Storage temperature range		-65	150	°C
P_D	Power dissipation per package	above +70°C: derate linearly with 8mW/K		500	mW
T_L	Lead temperature	At distance 1/16±1/32 in. from case for 60 sec(CERAMIC) 10 sec(PLASTIC)		300 260	°C

Recommended Operating Conditions

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range V_{CC} : GD54/74HC Types GD54/74HCT Types	2 4.5	6 5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A : GD74 Types GD54 Types	-40 -55	+85 +125	°C
Input Rise and Fall times t_r, t_f : GD54/74HC Types at 2V at 4.5V at 6V GD54/74HCT Types at 4.5V		1000 500 400 500	ns

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HC 190		GD54HC 190		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2		1.5 3.15 4.2		V
V _{IL}	LOW level input voltage		2.0 4.5 6.0			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH}	I _{OH} =-20μA	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0	1.9 4.4 5.9		1.9 4.4 5.9		V
		or V _{IL}	I _{OH} =-4mA I _{OH} =-5.2mA	4.5 6.0	3.98 5.48	4.3 5.2	3.84 5.34		3.7 5.2		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH}	I _{OL} =20μA	2.0 4.5 6.0			0.1 0.1 0.1	0.1 0.1 0.1		0.1 0.1 0.1	V
		or V _{IL}	I _{OL} =4mA I _{OL} =5.2mA	4.5 6.0		0.17 0.15	0.26 0.26	0.33 0.33		0.4 0.4	
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	6.0			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	6.0			8		80		160	μA

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HCT190		GD54HCT190		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		4.5 to 5.5	2.0			2.0		2.0		V
V _{IL}	LOW level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH}	I _{OH} =-20μA	4.5	4.4	4.5	4.4		4.4		V
		or V _{IL}	I _{OH} =-4mA	4.5	3.98	4.3	3.84		3.7		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH}	I _{OL} =20μA	4.5			0.1	0.1		0.1	V
		or V _{IL}	I _{OL} =4mA	4.5		0.17	0.26	0.33		0.4	
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	5.5			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	5.5			8		80		160	μA

Timing Requirements for HC: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER		V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HC190		GD54HC190		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_w	Pulse width	CLK high or low	2.0	120	28		150		180		ns
			4.5	24	10		30		36		
			6.0	21	8		26		31		
		$\overline{\text{LOAD}}$ low	2.0	120	28		150		180		ns
			4.5	24	10		30		36		
			6.0	21	8		26		31		
t_{su}	Setup time	D_n to $\overline{\text{LOAD}}$	2.0	100	19		125		150		ns
			4.5	20	7		25		30		
			6.0	17	6		21		26		
		$\overline{\text{CE}}$ to CLK	2.0	140	39		175		210		ns
			4.5	28	14		35		42		
			6.0	24	11		30		36		
		$\overline{\text{U/D}}$ to CLK	2.0	205	61		255		310		ns
			4.5	41	22		51		60		
			6.0	35	18		43		53		
t_{rec}	Recovery time	$\overline{\text{LOAD}}$ to CLK	2.0	5			5		5		ns
			4.5	5			5		5		
			6.0	5			5		5		
t_h	Hold time	$D_n, \overline{\text{CE}}, \overline{\text{U/D}}$ to CLK	2.0	5			5		5		ns
			4.5	5			5		5		
			6.0	5			5		5		

AC Characteristics for HC: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HC190		GD54HC190		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
f_{max}	Maximum clock pulse frequency	2.0 4.5 6.0	3.0 15 18			2.4 12 14		2.0 10 12		MHz
$t_{\text{PLH}}/$ t_{PHL}	Propagation Delay Time $\overline{\text{LOAD}}$ to Q_n	2.0 4.5 6.0		60 20 16	220 44 37		275 55 47		330 66 50	ns
$t_{\text{PLH}}/$ t_{PHL}	Propagation Delay Time D_n to Q_n	2.0 4.5 6.0		60 20 16	220 44 37		275 55 47		330 66 50	ns
$t_{\text{PLH}}/$ t_{PHL}	Propagation Delay Time CLK to $\overline{\text{RCO}}$	2.0 4.5 6.0		42 15 12	150 30 26		190 38 33		225 45 38	ns
$t_{\text{PLH}}/$ t_{PHL}	Propagation Delay Time CLK to Q_n	2.0 4.5 6.0		62 21 17	220 44 37		275 55 47		330 62 56	ns
$t_{\text{PLH}}/$ t_{PHL}	Propagation Delay Time CLK to Max/Min	2.0 4.5 6.0		80 28 22	250 50 42		320 64 54		395 77 65	ns
$t_{\text{PLH}}/$ t_{PHL}	Propagation Delay Time $\overline{\text{U/D}}$ to $\overline{\text{RCO}}$	2.0 4.5 6.0		50 18 14	210 42 36		265 53 45		315 63 54	ns
$t_{\text{PLH}}/$ t_{PHL}	Propagation Delay Time $\overline{\text{U/D}}$ to Mix/Min	2.0 4.5 6.0		44 16 13	190 38 32		240 48 41		285 57 43	ns
$t_{\text{PLH}}/$ t_{PHL}	Propagation Delay Time $\overline{\text{CE}}$ to $\overline{\text{RCO}}$	2.0 4.5 6.0		35 13 11	130 26 22		165 33 28		195 39 33	ns
$t_{\text{TLH}}/$ t_{THL}	Output Transition Time	2.0 4.5 6.0		19 7 6	75 15 13		95 19 16		110 22 19	ns

Timing Requirements for HCT: $t_r = t_f = 6\text{ns}$ $C_L = 50\text{ pF}$

SYMBOL	PARAMETER		V_{CC} (V)	$T_A = 25^\circ\text{C}$			GD74HCT190		GD54HCT190		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_w	Pulse width	CLK high or low	4.5	31	10		39		47		ns
		$\overline{\text{LOAD}}$ low	4.5	22	12		28		33		ns
t_{su}	Setup time	D_n to $\overline{\text{LOAD}}$	4.5	20	10		25		30		ns
		$\overline{\text{CE}}$ to CLK	4.5	31	18		39		47		ns
		$\overline{\text{U/D}}$ to CLK	4.5	42	25		53		63		ns
t_{rec}	Recovery time	$\overline{\text{LOAD}}$ to CLK	4.5	5			5		5		ns
t_h	Hold time	D_n , $\overline{\text{CE}}$, $\overline{\text{U/D}}$ to CLK	4.5	5			5		5		ns

AC Characteristics for HCT: $t_r = t_f = 6\text{ns}$ $C_L = 50\text{ pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A = 25^\circ\text{C}$			GD74HCT190		GD54HCT190		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
f_{max}	Maximum clock pulse frequency	4.5	16	27		13		11		Mhz
$t_{\text{PLH}}/$ t_{PHL}	Propagation Delay Time $\overline{\text{LOAD}}$ to Q_n	4.5		26	49		61		74	ns
$t_{\text{PLH}}/$ t_{PHL}	Propagation Delay Time D_n to Q_n	4.5		24	49		55		66	ns
$t_{\text{PLH}}/$ t_{PHL}	Propagation Delay Time CLK to $\overline{\text{RCO}}$	4.5		20	35		44		53	ns
$t_{\text{PLH}}/$ t_{PHL}	Propagation Delay Time CLK to Q_n	4.5		25	48		60		72	ns
$t_{\text{PLH}}/$ t_{PHL}	Propagation Delay Time CLK to Max/Min	4.5		32	56		72		85	ns
$t_{\text{PLH}}/$ t_{PHL}	Propagation Delay Time $\overline{\text{U/D}}$ to $\overline{\text{RCO}}$	4.5		24	45		56		68	ns
$t_{\text{PLH}}/$ t_{PHL}	Propagation Delay Time $\overline{\text{U/D}}$ to Mix/Min	4.5		24	45		56		68	ns
$t_{\text{PLH}}/$ t_{PHL}	Propagation Delay Time $\overline{\text{CE}}$ to $\overline{\text{RCO}}$	4.5		20	40		58		65	ns
$t_{\text{TLH}}/$ t_{THL}	Output Transition Time	4.5		7	15		19		22	ns

AC Waveforms

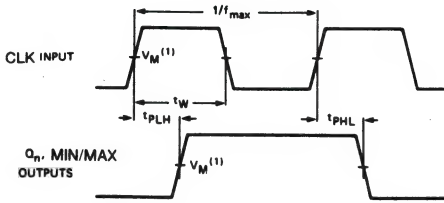


Fig. 3 Waveforms showing the clock (CLK) to output (Q_n) propagation delays, the clock pulse width and the maximum clock pulse frequency.

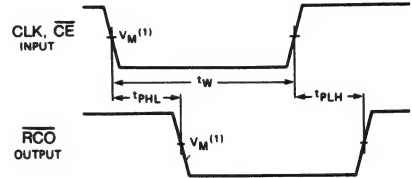


Fig. 4 Waveforms showing the clock and count enable inputs (CLK, \overline{CE}) to ripple clock output (\overline{RCO}) propagation delays and the \overline{CE} pulse width.

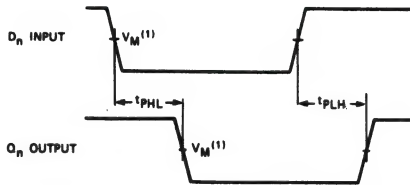


Fig. 5 Waveforms showing the input (D_n) to output (Q_n) propagation delays.

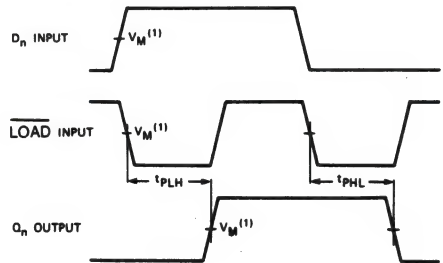


Fig. 6 Waveforms showing the input (\overline{LOAD}) to output (Q_n) propagation delays.

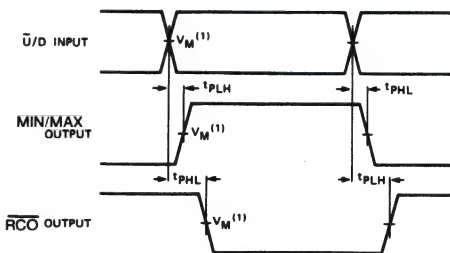


Fig. 7 Waveforms showing the up/down count input ($\overline{U/D}$) to terminal count and ripple clock output (Min/MAX, \overline{RCO}) propagation delays.

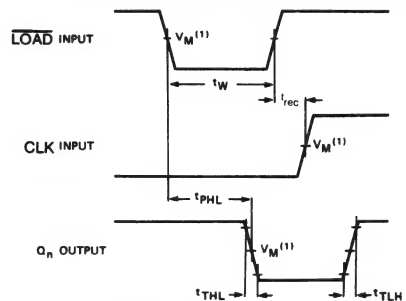


Fig. 8 Waveforms showing the parallel load input (\overline{LOAD}) pulsewidth, recovery time to clock (CLK) and the output (Q_n) transition times.

AC Waveforms (Continued)

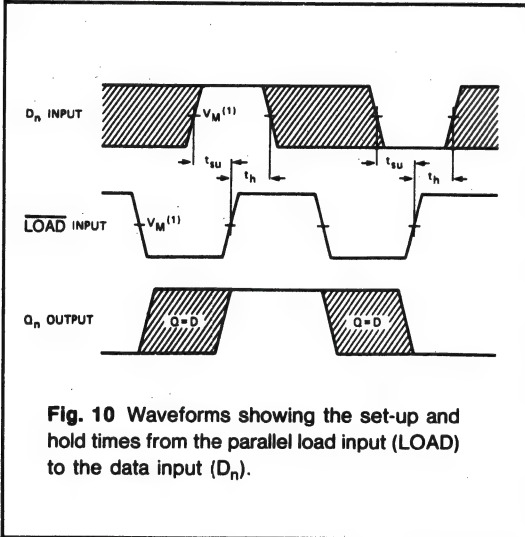


Fig. 10 Waveforms showing the set-up and hold times from the parallel load input (LOAD) to the data input (D_n).

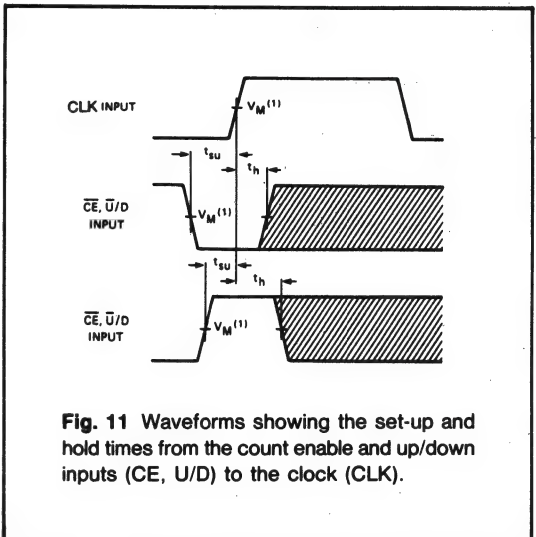


Fig. 11 Waveforms showing the set-up and hold times from the count enable and up/down inputs (\overline{CE} , $\overline{U/D}$) to the clock (CLK).

Note to AC waveforms

- (1) HC : $V_M = 50\%$; $V_I = \text{GND to } V_{CC}$.
HCT : $V_M = 1.3V$; $V_I = \text{GND to } 3V$.

Note to Figs 10, 11

The shaded areas indicate when the input is permitted to change for predictable output performance.

GD54/74HC191, GD54/74HCT191

SYNCHRONOUS 4-BIT BINARY UP-DOWN COUNTER WITH MODE CONTROL

General Description

These devices are identical in pinout to the 54/74LS191. This synchronous, reversible, 4-Bit binary up/down counter can be preset by applying the desired value in 4-bit binary to the preset inputs and then bringing the load input low. Counting is achieved on the rising edge of the clock when the load input is high, the count enable is low, and the count up/down is either low (up counting) or high (down counting). Two outputs have been made available to preform the cascading function: ripple clock and carry out. The ripple clock produces a low level output pulse and carry out produces a high level output pulse when the counter overflows or underflows. Ripple clock can be used for cascading and carry out can be used for look-ahead.

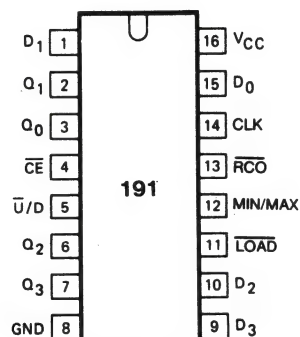
Features

- Low Power consumption characteristic of CMOS devices
- Output drive capability: 10LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts
for HCT 4.5 to 5.5 volts
- Low input current: 1 μ A Max.
- Low quiescent current: 80 μ A Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs

Function Table

OPERATING MODE	INPUTS					OUTPUTS
	LOAD	U/D	CE	CLK	D _n	
parallel load	L	X	X	X	L	L
	L	X	X	X	H	H
count up	H	L	I	↑	X	count up
count down	H	H	I	↑	X	count down
hold (do nothing)	H	X	H	X	X	no change

Pin Configuration



Suffix-Blank : Plastic Dual In Line Package
 Suffix-J : Ceramic Dual In Line Package
 Suffix-D : Small Outline Package

MIN/MAX and RCO Function Table

INPUTS			TERMINAL COUNT STATE				OUTPUTS	
U/D	CE	CLK	Q ₀	Q ₁	Q ₂	Q ₃	MIN/MAX	RCO
H	H	X	H	X	X	H	L	H
L	H	X	H	X	X	H	H	H
L	L	⌋	H	X	X	H	⌋	⌋
L	H	X	L	L	L	L	L	H
H	H	X	L	L	L	L	H	H
H	L	⌋	L	L	L	L	⌋	⌋

I = LOW voltage level one set-up time prior to the LOW-to-HIGH CLK transition

⌋ = one LOW level pulse

⌋ = MIN/MAX goes LOW on a LOW-to-HIGH CLK transition

Logic Diagram

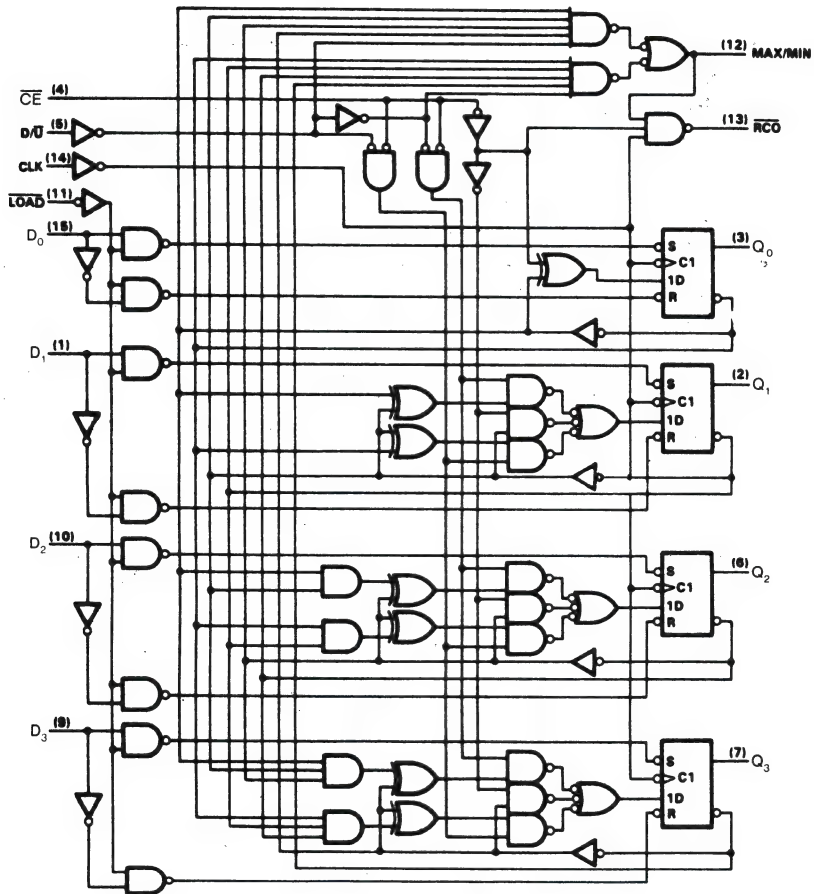


Fig. 1 Logic diagram

Typical Load, Count and Inhibit Sequences

Illustrated below is the following sequence:

1. Load (preset) to binary thirteen.
2. Count up to fourteen, fifteen (maximum), zero, one, and two.
3. Inhibit.
4. Count down to one, zero (minimum), fifteen, fourteen, and thirteen.

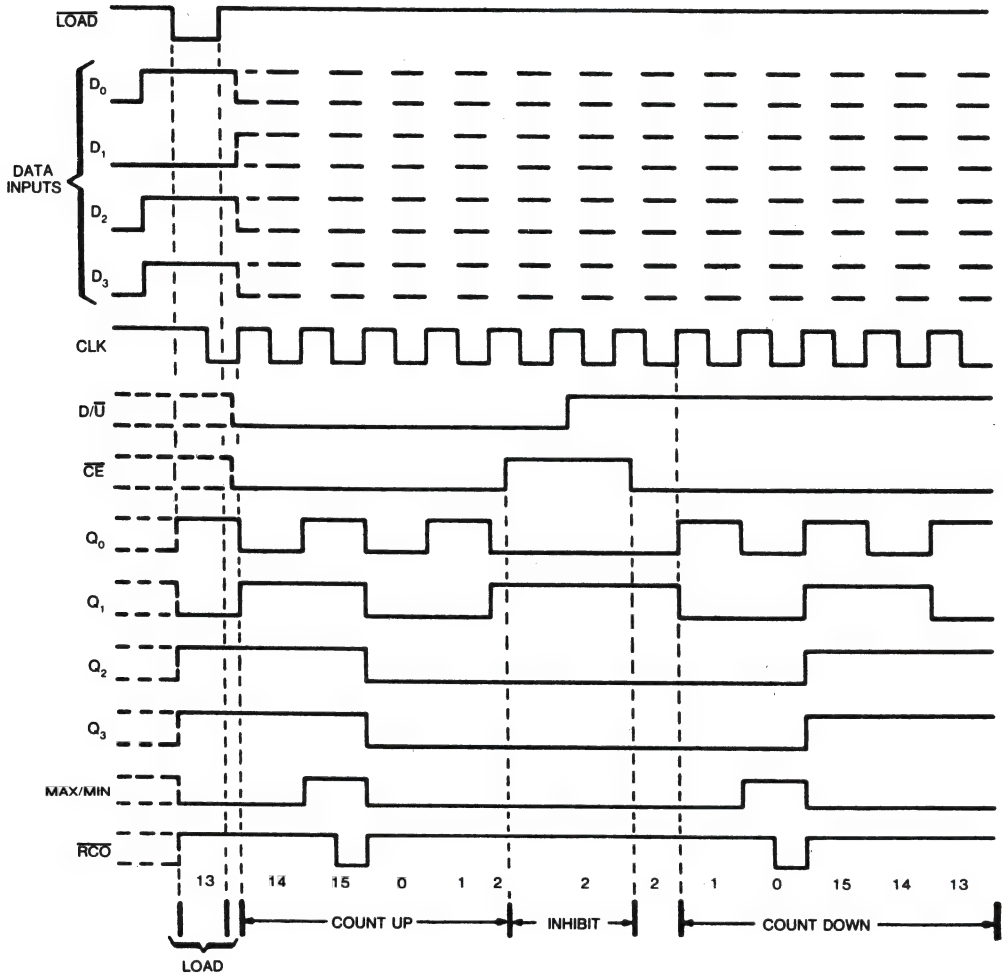


Fig. 2 Typical Load, count, and Inhibit Sequences

Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC Supply voltage		-0.5	+7	V
I_{IK}, I_{OK}	DC input or output diode current	for $V_I < -0.5$ or $V_I > V_{CC} + 0.5V$		20	mA
I_O	DC output source or sink current	for $-0.5V < V_O < V_{CC} + 0.5V$		25	mA
I_{CC}	DC V_{CC} or GND current			50	mA
T_{stg}	Storage temperature range		-65	150	°C
P_D	Power dissipation per package	above +70°C: derate linearly with 8mW/K		500	mW
T_L	Lead temperature	At distance 1/16 ± 1/32 in. from case for 60 sec(CERAMIC) 10 sec(PLASTIC)		300 260	°C

Recommended Operating Conditions

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range V_{CC} : GD54/74HC Types	2	6	V
GD54/74HCT Types	4.5	5.5	
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A : GD74 Types	-40	+85	°C
GD54 Types	-55	+125	
Input Rise and Fall times t_r, t_f : GD54/74HC Types at 2V		1000	ns
at 4.5V		500	
at 6V		400	
GD54/74HCT Types at 4.5V		500	

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HC191		GD54HC191		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2		1.5 3.15 4.2		V
V _{IL}	LOW level input voltage		2.0 4.5 6.0			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH} I _{OH} =-20μA	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V
		or V _{IL} I _{OH} =-4mA I _{OH} =-5.2mA	4.5 6.0	3.98 5.48	4.3 5.2		3.84 5.34		3.7 5.2		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH} I _{OL} =20μA	2.0 4.5 6.0			0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V
		or V _{IL} I _{OL} =4mA I _{OL} =5.2mA	4.5 6.0		0.17 0.15	0.26 0.26		0.33 0.33		0.4 0.4	
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	6.0			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	6.0			8		80		160	μA

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HCT191		GD54HCT191		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		4.5 to 5.5	2.0 ⁺			2.0		2.0		V
V _{IL}	LOW level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH} I _{OH} =-20μA	4.5	4.4	4.5		4.4		4.4		V
		or V _{IL} I _{OH} =-4mA	4.5	3.98	4.3		3.84		3.7		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH} I _{OL} =20μA	4.5			0.1		0.1		0.1	V
		or V _{IL} I _{OL} =4mA	4.5		0.17	0.26		0.33		0.4	
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	5.5			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	5.5			8		80		160	μA

Timing Requirements for HC: $t_r = t_f = 6\text{ns}$ $C_L = 50\text{ pF}$

SYMBOL	PARAMETER		V_{CC} (V)	$T_A = 25^\circ\text{C}$			GD74HC191		GD54HC191		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_w	Pulse width	CLK high or low	2.0	120	28		150		180		ns
			4.5	24	10		30		36		
			6.0	21	8		26		31		
		$\overline{\text{LOAD}}$ low	2.0	120	28		150		180		ns
			4.5	24	10		30		36		
			6.0	21	8		26		31		
t_{su}	Setup time	D_n to $\overline{\text{LOAD}}$	2.0	100	19		125		150		ns
			4.5	20	7		25		30		
			6.0	17	6		21		26		
		$\overline{\text{CE}}$ to CLK	2.0	140	39		175		210		ns
			4.5	28	14		35		42		
			6.0	24	11		30		36		
		$\overline{\text{U/D}}$ to CLK	2.0	205	61		255		310		ns
			4.5	41	22		51		60		
			6.0	35	18		48		53		
t_{rec}	Recovery time	$\overline{\text{LOAD}}$ to CLK	2.0	35	8		45		55		ns
			4.5	7	3		9		11		
			6.0	6	2		8		9		
t_h	Hold time	$D_n, \overline{\text{CE}}, \overline{\text{U/D}}$ to CLK	2.0	5			5		5		ns
			4.5	5			5		5		
			6.0	5			5		5		

AC Characteristics for HC: $t_r = t_f = 6\text{ns}$ $C_L = 50\text{ pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A = 25^\circ\text{C}$			GD74HC191		GD54HC191		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
f_{max}	Maximum Clock Pulse Frequency	2.0 4.5 6.0	3.0 15 18			2.4 12 14		2.0 10 12		MHz
$t_{\text{PLH}}/$ t_{PHL}	Propagation Delay Time $\overline{\text{LOAD}}$ to Q_n	2.0 4.5 6.0		60 20 16	220 44 37		275 55 47		330 66 50	ns
$t_{\text{PLH}}/$ t_{PHL}	Propagation Delay Time D_n to Q_n	2.0 4.5 6.0		60 20 16	220 44 37		275 55 47		330 66 50	ns
$t_{\text{PLH}}/$ t_{PHL}	Propagation Delay Time CLK to $\overline{\text{RCO}}$	2.0 4.5 6.0		42 15 12	150 30 26		190 38 33		225 45 38	ns
$t_{\text{PLH}}/$ t_{PHL}	Propagation Delay Time CLK to Q_n	2.0 4.5 6.0		62 21 17	220 44 37		275 55 47		330 62 56	ns
$t_{\text{PLH}}/$ t_{PHL}	Propagation Delay Time CLK to MIN/MAX	2.0 4.5 6.0		80 28 22	250 50 42		320 64 54		395 77 65	ns
$t_{\text{PLH}}/$ t_{PHL}	Propagation Delay Time D/\overline{U} to $\overline{\text{RCO}}$	2.0 4.5 6.0		50 18 14	210 42 36		265 53 45		315 63 54	ns
$t_{\text{PLH}}/$ t_{PHL}	Propagation Delay Time D/\overline{U} to MIN/MAX	2.0 4.5 6.0		44 16 13	190 38 32		240 48 41		285 57 48	ns
$t_{\text{PLH}}/$ t_{PHL}	Propagation Delay Time $\overline{\text{CE}}$ to $\overline{\text{RCO}}$	2.0 4.5 6.0		35 13 11	130 26 22		165 33 28		195 39 33	ns
$t_{\text{TLH}}/$ t_{THL}	Output Transition Time	2.0 4.5 6.0		19 7 6	75 15 13		95 19 16		110 22 19	ns

Timing Requirements for HCT: $t_r = t_f = 6\text{ns}$ $C_L = 50\text{ pF}$

SYMBOL	PARAMETER		V_{CC} (V)	$T_A = 25^\circ\text{C}$			GD74HCT191		GD54HCT191		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_w	Pulse width	CLK high or low	4.5	31	10		39		47		ns
		$\overline{\text{LOAD}}$ low	4.5	22	12		28		33		ns
t_{su}	Setup time	D_n to $\overline{\text{LOAD}}$	4.5	20	10		25		30		ns
		$\overline{\text{CE}}$ to CLK	4.5	31	18		39		47		ns
		$\overline{U/D}$ to CLK	4.5	42	25		53		63		ns
t_{rec}	Recovery time	$\overline{\text{LOAD}}$ to CLK	4.5	7	4		9		11		ns
t_h	Hold time	D_n , $\overline{\text{CE}}$, $\overline{U/D}$ to CLK	4.5	5			5		5		ns

AC Characteristics for HCT: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HCT191		GD54HCT191		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
f_{max}	Maximum Clock Pulse Frequency	4.5	16	27		13		11		MHz
$t_{\text{PLH}}/$ t_{PHL}	Propagation Delay Time $\overline{\text{LOAD}}$ to Qn	4.5		26	49		61		74	ns
$t_{\text{PLH}}/$ t_{PHL}	Propagation Delay Time Dn to Qn	4.5		24	49		55		66	ns
$t_{\text{PLH}}/$ t_{PHL}	Propagation Delay Time CLK to $\overline{\text{RCO}}$	4.5		20	35		44		53	ns
$t_{\text{PLH}}/$ t_{PHL}	Propagation Delay Time CLK to Qn	4.5		25	48		60		72	ns
$t_{\text{PLH}}/$ t_{PHL}	Propagation Delay Time CLK to MIN/MAX	4.5		32	56		72		85	ns
$t_{\text{PLH}}/$ t_{PHL}	Propagation Delay Time D/ $\overline{\text{U}}$ to $\overline{\text{RCO}}$	4.5		24	45		56		68	ns
$t_{\text{PLH}}/$ t_{PHL}	Propagation Delay Time D/ $\overline{\text{U}}$ to MIN/MAX	4.5		24	45		56		68	ns
$t_{\text{PLH}}/$ t_{PHL}	Propagation Delay Time $\overline{\text{CE}}$ to $\overline{\text{RCO}}$	4.5		20	40		58		65	ns
$t_{\text{TLH}}/$ t_{THL}	Output Transition Time	4.5		7	15		19		22	ns

AC Waveforms

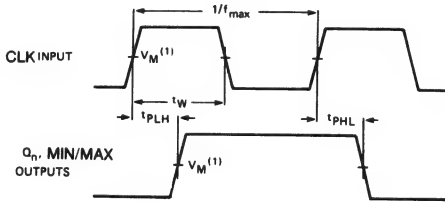


Fig. 3 Waveforms showing the clock (CLK) to output (Q_n) propagation delays, the clock pulse width and the maximum clock pulse frequency.

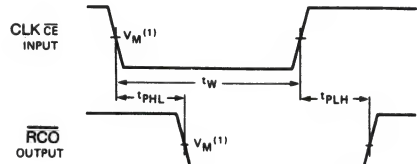


Fig. 4 Waveforms showing the clock and count enable inputs (CLK \overline{CE}) to ripple clock output (RCO) propagation delays and the CE pulse width.

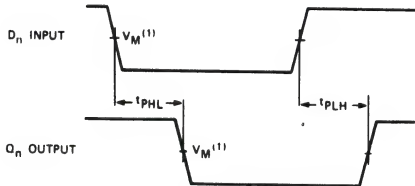


Fig. 5 Waveforms showing the input (D_n) to output (Q_n) propagation delays.

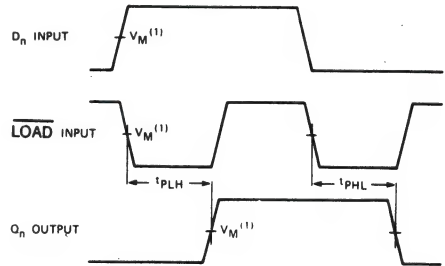


Fig. 6 Waveforms showing the input (\overline{LOAD}) to output (Q_n) propagation delays.

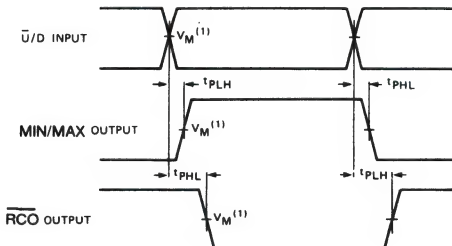


Fig. 7 Waveforms showing the up/down count input ($\overline{U/D}$) to terminal count and ripple clock output (\overline{RCO} , MIN/MAX) propagation delays.

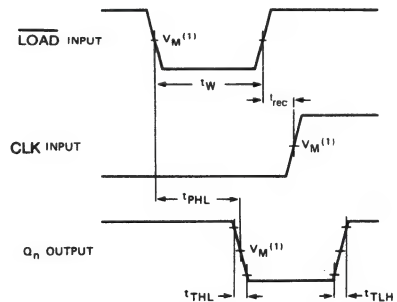


Fig. 8 Waveforms showing the parallel load input (\overline{LOAD}) pulse width, recovery time to clock (CLK) and the output (Q_n) transition times.

AC Waveforms

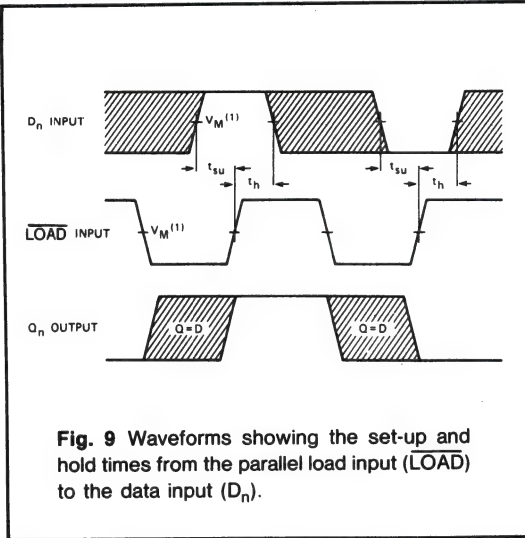


Fig. 9 Waveforms showing the set-up and hold times from the parallel load input (\overline{LOAD}) to the data input (D_n).

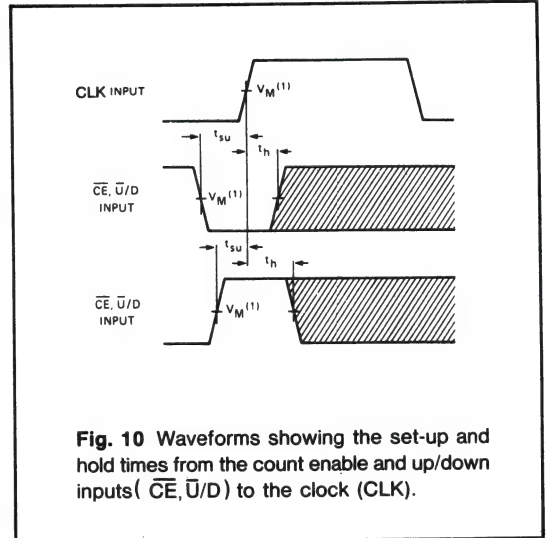


Fig. 10 Waveforms showing the set-up and hold times from the count enable and up/down inputs (\overline{CE} , $\overline{U/D}$) to the clock (CLK).

Note to AC waveforms

- (1) HC : $V_M = 50\%$; $V_I = \text{GND to } V_{CC}$.
HCT : $V_M = 1.3V$; $V_I = \text{GND to } 3V$.

Note to Figs 9 and 10

The shaded areas indicate when the input is permitted to change for predictable output performance.

GD54/74HC192, GD54/74HCT192

SYNCHRONOUS DECADE UP/DOWN COUNTER WITH A CLEAR & DUAL CLOCKS

General Description

These devices are identical in pinout to the 54/74LS192. This decade counter has two separate clock inputs; an up count input and a down count input. It can be preset by applying the desired value in BCD to the preset inputs and then bringing the load input low. Up or down counting is achieved by bringing the load input high and clocking the appropriate clock input. The state of the counter changes on the rising edge of the appropriate clock. All 4 internal stages can be cleared by putting a high level on the clear input independently of either count input. This counter can be cascaded by connecting carry and borrow of the least significant counter to clock-up and clock-down respectively, of the next more significant counter.

Features

- Low Power consumption characteristic of CMOS devices
- Output drive capability: 10 LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts
for HCT 4.5 to 5.5 volts
- Low input current: 1 μ A Max.
- Low quiescent current: 80 μ A Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs

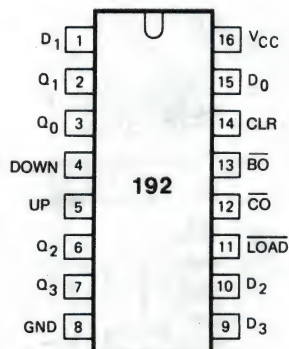
Function Table

OPERATING MODE	INPUTS								OUTPUTS					
	CLR	LOAD	UP	DOWN	D ₀	D ₁	D ₂	D ₃	Q ₀	Q ₁	Q ₂	Q ₃	C \overline{O}	B \overline{O}
reset (clear)	H	X	X	L	X	X	X	X	L	L	L	L	H	L
	H	X	X	H	X	X	X	X	L	L	L	L	H	H
parallel load	L	L	X	L	L	L	L	L	L	L	L	L	H	L
	L	L	X	H	L	L	L	L	L	L	L	L	H	H
	L	L	L	X	H	X	X	H	$Q_n = D_n$ $Q_n = D_n$				L	H
	L	L	H	X	H	X	X	H					H	H
count up	L	H	\uparrow	H	X	X	X	X	count up				H*	H
count down	L	H	H	\uparrow	X	X	X	X	count down				H	H**

* $\overline{C\overline{O}}$ = UP at terminal count up (HLLH)

** $\overline{B\overline{O}}$ = DOWN at terminal count down (LLLL)

Pin Configuration



Suffix-Blank : Plastic Dual In Line Package
 Suffix-J : Ceramic Dual In Line Package
 Suffix-D : Small Outline Package

Logic Diagram

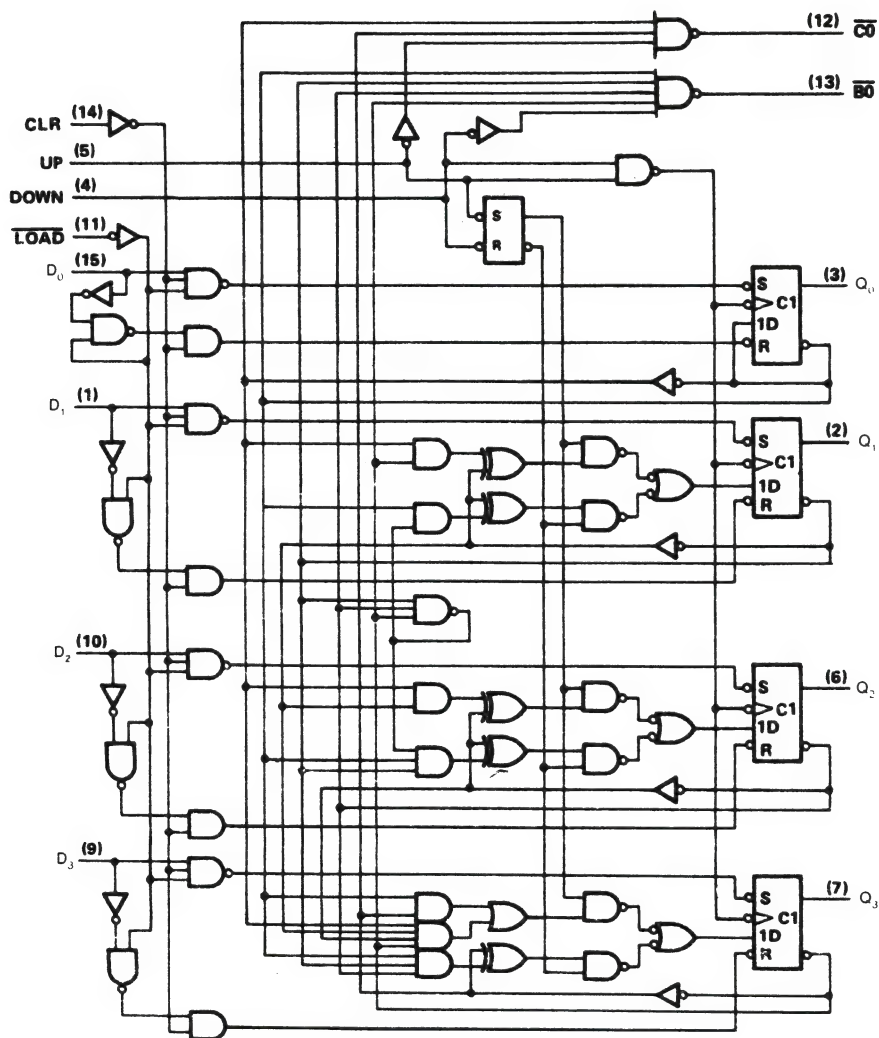
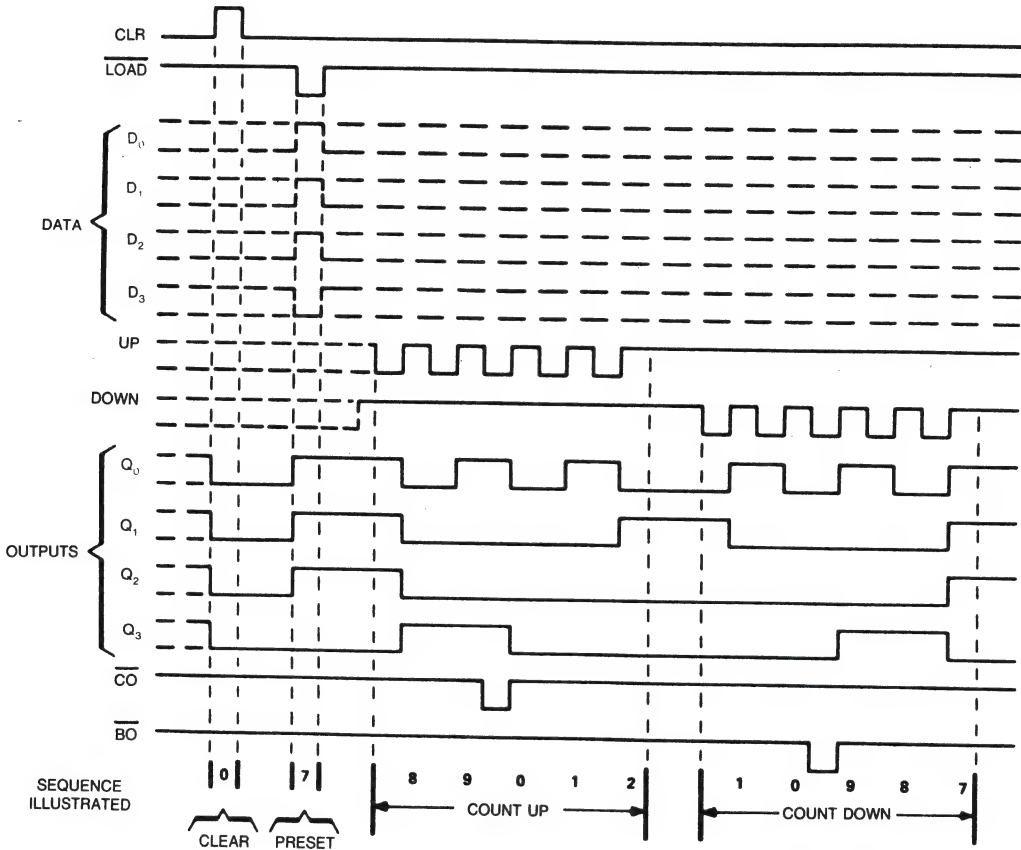


Fig. 1 Logic diagram

Typical Clear, Load, and Count Sequence

Illustrated below is the following sequence:

1. Clear outputs to zero.
2. Load (preset) to BCD seven.
3. Count up to eight, nine, carry, zero, one, and two.
4. Count down to one, zero, borrow, nine, eight, and seven.



NOTES: A. Clear overrides load, data, and count inputs.

B. When counting up, count-down input must be high; when counting down, count-up input must be high.

Fig. 2 Typical clear, load, and count sequence

Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC Supply voltage		-0.5	+7	V
I_{IK}, I_{OK}	DC input or output diode current	for $V_I < -0.5$ or $V_I > V_{CC} + 0.5V$		20	mA
I_O	DC output source or sink current	for $-0.5V < V_O < V_{CC} + 0.5V$		25	mA
I_{CC}	DC V_{CC} or GND current			50	mA
T_{stg}	Storage temperature range		-65	150	°C
P_D	Power dissipation per package	above +70°C: derate linearly with 8mW/K		500	mW
T_L	Lead temperature	At distance $1/16 \pm 1/32$ in. from case for 60 sec(CERAMIC) 10 sec(PLASTIC)		300 260	°C

Recommended Operating Conditions

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range V_{CC} : GD54/74HC Types GD54/74HCT Types	2 4.5	6 5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A : GD74 Types GD54 Types	-40 -55	+85 +125	°C
Input Rise and Fall times t_r, t_f : GD54/74HC Types at 2V at 4.5V at 6V GD54/74HCT Types at 4.5 V		1000 500 400 500	ns

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HC192		GD54HC192		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2		1.5 3.15 4.2		V
V _{IL}	LOW level input voltage		2.0 4.5 6.0			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH}	I _{OH} =-20μA	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0	1.9 4.4 5.9		1.9 4.4 5.9		V
			I _{OH} =-4mA	4.5 6.0	3.98 5.48	4.3 5.2	3.84 5.34		3.7 5.2		
		or V _{IL}	I _{OH} =-4mA	4.5 6.0	3.98 5.48	4.3 5.2	3.84 5.34		3.7 5.2		
			I _{OH} =-5.2mA	4.5 6.0	3.98 5.48	4.3 5.2	3.84 5.34		3.7 5.2		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH}	I _{OL} =20μA	2.0 4.5 6.0			0.1 0.1 0.1	0.1 0.1 0.1		0.1 0.1 0.1	V
			I _{OL} =4mA	4.5 6.0		0.17 0.15	0.26 0.26	0.33 0.33		0.4 0.4	
		or V _{IL}	I _{OL} =4mA	4.5 6.0		0.17 0.15	0.26 0.26	0.33 0.33		0.4 0.4	
			I _{OL} =5.2mA	4.5 6.0		0.17 0.15	0.26 0.26	0.33 0.33		0.4 0.4	
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	6.0			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	6.0			8		80		160	μA

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HCT192		GD54HCT192		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		4.5 to 5.5	2.0			2.0		2.0		V
V _{IL}	LOW level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH}	I _{OH} =-20μA	4.5	4.4	4.5	4.4		4.4		V
		or V _{IL}	I _{OH} =-4mA	4.5	3.98	4.3	3.84		3.7		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH}	I _{OL} =20μA	4.5			0.1	0.1		0.1	V
		or V _{IL}	I _{OL} =4mA	4.5		0.17	0.26	0.33		0.4	
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	5.5			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	5.5			8		80		160	μA

Timing Requirements for HC $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER		V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HC192		GD54HC192		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_w	Pulse width	CLR high, $\overline{\text{LOAD}}$ low UP, DOWN high or low	2.0	120			150		180		ns
			4.5	24			30		36		
			6.0	20			26		30		
t_{su}	Setup time	D_n to $\overline{\text{LOAD}}$	2.0	100			125		150		ns
			4.5	20			25		30		
			6.0	17			20		26		
t_{rec}	Recovery time	CLR, $\overline{\text{LOAD}}$ to UP, DOWN	2.0	50			65		75		ns
			4.5	10			73		15		
			6.0	9			11		13		
t_h	Hold time	D_n to $\overline{\text{LOAD}}$ UP high after DOWN \uparrow DOWN high after UP \uparrow	2.0	0			0		0		ns
			4.5	0			0		0		
			6.0	0			0		0		

AC Characteristics for HC: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER		V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HC192		GD54HC192		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
f_{max}	Maximum clock pulse frequency		2.0	4.2	8		3.3		2.8		MHz
			4.5	21	55		17		14		
			6.0	24	60		19		16		
$t_{PLH}/$ t_{PHL}	Propagation Delay Time UP to \overline{CO}		2.0		50	125		155		190	ns
			4.5		16	25		31		38	
			6.0		14	21		26		32	
$t_{PLH}/$ t_{PHL}	Propagation Delay Time DOWN to \overline{BO}		2.0		50	125		155		190	ns
			4.5		16	25		31		38	
			6.0		14	21		26		32	
$t_{PLH}/$ t_{PHL}	Propagation Delay Time UP or DOWN to Q_n		2.0		150	215		270		325	ns
			4.5		33	43		54		65	
			6.0		28	37		46		55	
$t_{PLH}/$ t_{PHL}	Propagation Delay Time $\overline{\text{LOAD}}$ TO Q_n		2.0		150	215		270		325	ns
			4.5		33	43		54		65	
			6.0		28	37		46		55	
$t_{PLH}/$ t_{PHL}	Propagation Delay Time CLR to Q_n		2.0		140	200		250		300	ns
			4.5		28	40		50		60	
			6.0		24	34		43		51	
$t_{TLH}/$ t_{THL}	Output Transition Time		2.0		19	75		95		110	ns
			4.5		7	15		19		22	
			6.0		6	13		16		19	

Timing Requirements for HCT: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER		V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HCT192		GD54HCT192		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_w	Pulse width	CLR high, $\overline{\text{LOAD}}$ low UP, DOWN high or low	4.5	26			32		38		ns
t_{su}	Setup time	D_n to $\overline{\text{LOAD}}$	4.5	22			27		32		ns
t_{rec}	Recovery time	CLR, $\overline{\text{LOAD}}$ to UP, DOWN	4.5	12			15		19		ns
t_h	Hold time	D_n to $\overline{\text{LOAD}}$ UP high after DOWN \uparrow DOWN high after UP \uparrow	4.5	0			0		0		ns

AC Characteristics for HCT: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HCT192		GD54HCT192		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
f_{max}	Maximum Clock Pulse Frequency	4.5	20			16		13		MHz
$t_{PLH}/$ t_{PHL}	Propagation Delay Time Up to $\overline{\text{CO}}$	4.5		20	30		35		42	ns
$t_{PLH}/$ t_{PHL}	Propagation Delay Time DOWN to $\overline{\text{BO}}$	4.5		20	30		35		42	ns
$t_{PLH}/$ t_{PHL}	Propagation Delay Time UP, DOWN to Q_n	4.5		37	47		58		69	ns
$t_{PLH}/$ t_{PHL}	Propagation Delay Time $\overline{\text{LOAD}}$ to Q_n	4.5		37	47		58		69	ns
$t_{PLH}/$ t_{PHL}	Propagation Delay Time CLR to Q_n	4.5		32	44		54		64	ns
$t_{TLH}/$ t_{THL}	Output Transition Time	4.5		7	15		19		22	ns

AC Waveforms

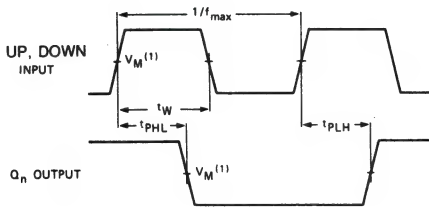


Fig. 3 Waveforms showing the clock (UP, DOWN) to output (Q_n) propagation delays, the clock pulse width and the maximum clock pulse frequency.

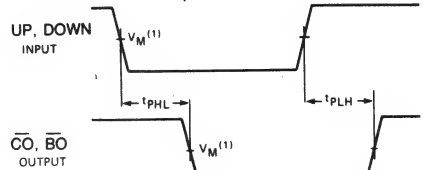


Fig. 4 Waveforms showing the clock (UP, DOWN) to terminal count output (\overline{CO} , \overline{BO}) propagation delays.

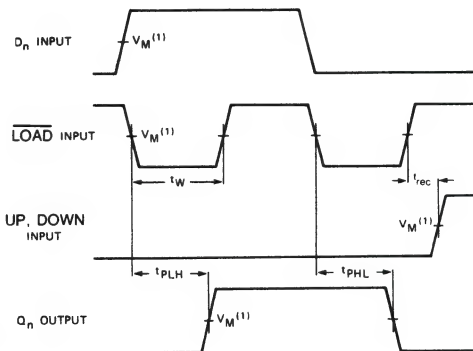


Fig. 5 Waveforms showing the parallel load input (LOAD) to Q_n output propagation delays and recovery time to clock input (UP DOWN)

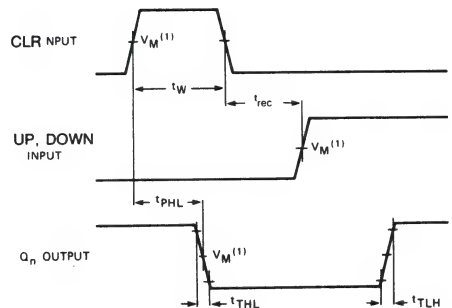


Fig. 6 Waveforms showing the master clear input (CLR) pulse width, CLR to Q_n propagation delays, CLR to (UP, DOWN) recovery time and output transition times.

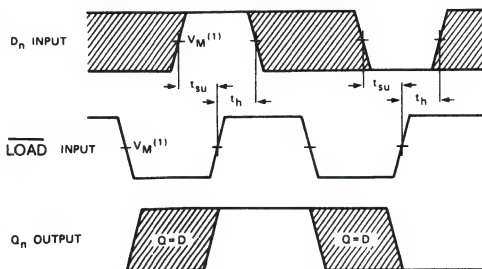


Fig. 7 Waveforms showing the data input (D_n) to parallel load input (LOAD) set-up and hold times.

Note to Fig. 7

The shaded areas indicate when the input is permitted to change for predictable output performance.

Note to AC waveforms

- (1) HC : $V_M=50\%$; $V_I=GND$ to V_{CC} .
- HCT : $V_M=1.3V$; $V_I=GND$ to $3V$.

GD54/74HC193, GD54/74HCT193

SYNCHRONOUS 4-BIT BINARY UP/DOWN COUNTER WITH A CLEAR & DUAL CLOCKS

General Description

These devices are identical in pinout to the 54/74LS193. This 4-bit binary counter has two separate clock inputs: an up count input and a down count input. It can be preset by applying the desired value in 4 bit binary to the preset inputs and then bringing the load input low. Up or down counting is achieved by bringing the load input high and clocking the appropriate clock input. The counter state changes on the rising edge of the appropriate clock. All 4 internal stages can be cleared by putting a high level on the clear input independently of either count input. This counter can be cascaded by connecting carry and borrow of the least significant counter to clock-up and clock-down respectively, of the next more significant counter.

Features

- Low Power consumption characteristic of CMOS devices
- Output drive capability: 10 LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts
for HCT 4.5 to 5.5 volts
- Low input current: 1 μ A Max.
- Low quiescent current: 20 μ A Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protectin on all inputs

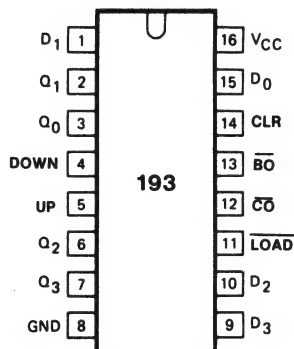
Function Table

OPERATING MODE	INPUTS								OUTPUTS					
	CLR	LOAD	UP	DOWN	D ₀	D ₁	D ₂	D ₃	Q ₀	Q ₁	Q ₂	Q ₃	\overline{CO}	\overline{BO}
reset (clear)	H	X	X	L	X	X	X	X	L	L	L	L	H	L
	H	X	X	H	X	X	X	X	L	L	L	L	H	H
parallel load	L	L	X	L	L	L	L	L	L	L	L	L	H	L
	L	L	X	H	L	L	L	L	L	L	L	L	H	H
	L	L	L	X	H	X	X	H	H	H	H	H	L	H
	L	L	H	X	H	H	H	H	H	H	H	H	H	H
count up	L	H	↑	H	X	X	X	X	count up				H*	H
count down	L	H	H	↑	X	X	X	X	count down				H	H**

* \overline{CO} = UP at terminal count up (HHHH)

** \overline{BO} = DOWN at terminal count down (LLLL)

Pin Configuration



Suffix-Blank : Plastic Dual In Line Package
 Suffix-J : Ceramic Dual In Line Package
 Suffix-D : Small Outline Package

Logic Diagram Logic Diagram

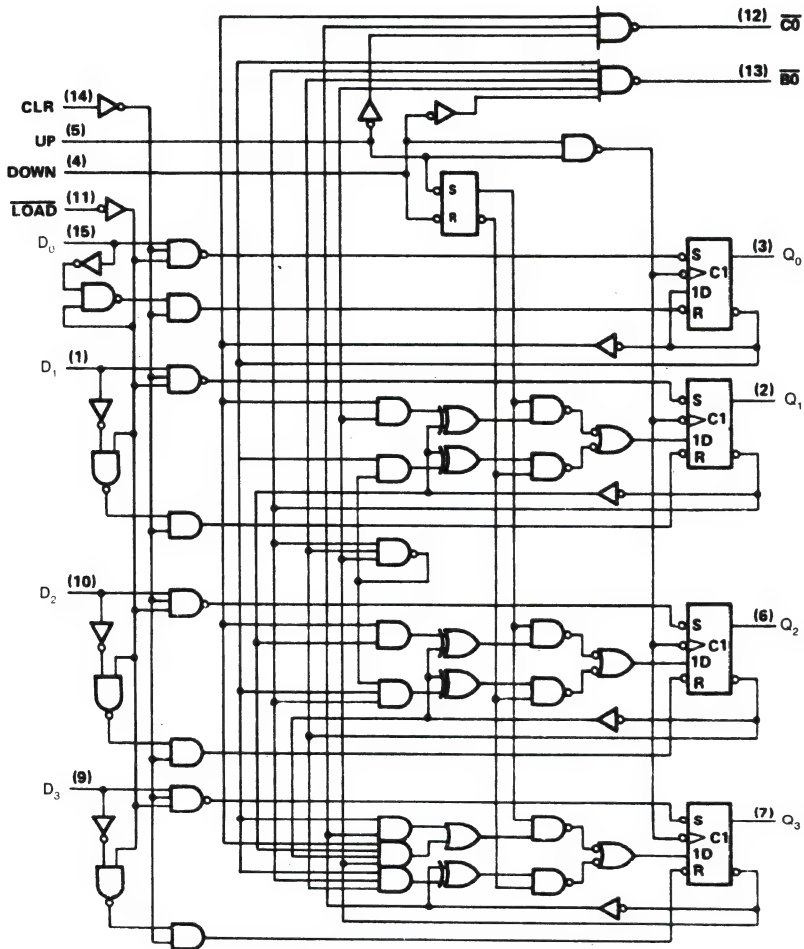
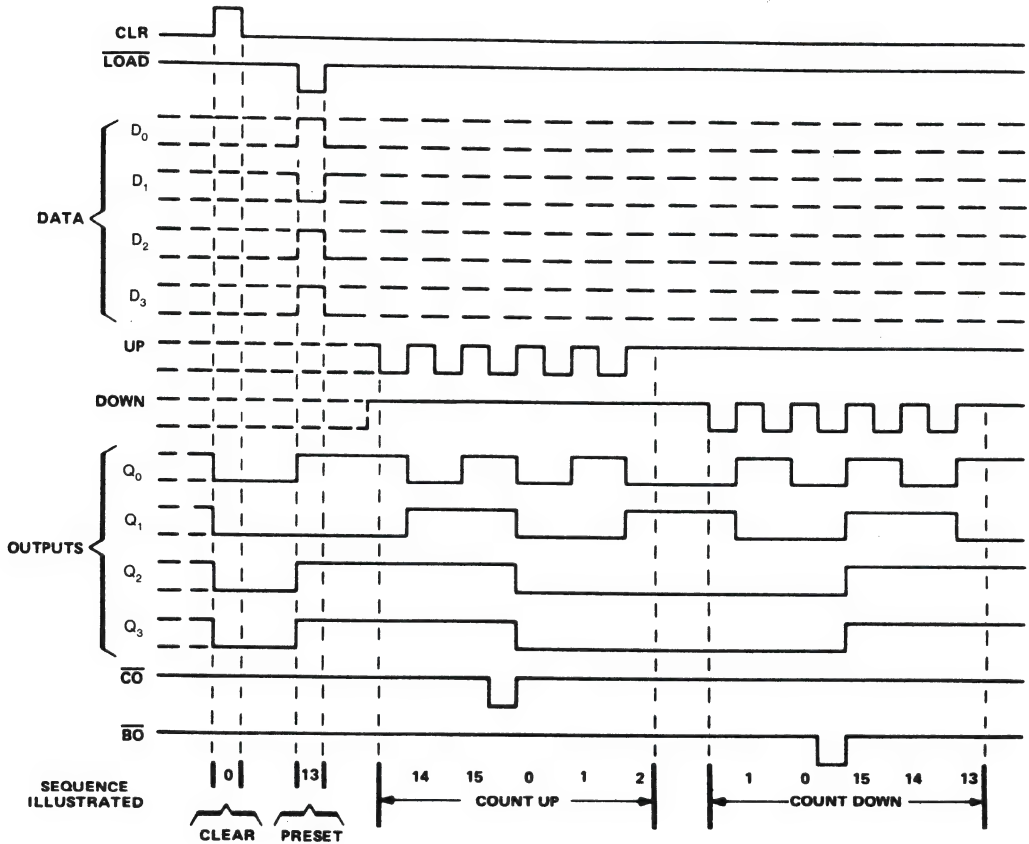


Fig. 2 Logic diagram

Typical Clear, Load, and Count Sequences

Illustrated below is the following sequence:

1. Clear outputs to zero.
2. Load (preset) to binary thirteen.
3. Count up to fourteen, fifteen, carry, zero, one, and two.
4. Count down to one, zero, borrow, fifteen, fourteen, and thirteen.



NOTES: A. Clear overrides load, data, and count inputs.

B. When counting up, count-down input must be high; when counting down, count-up input must be high.

Fig. 2 Typical clear, load, and count Sequence

Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC Supply voltage		-0.5	+7	V
I_{IK}, I_{OK}	DC input or output diode current	for $V_I < -0.5$ or $V_I > V_{CC} + 0.5V$		20	mA
I_O	DC output source or sink current	for $-0.5V < V_O < V_{CC} + 0.5V$		25	mA
I_{CC}	DC V_{CC} or GND current			50	mA
T_{stg}	Storage temperature range		-65	150	°C
P_D	Power dissipation per package	above +70°C: derate linearly with 8mW/K		500	mW
T_L	Lead temperature	At distance 1/16 ± 1/32 in. from case for 60 sec(CERAMIC) 10 sec(PLASTIC)		300 260	°C

Recommended Operating Conditions

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range V_{CC} : GD54/74HC Types GD54/74HCT Types	2 4.5	6 5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A : GD74 Types GD54 Types	-40 -55	+85 +125	°C
Input Rise and Fall times t_r, t_f : GD54/74HC Types at 2V at 4.5V at 6V GD54/74HCT Types at 4.5 V		1000 500 400 500	ns

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HC193		GD54HC193		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2		1.5 3.15 4.2		V
V _{IL}	LOW level input voltage		2.0 4.5 6.0			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH}	I _{OH} =-20μA	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0	1.9 4.4 5.9		1.9 4.4 5.9		V
			I _{OH} =-4mA	4.5 6.0	3.98 5.48	4.3 5.2	3.84 5.34		3.7 5.2		
		or V _{IL}	I _{OH} =-5.2mA	4.5 6.0	3.98 5.48	4.3 5.2	3.84 5.34		3.7 5.2		
			I _{OH} =-5.2mA	4.5 6.0	3.98 5.48	4.3 5.2	3.84 5.34		3.7 5.2		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH}	I _{OL} =20μA	2.0 4.5 6.0			0.1 0.1 0.1	0.1 0.1 0.1		0.1 0.1 0.1	V
			I _{OL} =4mA	4.5 6.0		0.17 0.15	0.26 0.26	0.33 0.33		0.4 0.4	
		or V _{IL}	I _{OL} =4mA	4.5 6.0		0.17 0.15	0.26 0.26	0.33 0.33		0.4 0.4	
			I _{OL} =5.2mA	4.5 6.0		0.17 0.15	0.26 0.26	0.33 0.33		0.4 0.4	
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	6.0			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	6.0			8		80		160	μA

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HCT193		GD54HCT193		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		4.5 to 5.5	2.0			2.0		2.0		V
V _{IL}	LOW level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH}	I _{OH} =-20μA	4.5	4.4	4.5	4.4		4.4		V
		or V _{IL}	I _{OH} =-4mA	4.5	3.98	4.3	3.84		3.7		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH}	I _{OL} =20μA	4.5			0.1	0.1		0.1	V
		or V _{IL}	I _{OL} =4mA	4.5		0.17	0.26	0.33		0.4	
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	5.5			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	5.5			8		80		160	μA

Timing Requirements for HC: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER		V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HC193		GD54HC193		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_w	Pulse width	CLR high, $\overline{\text{LOAD}}$ low UP, DOWN high or low	2.0 4.5 6.0	120 24 20			150 30 26		180 36 30		ns
t_{su}	Setup time	D_n to $\overline{\text{LOAD}}$	2.0 4.5 6.0	100 20 17			125 25 20		150 30 26		ns
t_{rec}	Recovery time	CLR, $\overline{\text{LOAD}}$ to UP, DOWN	2.0 4.5 6.0	50 10 9			65 13 11		75 15 13		ns
t_h	Hold time	D_n to $\overline{\text{LOAD}}$ UP high after DOWN \uparrow DOWN high after UP \uparrow	2.0 4.5 6.0	0 0 0			0 0 0		0 0 0		ns

AC Characteristics for HC: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER		V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HC193		GD54HC193		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
f_{max}	Maximum Clock Pulse Frequency		2.0 4.5 6.0	4.2 21 24	8 55 60		3.3 17 19		2.8 14 16		MHz
$t_{PLH}/$ t_{PHL}	Propagation Delay Time UP to $\overline{\text{CO}}$, DOWN to $\overline{\text{BO}}$		2.0 4.5 6.0		50 16 14	125 25 21		155 31 26		190 38 32	ns
$t_{PLH}/$ t_{PHL}	Propagation Delay Time UP, DOWN to Q_n		2.0 4.5 6.0		150 33 28	215 43 37		270 54 46		325 65 55	ns
$t_{PLH}/$ t_{PHL}	Propagation Delay Time $\overline{\text{LOAD}}$ to Q_n		2.0 4.5 6.0		150 33 28	215 43 37		270 54 46		325 65 55	ns
$t_{PLH}/$ t_{PHL}	Propagation Delay Time CLR to Q_n		2.0 4.5 6.0		140 28 24	200 40 34		250 50 43		300 60 51	ns
$t_{TLH}/$ t_{THL}	Output Transition Time		2.0 4.5 6.0		19 7 6	75 15 13		95 19 16		110 22 19	ns

Timing Requirements for HCT: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER		V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HCT193		GD54HCT193		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_w	Pulse width	CLR high, $\overline{\text{LOAD}}$ low UP, DOWN high or low	4.5	26			32		38		ns
t_{su}	Setup time	D_n to $\overline{\text{LOAD}}$	4.5	22			27		32		ns
t_{rec}	Recovery time	CLR, $\overline{\text{LOAD}}$ to UP, DOWN	4.5	12			15		19		ns
t_h	Hold time	D_n to $\overline{\text{LOAD}}$ UP high after DOWN \uparrow DOWN high after UP \uparrow	4.5	0			0		0		ns

AC Characteristics for HCT: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HCT193		GD54HCT193		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
f_{max}	Maximum clock pulse frequency	4.5	20			16		13		MHz
$t_{PLH}/$ t_{PHL}	Propagation Delay Time UP to \overline{CO} , DOWN to \overline{BO}	4.5		20	30		35		42	ns
$t_{PLH}/$ t_{PHL}	Propagation Delay Time UP, DOWN to Q_n	4.5		37	47		58		69	ns
$t_{PLH}/$ t_{PHL}	Propagation Delay Time $\overline{\text{LOAD}}$ to Q_n	4.5		37	47		58		69	ns
$t_{PLH}/$ t_{PHL}	Propagation Delay Time CLR to Q_n	4.5		32	44		54		64	ns
$t_{TLH}/$ t_{THL}	Output Transition Time	4.5		7	15		19		22	ns

AC Waveforms

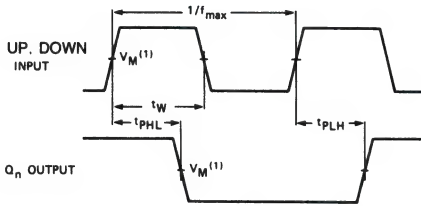


Fig. 3 Waveforms showing the clock (UP, DOWN) to output (Q_n) propagation delays, the clock pulse width and the maximum clock pulse frequency.

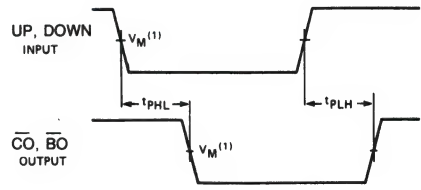


Fig. 4 Waveforms showing the clock (UP, DOWN) to terminal count output ($\overline{CO}, \overline{BO}$) propagation delays.

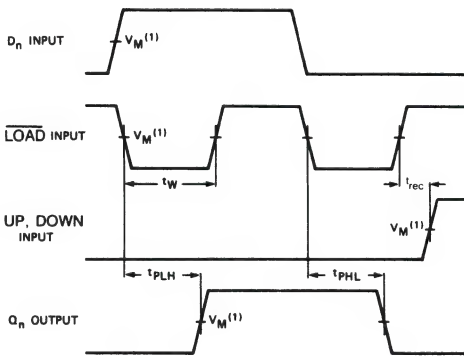


Fig. 5 Waveforms showing the parallel load input (\overline{LOAD}) to Q_n output propagation delays and recovery time to clock input (UP, DOWN)

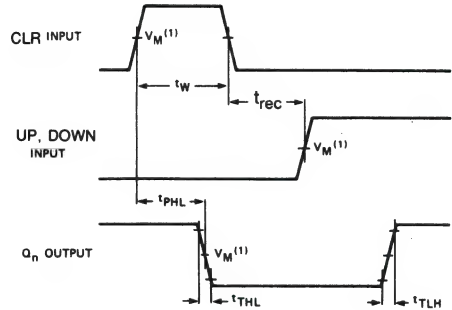


Fig. 6 Waveforms showing the master clear input (CLR) pulse width, CLR to Q_n propagation delays, CLR to (UP, DOWN) recovery time and output transition times.

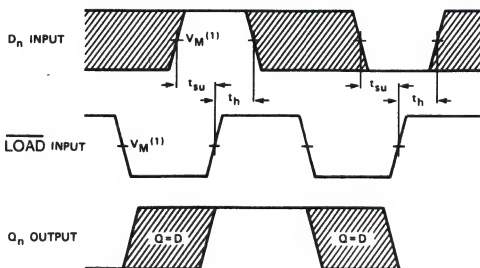


Fig. 7 Waveforms showing the data input (D_n) to parallel load input (\overline{LOAD}) set-up and hold times.

Note to Fig. 7

The shaded areas indicate when the input is permitted to change for predictable output performance.

Note to AC waveforms

- (1) HC : $V_M = 50\%$; $V_i = \text{GND to } V_{CC}$.
HCT : $V_M = 1.3V$; $V_i = \text{GND to } 3V$.

GD54/74HC194, GD54/74HCT194

4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER

General Description

These devices are identical in pinout to the 54/74LS194. This circuit has virtually all of the features a system designer may want in a shift register. It features parallel load, parallel outputs, right & left shift serial inputs, mode control inputs, and a direct overriding clear line. This register has four distinct modes of operation:

Inhibit Clock (Do nothing)

Shift Right (In the direction Q_0 toward Q_3)

Shift Left (In the direction Q_3 toward Q_0)

Parallel (Broadside) Load

These devices are characterized for operation over wide temperature ranges to meet industry and military specifications.

Features

- Low Power consumption characteristic of CMOS devices
- Output drive capability: 10 LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts
for HCT 4.5 to 5.5 volts
- Low input current: $1\mu A$ Max.
- Low quiescent current: $80\mu A$ Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs

Function Table

OPERATING MODES	INPUTS							OUTPUTS			
	CLK	CLR	S_1	S_0	SR	SL	D_n	Q_0	Q_1	Q_2	Q_3
reset (clear)	X	L	X	X	X	X	X	L	L	L	L
hold ("do nothing")	X	H	I	I	X	X	X	q_0	q_1	q_2	q_3
shift left	↑	H	h	I	X	I	X	q_1	q_2	q_3	L
	↑	H	h	I	X	h	X	q_1	q_2	q_3	H
shift right	↑	H	I	h	I	X	X	L	q_0	q_1	q_2
	↑	H	I	h	h	X	X	H	q_0	q_1	q_2
parallel load	↑	H	h	h	X	X	d_n	d_0	d_1	d_2	d_3

H = HIGH voltage level

h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CLK transition

L = LOW voltage level

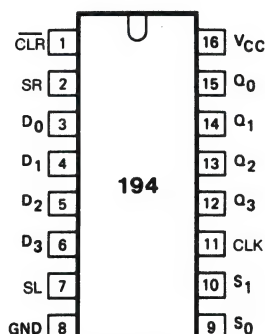
I = LOW voltage level one set-up time prior to the LOW-to-HIGH CLK transition

q,d = lower case letters indicate the state of the referenced input for output one set-up time prior to the LOW-to-HIGH CLK transition

X = don't care

↑ = LOW-to-HIGH CLK transition

Pin Configuration



Suffix-Blank : Plastic Dual In Line Package

Suffix-J : Ceramic Dual In Line Package

Suffix-D : Small Outline Package

Logic Diagram

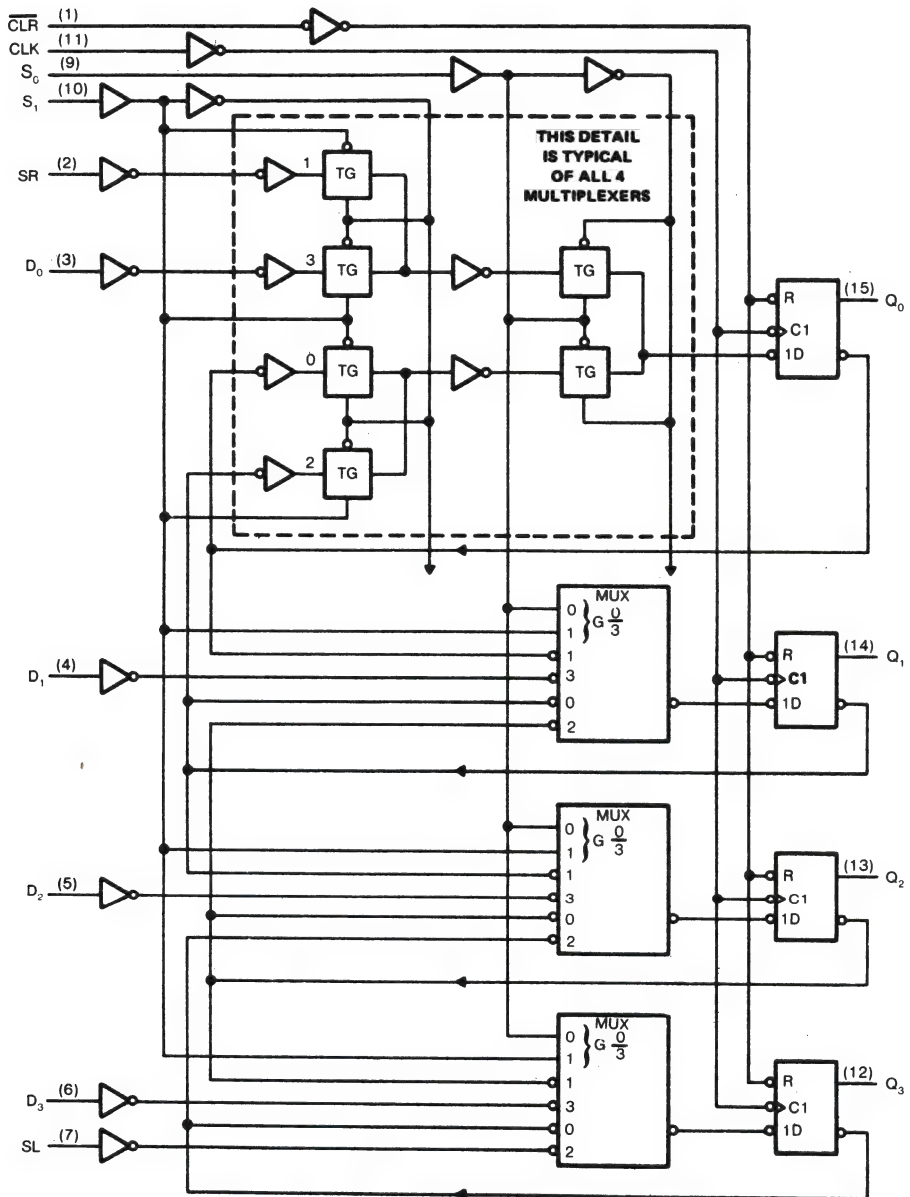


Fig. 1. Logic diagram

Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC Supply voltage		-0.5	+7	V
I_{IK}, I_{OK}	DC input or output diode current	for $V_I < -0.5$ or $V_I > V_{CC} + 0.5V$		20	mA
I_O	DC output source or sink current	for $-0.5V < V_O < V_{CC} + 0.5V$		25	mA
I_{CC}	DC V_{CC} or GND current			50	mA
T_{stg}	Storage temperature range		-65	150	°C
P_D	Power dissipation per package	above +70°C: derate linearly with 8mW/K		500	mW
T_L	Lead temperature	At distance 1/16±1/32 in. from case for 60 sec(CERAMIC) 10 sec(PLASTIC)		300 260	°C

Recommended Operating Conditions

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range V_{CC} : GD54/74HC Types GD54/74HCT Types	2 4.5	6 5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A : GD74 Types GD54 Types	-40 -55	+85 +125	°C
Input Rise and Fall times t_r, t_f : GD54/74HC Types at 2V at 4.5V at 6V GD54/74HCT Types at 4.5 V		1000 500 400 500	ns

Typical Clear, Load, Right-Shift, Left-Shift, Inhibit and Clear Sequences

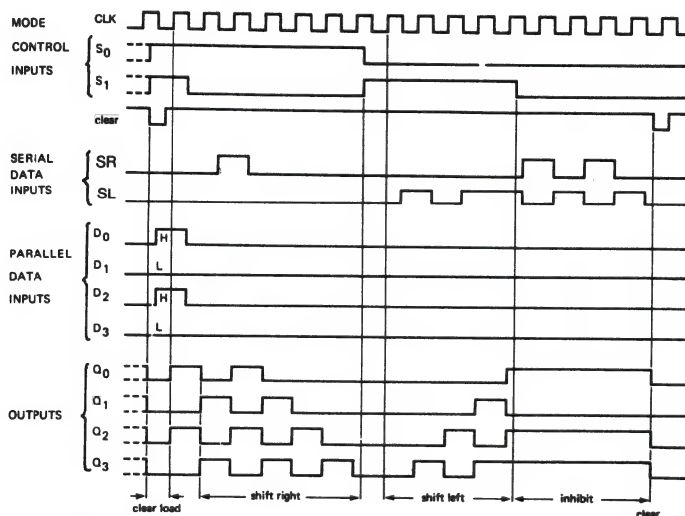


Fig. 2 Typical load, right-shift, left-shift, inhibit and clear sequences

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION		V _{CC} (V)	T _A =25°C			GD74HC194		GD54HC194		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage			2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2		1.5 3.15 4.2		V
V _{IL}	LOW level input voltage			2.0 4.5 6.0			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH}	I _{OH} =-20μA	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V
		or V _{IL}	I _{OH} =-4mA	4.5 6.0	3.98 5.48	4.3 5.2		3.84 5.34		3.7 5.2		
			I _{OH} =-5.2mA									
V _{OL}	LOW level output voltage	V _{IN} =V _{IH}	I _{OL} =20μA	2.0 4.5 6.0			0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V
		or V _{IL}	I _{OL} =4mA	4.5 6.0		0.17 0.15	0.26 0.26		0.33 0.33		0.4 0.4	
			I _{OL} =5.2mA									
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND		6.0			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA		6.0			8		80		160	μA

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION		V _{CC} (V)	T _A =25°C			GD74HCT194		GD54HCT194		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage			4.5 to 5.5	2.0			2.0		2.0		V
V _{IL}	LOW level input voltage			4.5 to 5.5			0.8		0.8		0.8	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH}	I _{OH} =-20μA	4.5	4.4	4.5		4.4		4.4		V
		or V _{IL}	I _{OH} =-4mA	4.5	3.98	4.3		3.84		3.7		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH}	I _{OL} =20μA	4.5			0.1		0.1		0.1	V
		or V _{IL}	I _{OL} =4mA	4.5		0.17	0.26		0.33		0.4	
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND		5.5			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA		5.5			8		80		160	μA

Timing Requirements for HC: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER		V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HC194		GD54HC194		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_w	Pulse width	$\overline{\text{CLR}}$ low, CLK	2.0	80			100		120		ns
			4.5	16			20		24		
			6.0	14			17		20		
t_{su}	Setup time	Sn, Dn to CLK	2.0	80			100		120		ns
			4.5	16			20		24		
			6.0	12			17		20		
t_h	Hold time	Dn to CLK	2.0	0			0		0		ns
			4.5	0			0		0		
			6.0	0			0		0		

AC Characteristics for HC: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER		V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HC194		GD54HC194		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
f_{max}	Maximum Clock Pulse Frequency		2.0	6			5		4.2		Mhz
			4.5	31			25		21		
			6.0	36			29		25		
$t_{PLH}/$ t_{PHL}	Propagation Delay Time CLK to Qn		2.0		47	145		180		220	ns
			4.5		16	29		36		44	
			6.0		13	25		31		36	
$t_{PLH}/$ t_{PHL}	Propagation Delay Time $\overline{\text{CLR}}$ to Qn		2.0		39	140		175		210	ns
			4.5		13	28		35		42	
			6.0		11	24		30		35	
$t_{THL}/$ t_{THL}	Output Transition Time		2.0		19	75		95		110	ns
			4.5		7	15		19		22	
			6.0		6	13		16		19	

Timing Requirements for HCT: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER		V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HCT194		GD54HCT194		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_w	Pulse width	$\overline{\text{CLR}}$ low, CLK	4.5	16			20		24		ns
t_{su}	Setup time	Sn, Dn to CLK	4.5	16			20		24		ns
t_h	Hold time	Dn to CLK	4.5	0			0		0		ns

AC Characteristics for HCT: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HCT194		GD54HCT194		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
f_{max}	Maximum clock pulse frequency	4.5	30			23		20		Mhz
$t_{PLH}/$ t_{PHL}	Propagation Delay Time $\overline{\text{CLK}}$ to Qn	4.5		19	32		40		48	ns
$t_{PLH}/$ t_{PHL}	Propagation Delay Time $\overline{\text{CLR}}$ to Qn	4.5		16	31		39		46	ns
$t_{THL}/$ t_{TTL}	Output Transition Time	4.5		7	15		19		22	ns

AC Waveforms

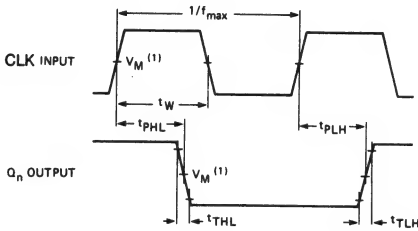


Fig. 3 Waveforms showing the clock (CLK) to output (Q_n) propagation delays, the clock pulse width, the output transition times and the maximum clock frequency.

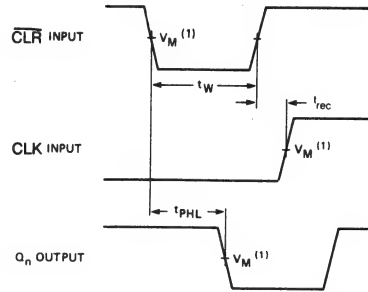


Fig. 4 Waveforms showing the master clear (\overline{CLR}) pulse width, the master clear to output (Q_n) propagation delays and CLK the master clear to clock recovery time.

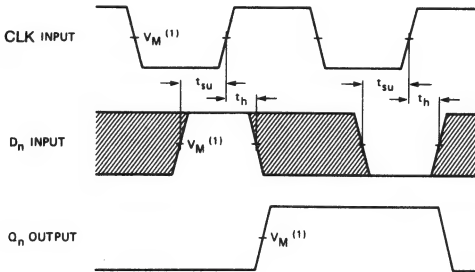


Fig. 5 Waveforms showing the set-up and hold times from the data inputs (D_n) to the clock (CLK).

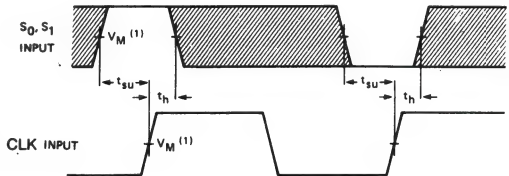


Fig. 6 Waveforms showing the set-up and hold times from the mode control inputs (S_n) to the clock input (CLK).

Note to Fig5 and 6

The shaded areas indicate when the input is permitted to change for predictable output performance.

Note to AC waveforms

- (1) HC : $V_M = 50\%$; $V_i = \text{GND}$ to V_{CC} .
HCT : $V_M = 1.3V$; $V_i = \text{GND}$ to $3V$.

GD54/74HC195, GD54/74HCT195

4-BIT PARALLEL-ACCESS SHIFT REGISTER

General Description

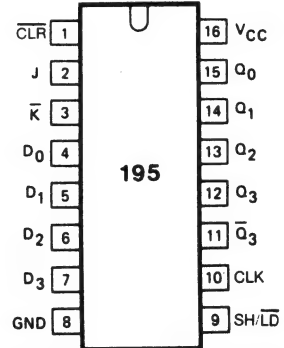
These devices are identical in pinout to the 54/74LS195. This circuit features parallel inputs, parallel outputs, J-K serial inputs, shift/load control input, and a direct overriding clear. This shift register can operate in two modes:

Parallel (Broadsied) Load

Shift Right (In the direction Q_0 toward Q_3)

Parallel loading is accomplished by applying the four bits of data, and taking the shift/load control input low. Serial shifting occurs synchronously when the shift/load control input is high, where serial data are entered through the J-K inputs. These devices are characterized for operation over wide temperature ranges to meet industry and military specifications.

Pin Configuration



Suffix-Blank : Plastic Dual In Line Package
 Suffix-J : Ceramic Dual In Line Package
 Suffix-D : Small Outline Package

Features

- Low Power consumption characteristic of CMOS devices
- Output drive capability: 10 LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts
for HCT 4.5 to 5.5 volts
- Low input current: $1\mu A$ Max.
- Low quiescent current: $80\mu A$ Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs

Function Table

OPERATING MODES	INPUTS						OUTPUTS					
	CLK	CLR	SH/LD	J	K	D_n	Q_0	Q_1	Q_2	Q_3	$\overline{Q_3}$	
asynchronous reset	L	X	X	X	X	X	L	L	L	L	H	
shift, set first stage	H	↑	h	h	h	X	H	q_0	q_1	q_2	$\overline{q_2}$	
shift, reset first stage	H	↑	h	l	l	X	L	q_0	q_1	q_2	$\overline{q_2}$	
shift, toggle first stage	H	↑	h	h	l	X	$\overline{q_0}$	q_0	q_1	q_2	$\overline{q_2}$	
shift, retain first stage	H	↑	h	l	h	X	q_0	q_0	q_1	q_2	$\overline{q_2}$	
parallel load	H	↑	l	X	X	d_n	d_0	d_1	d_2	d_3	$\overline{d_3}$	

H = HIGH voltage level

h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CLK transition

L = LOW voltage level

l = LOW voltage level one set-up time prior to the LOW-to-HIGH CLK transition

q, d = lower case letters indicate the state of the referenced input for output one set-up time prior to the LOW-to-HIGH CLK transition

X = don't care

↑ = LOW-to-HIGH CLK transition

Logic Diagram

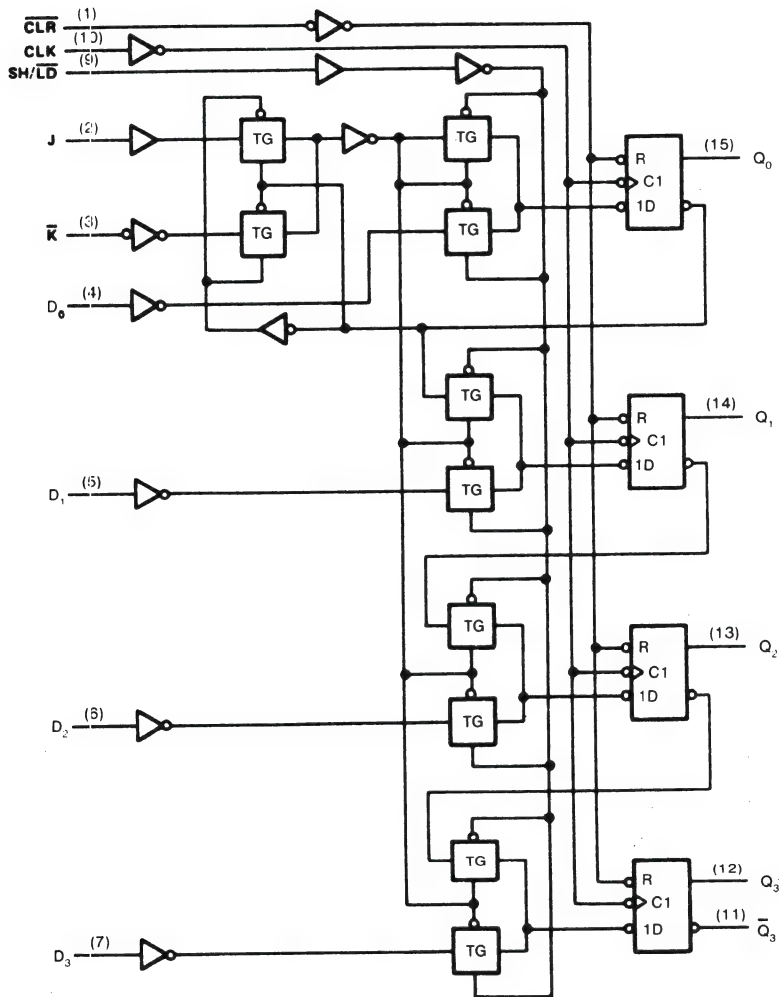


Fig. 1 Logic diagram

Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC Supply voltage		-0.5	+7	V
I_{IK}, I_{OK}	DC input or output diode current	for $V_I < -0.5$ or $V_I > V_{CC} + 0.5$ V		20	mA
I_O	DC output source or sink current	for -0.5 V $< V_O < V_{CC} + 0.5$ V		25	mA
I_{CC}	DC V_{CC} or GND current			50	mA
T_{stg}	Storage temperature range		-65	150	°C
P_D	Power dissipation per package	above +70°C: derate linearly with 8mW/K		500	mW
T_L	Lead temperature	At distance 1/16 ± 1/32 in. from case for 60 sec (CERAMIC) 10 sec (PLASTIC)		300 260	°C

Recommended Operating Conditions

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range V_{CC} : GD54/74HC Types GD54/74HCT Types	2 4.5	6 5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A : GD74 Types GD54 Types	-40 -55	+85 +125	°C
Input Rise and Fall times t_r, t_f : GD54/74HC Types at 2V at 4.5V at 6V GD54/74HCT Types at 4.5V		1000 500 400 500	ns

Typical Clear, Shift, and Load Sequences

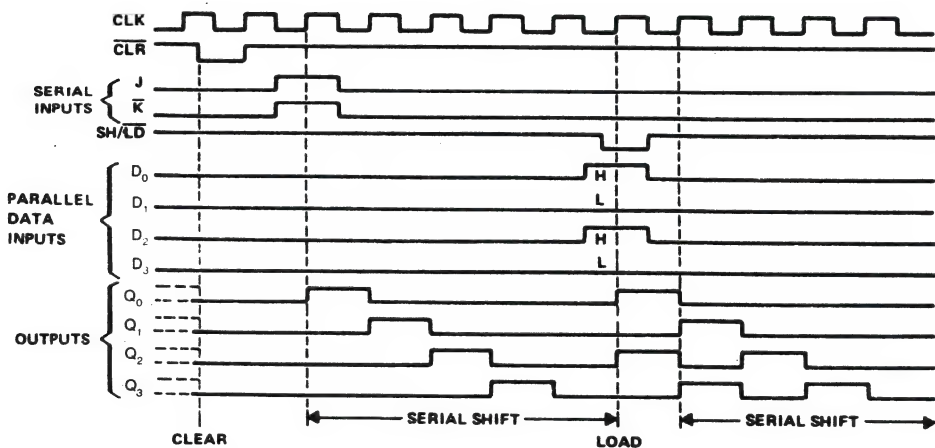


Fig. 2 Typical clear, shift, and load sequences

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION	V_{CC}	$T_A = 25^\circ\text{C}$			GD74HC195		GD54HC195		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V_{IH}	HIGH level input Voltage		2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2		1.5 3.15 4.2		V
V_{IL}	LOW level output voltage		2.0 4.5 6.0			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V
V_{OH}	HIGH level output voltage	$V_{IN} = V_{IH}$	$I_{OH} = -20\mu\text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0	1.9 4.4 5.9		1.9 4.4 5.9		V
			$I_{OH} = -4\text{mA}$	4.5 6.0	3.98 5.48	4.3 5.2	3.84 5.34		3.7 5.2		
		or V_{IL}	$I_{OH} = -5.2\text{mA}$	4.5 6.0	3.98 5.48	4.3 5.2	3.84 5.34		3.7 5.2		
V_{OL}	LOW level output voltage	$V_{IN} = V_{IH}$	$I_{OL} = 20\mu\text{A}$	2.0 4.5 6.0			0.1 0.1 0.1	0.1 0.1 0.1		0.1 0.1 0.1	V
			$I_{OL} = 4\text{mA}$	4.5 6.0		0.17 0.15	0.26 0.26	0.33 0.33		0.4 0.4	
		or V_{IL}	$I_{OL} = 5.2\text{mA}$	4.5 6.0		0.17 0.15	0.26 0.26	0.33 0.33		0.4 0.4	
$ I_{IN} $	Input leakage Current	$V_{IN} = V_{CC}$ or GND	6.0			0.1		1.0		1.0	μA
I_{CC}	Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND $I_{out} = 0\mu\text{A}$	6.0			8		80		160	μA

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION	V_{CC}	$T_A = 25^\circ\text{C}$			GD74HCT195		GD54HCT195		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V_{IH}	HIGH level input Voltage		4.5 to 5.5	2.0			2.0		2.0		V
V_{IL}	LOW level output voltage		4.5 to 5.5			0.8		0.8		0.8	V
V_{OH}	HIGH level output voltage	$V_{IN} = V_{IH}$	$I_{OH} = -20\mu\text{A}$	4.5	4.4	4.5	4.4		4.4		V
		or V_{IL}	$I_{OH} = -4\text{mA}$	4.5	3.98	4.3	3.84		3.7		
V_{OL}	LOW level output voltage	$V_{IN} = V_{IH}$	$I_{OL} = 20\mu\text{A}$	4.5			0.1		0.1		V
		or V_{IL}	$I_{OL} = 4\text{mA}$	4.5		0.17	0.26		0.33		
$ I_{IN} $	Input leakage Current	$V_{IN} = V_{CC}$ or GND	5.5			0.1		1.0		1.0	μA
I_{CC}	Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND $I_{out} = 0\mu\text{A}$	5.5			8		80		160	μA

Timing Requirements for HC: $t_r = t_f = 6\text{ns}$ $C_L = 50\text{ pF}$

SYMBOL	PARAMETER		V_{CC} (V)	$T_A = 25^\circ\text{C}$			GD74HC195		GD54HC195		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_w	Pulse width	$\overline{\text{CLR}}$ low, CLK	2.0	80			100		120		ns
			4.5	16			20		24		
			6.0	14			17		20		
t_{su}	Setup time	SH/ $\overline{\text{LD}}$, Dn, J, $\overline{\text{K}}$	2.0	80			100		120		ns
			4.5	16			20		24		
			6.0	12			17		20		
t_{rec}	Recovery time	$\overline{\text{CLR}}$ to CLK	2.0	80			100		120		ns
			4.5	16			20		24		
			6.0	12			17		20		
t_h	Hold time	SH/ $\overline{\text{LD}}$, Dn, J, $\overline{\text{K}}$ to CLK	2.0	0			0		0		ns
			4.5	0			0		0		
			6.0	0			0		0		

AC Characteristics for HC: $t_r = t_f = 6\text{ns}$ $C_L = 50\text{ pF}$

SYMBOL	PARAMETER		V_{CC} (V)	$T_A = 25^\circ\text{C}$			GD74HC195		GD54HC195		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
f_{max}	Maximum Clock Pulse Frequency		2.0	6			5		4.2		MHz
			4.5	31			25		21		
			6.0	36			29		25		
$t_{PLH}/$ t_{PHL}	Propagation Delay Time CLK to Qn, $\overline{\text{Qn}}$		2.0		50	145		180		220	ns
			4.5		17	29		36		44	
			6.0		13	25		31		36	
$t_{PLH}/$ t_{PHL}	Propagation Delay Time $\overline{\text{CLR}}$ to Qn, $\overline{\text{Qn}}$		2.0		41	140		175		210	ns
			4.5		15	28		35		42	
			6.0		12	24		30		35	
$t_{TLH}/$ t_{THL}	Output Transition Time		2.0		19	75		95		110	ns
			4.5		7	15		19		22	
			6.0		6	13		16		19	

Timing Requirements for HCT: $t_r = t_f = 6\text{ns}$ $C_L = 50\text{ pF}$

SYMBOL	PARAMETER		V_{CC} (V)	$T_A = 25^\circ\text{C}$			GD74HCT195		GD54HCT195		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_w	Pulse width	$\overline{\text{CLR}}$ low, CLK	4.5	16			20		24		ns
t_{su}	Setup time	SH/ $\overline{\text{LD}}$, Dn, J, $\overline{\text{K}}$	4.5	16			20		24		ns
t_{rec}	Recovery time	$\overline{\text{CLR}}$ to CLK	4.5	16			20		24		ns
t_h	Hold time	SH/ $\overline{\text{LD}}$, Dn, J, $\overline{\text{K}}$ to CLK	4.5	0			0		0		ns

AC Characteristics for HCT: $t_r = t_f = 6\text{ns}$ $C_L = 50\text{ pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A = 25^\circ\text{C}$			GD74HCT195		GD54HCT195		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
f_{max}	Maximum Clock Pulse Frequency	4.5	30			23		20		MHz
$t_{PLH}/$ t_{PHL}	Propagation Delay Time CLK to Q_n, \overline{Q}_n	4.5		19	32		40		48	ns
$t_{PLH}/$ t_{PHL}	Propagation Delay Time $\overline{\text{CLR}}$ to Q_n, \overline{Q}_n	4.5		16	31		40		46	ns
$t_{TLH}/$ t_{THL}	Output Transition Time	4.5		7	15		19		22	ns

AC Waveforms

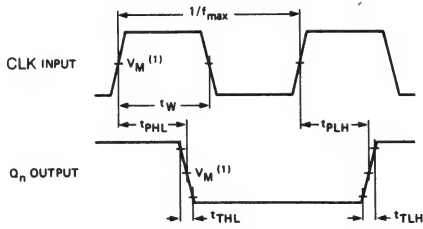


Fig. 3 Waveforms showing the clock (CLK) to output (Q_n) propagation delays, the clock pulse width, the output transition times and the maximum clock frequency.

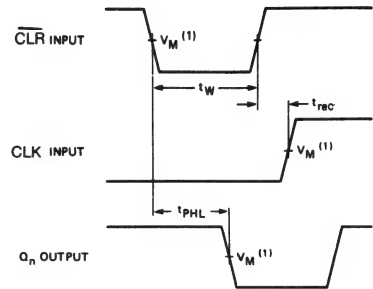


Fig. 4 Waveforms showing the master clear (\overline{CLR}) pulse width, the master clear to output (Q_n) propagation delays and the master clear to clock (CLK) recovery time

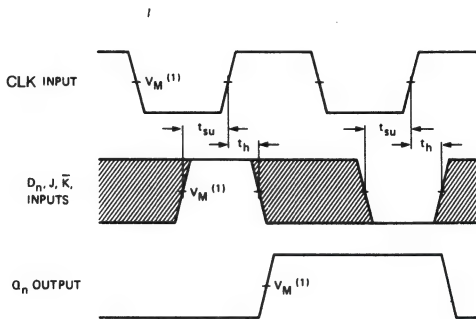


Fig. 5 Waveforms showing the data set-up and hold times for J, \overline{K} and D_n inputs.

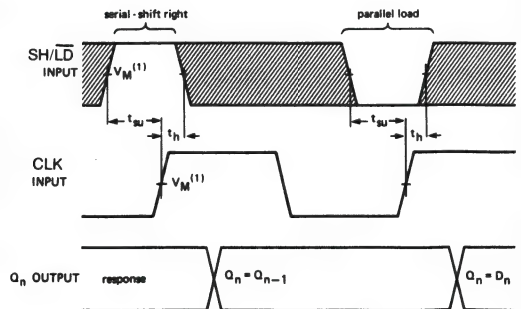


Fig. 6 Waveforms showing the set-up and hold times from the parallel enable input (SH/ \overline{LD}) to the clock (CLK).

Note to Figs. 5 and 6

The shaded areas indicate when the input is permitted to change for predictable output performance.

Note to AC waveforms

- (1) HC : $V_M = 50\%$; $V_I = GND$ to V_{CC} .
HCT : $V_M = 1.3V$; $V_I = GND$ to $3V$.

GD54/74HC221, GD54/74HCT221

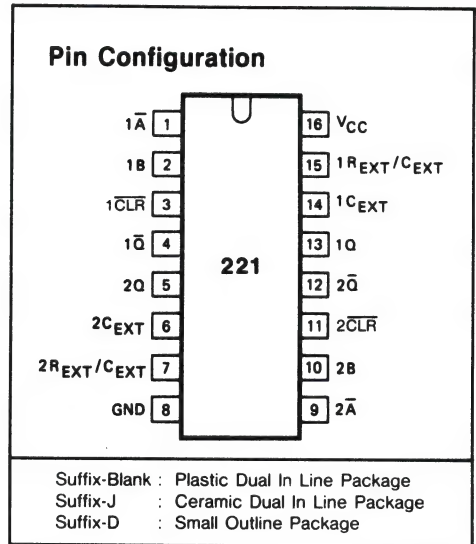
DUAL NON-RETRIGGERABLE MONOSTABLE MULTIVIBRATORS

General Description

These devices are identical in pinout to the 54/74LS221. They consist of two non-retriggerable monostable multivibrators. Each multivibrator features an active-low asynchronous clear and both negative- and positive-edge triggered inputs, either of which can be used as an enable. Also included is a clear input that when taken low resets the one shot. This circuit cannot be retriggered until the output times out. The output pulse width can be controlled with stability by the simple equation:

$$PW = (R_{EXT}) (C_{EXT})$$

Where PW is in seconds, R_{EXT} is in ohms, and C_{EXT} is in farads. Schmitt triggers circuitry is provided for B inputs. Refer to GD74 HC/HCT 123 and 423 for different functionalities. These devices are characterized for operation over wide temperature ranges to meet industry and military specifications.



Features

- Low Power consumption characteristic of CMOS devices
- Output drive capability: 10 LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts
for HCT 4.5 to 5.5 volts
- Low input current: 1μA Max.
- Low quiescent current: 80μA Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs

Function Table

INPUTS			OUTPUT	
\overline{nCLR}	$n\overline{A}$	nB	nQ	$n\overline{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑		
H	↓	H		
↑	L	H		

H = HIGH voltage level

L = LOW voltage level

X = don't care

↑ = LOW-to-HIGH transition

↓ = HIGH-to-LOW transition

= one HIGH-level output pulse

= one LOW-level output pulse

Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC Supply voltage		-0.5	+7	V
I_{IK}, I_{OK}	DC input or output diode current	for $V_I < -0.5$ or $V_I > V_{CC} + 0.5V$		20	mA
I_O	DC output source or sink current	for $-0.5V < V_O < V_{CC} + 0.5V$		25	mA
I_{CC}	DC V_{CC} or GND current			50	mA
T_{stg}	Storage temperature range		-65	150	°C
P_D	Power dissipation per package	above +70°C: derate linearly with 8mW/K		500	mW
T_L	Lead temperature	At distance 1/16 ± 1/32 in. from case for 60 sec(CERAMIC) 10 sec(PLASTIC)		300 260	°C

Recommended Operating Conditions

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range V_{CC} : GD54/74HC Types GD54/74HCT Types	2 4.5	6 5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A : GD74 Types GD54 Types	-40 -55	+85 +125	°C
Input Rise and Fall times t_r, t_f : GD54/74HC Types at 2V at 4.5V at 6V GD54/74HCT Types at 4.5V		1000 500 400 500	ns

Logic Diagram

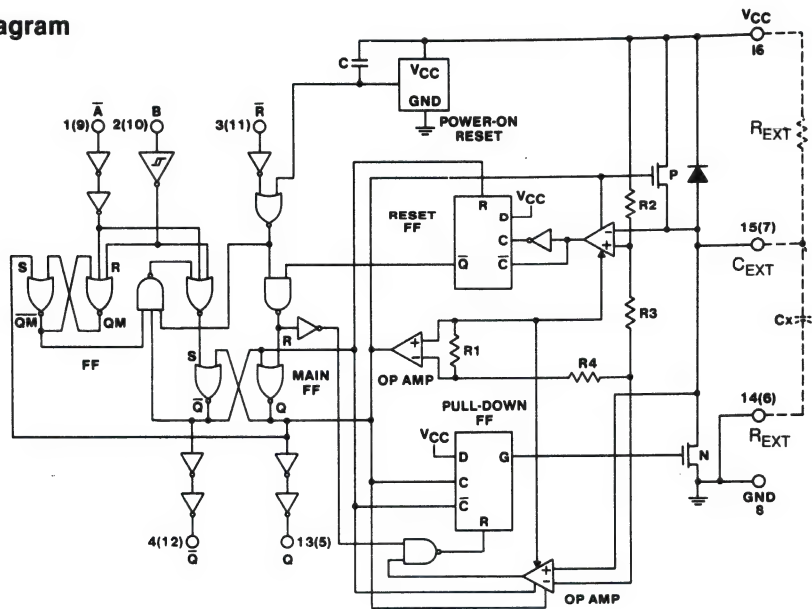


Fig. 1 Logic Diagram

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD54HC221		GD74HC22		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2		1.5 3.15 4.2		V
V _{IL}	LOW level input voltage		2.0 4.5 6.0			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH} or V _{IL}	I _{OH} =−20μA	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0	1.9 4.4 5.9		1.9 4.4 5.9		V
			I _{OH} =−4mA	4.5	3.98	4.3	3.84		3.7		
			I _{OH} =−5.2mA	6.0	5.48	5.2	5.34		5.2		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH} or V _{IL}	I _{OL} =20μA	2.0 4.5 6.0			0.1 0.1 0.1	0.1		0.1	V
			I _{OL} =4mA	4.5		0.17	0.26	0.33		0.4	
			I _{OL} =5.2mA	6.0		0.15	0.26	0.33		0.4	
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	6.0			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	6.0			8		80		160	μA

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HCT221		GD54HCT221		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		4.5 to 5.0	2.0			2.0		2.0		V
V _{IL}	LOW level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH} or V _{IL}	I _{OH} =−20μA	4.5	4.4	4.5	4.4		4.4		V
			I _{OH} =−4mA	4.5	3.98	4.3	3.84		3.7		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH} or V _{IL}	I _{OL} =20μA	4.5			0.1			0.1	V
			I _{OL} =4mA	4.5		0.17	0.26		0.33		
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	5.5			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	5.5			8		80		160	μA

Transfer Characteristic for HC

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HC221		GD54HC221		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{T+}	Positive-going threshold		2.0	0.7	1.2	1.5	0.7	1.5	0.7	1.5	V
			4.5	1.7	2.4	3.15	1.7	3.15	1.7	3.15	
			6.0	2.1	3.2	4.2	2.1	4.2	2.1	4.2	
V _{T-}	negative-going threshold		2.0	0.3	0.65	1.0	0.3	1.0	0.3	1.0	V
			4.5	0.9	1.7	2.2	0.9	2.2	0.9	2.2	
			6.0	1.2	2.1	3.0	1.2	3.0	1.2	3.0	
V _H	Hysteresis (V _{T+} -V _{T-})		2.0	0.2	0.6	1.0	0.2	1.0	0.2	1.0	V
			4.5	0.4	0.9	1.4	0.4	1.4	0.4	1.4	
			6.0	0.5	1.3	1.7	0.5	1.7	0.5	1.7	

Timing Requirements for HC: t_r=t_f=6ns C_L=50 pF

SYMBOL	PARAMETER		V _{CC} (V)	T _A =25°C			GD74HC221		GD54HC221		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t _w	Pulse width	Trigger n \overline{A} =low, nB=high Clear n \overline{CLR} =low	2.0	100			125		150		ns
			4.5	20			25		30		
			6.0	17			21		26		
		Output nQ=high, n \overline{Q} =low C _{EXT} =1000pF, R _{EXT} =10K Ω	4.5		7						μ s
			4.5		140						
		Output nQ=high, n \overline{Q} =low C _{EXT} =28pF, R _{EXT} =25K Ω	4.5								ns
			4.5		1.5						

AC Characteristics for HC: t_r=t_f=6ns C_L=50 pF

SYMBOL	PARAMETER	V _{CC} (V)	T _A =25°C			GD74HC221		GD54HC221		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t _{PHL}	Propagation Delay Time n \overline{CLR} , n \overline{A} , nB to nQ	2.0			240		290		340	ns
		4.5			44		58		68	
		6.0			38		49		58	
t _{PLH}	Propagation Delay Time n \overline{CLR} , n \overline{A} , nB to n \overline{Q}	2.0			200		240		290	ns
		4.5			36		48		58	
		6.0			31		41		48	
t _{PHL}	Propagation Delay Time n \overline{CLR} to nQ	2.0			200		250		305	ns
		4.5			38		51		61	
		6.0			34		42		52	
t _{PLH}	Propagation Delay Time n \overline{CLR} to n \overline{Q}	2.0			180		215		255	ns
		4.5			34		43		51	
		6.0			29		36		43	
t _{TLH} / t _{THL}	Output Transition Time	2.0		28	75		95		110	ns
		4.5		7	15		19		22	
		6.0		6	13		15		19	

Transfer Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HCT221		GD54HCT221		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{T+}	Positive-going threshold		4.5 5.5	1.2 1.4	1.55 1.75	1.9 2.1	1.2 1.4	1.9 2.1	1.2 1.4	1.9 2.1	V
V _{T-}	Negative-going threshold		4.5 5.5	0.5 0.6	0.85 1.0	1.2 1.4	0.5 0.6	1.2 1.4	0.5 0.6	1.2 1.4	V
V _H	Hysteresis (V _{T+} -V _{T-})		4.5 5.5	0.4 0.4	0.9 1.0	1.4 1.5	0.4 0.5	1.4 1.5	0.4 0.5	1.4 1.5	V

Timing Requirements for HCT, t_r=t_f=6ns C_L=50 pF

SYMBOL	PARAMETER		V _{CC} (V)	T _A =25°C			GD74HCT221		GD54HCT221		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t _w	Pulse width	Trigger n \overline{A} =low, nB=high Clear n \overline{CLR} =low	4.5	25			30		37		ns
		Output nQ=high, n \overline{Q} =low C _{EXT} =1000pF, R _{EXT} =2K Ω	4.5		7						μ s
		Output nQ=high, n \overline{Q} =low C _{EXT} =28pF, R _{EXT} =2K Ω	4.5		140						ns
		Output nQ=high, n \overline{Q} =low C _{EXT} =1000 F, R _{EXT} =5K Ω	4.5		1.5						μ s

AC Characteristics for HCT, t_r=t_f=6ns C_L=50 pF

SYMBOL	PARAMETER	V _{CC} (V)	T _A =25°C			GD74HCT221		GD54HCT221		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t _{PHL}	Propagation Delay Time n \overline{CLR} , n \overline{A} , nB to nQ	4.5			54		64		76	ns
t _{PLH}	Propagation Delay Time n \overline{CLR} , n \overline{A} , nB to n \overline{Q}	4.5			48		56		68	ns
t _{PHL}	Propagation Delay Time n \overline{CLR} to nQ	4.5			48		56		68	ns
t _{PLH}	Propagation Delay Time n \overline{CLR} to n \overline{Q}	4.5			48		56		68	ns
t _{TLH} / t _{THL}	Output Transition time	4.5		7	15		19		22	ns

AC Waveforms

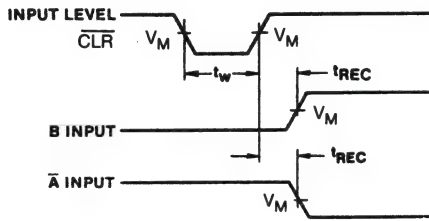


Fig. 2. Recovery times, $\overline{\text{CLR}}$ to A or B.

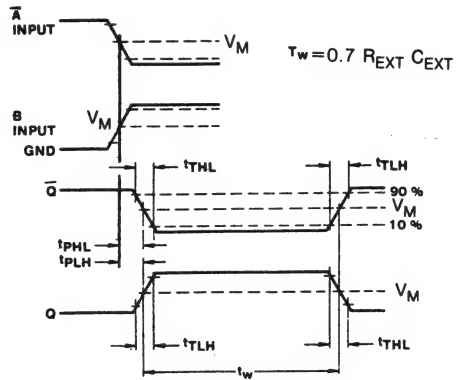


Fig. 3. Triggering of One Shot by input A or input B for a period t_w .

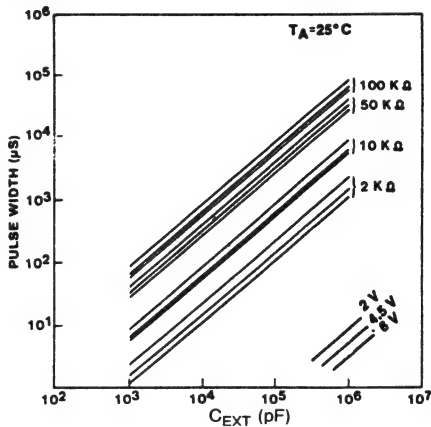


Fig. 4. Pulse width as a function of C_{EXT} for various values of R_{EXT} (2 KΩ to 100 KΩ) and V_{CC} (2V, 4.5V, 6V).

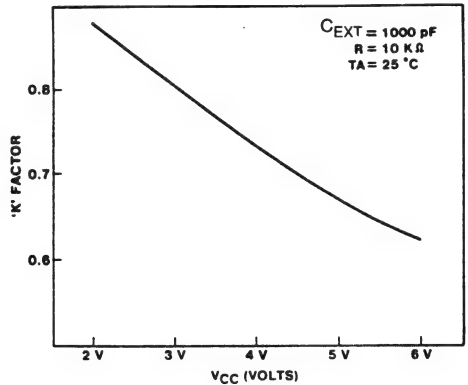


Fig. 5. K factor as a function of supply voltage [$T = K R_{\text{EXT}} C_{\text{EXT}}$]

Note to AC waveforms

- (1) HC : $V_M = 50\%$; $V_I = \text{GND to } V_{\text{CC}}$.
HCT : $V_M = 1.3\text{V}$; $V_I = \text{GND to } 3\text{V}$.

GD54/74HC240, GD54/74HCT240

OCTAL INVERTING 3-STATE BUFFERS

General Description

These devices are identical in pinout to the 54/74LS240. They contain eight inverting buffers with two active low enables. Each enable independently controls 4 buffers. These octal inverting buffers/line drivers/line receivers are designed to be used with 3-state memory address drivers, clock drivers, and other bus-oriented systems. Refer to the other devices for similar functionality:

HC/HCT 241 Noninverting, active-low & active-high enables.

HC/HCT 244 Noninverting, active-low enables. These devices are characterized for operation over wide temperature ranges to meet industry and military specifications.

Features

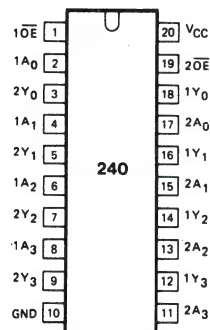
- Low Power consumption characteristic of CMOS devices
- Output drive capability: 15 LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts
for HCT 4.5 to 5.5 volts
- Low input current: $1\mu\text{A}$ Max.
- Low quiescent current: $80\mu\text{A}$ Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs

Function Table

INPUTS		OUTPUT
\overline{nOE}	nA_n	nY_n
L	L	H
L	H	L
H	X	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

Pin Configuration



Suffix-Blank : Plastic Dual In Line Package
 Suffix-J : Ceramic Dual In Line Package
 Suffix-D : Small Outline Package

Logic Diagram

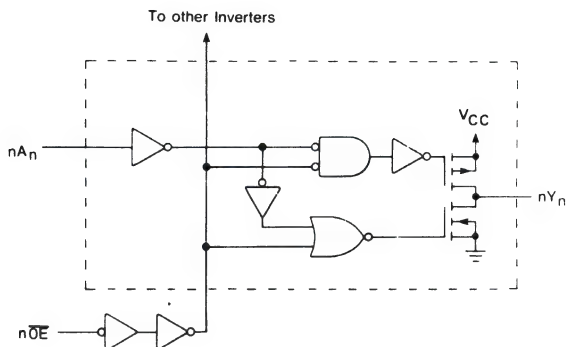


Fig. 1 Logic diagram (one gate)

Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC Supply voltage		-0.5	+7	V
I_{IK}, I_{OK}	DC input or output diode current	for $V_I < -0.5$ or $V_I > V_{CC} + 0.5V$		20	mA
I_O	DC output source or sink current	for $-0.5V < V_O < V_{CC} + 0.5V$		35	mA
I_{CC}	DC V_{CC} or GND current			70	mA
T_{stg}	Storage temperature range		-65	150	°C
P_D	Power dissipation per package	above +70°C: derate linearly with 8mW/K		500	mW
T_L	Lead temperature	At distance $1/16 \pm 1/32$ in. from case for 60 sec(CERAMIC) 10 sec(PLASTIC)		300 260	°C

Recommended Operating Conditions

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range V_{CC} : GD54/74HC Types GD54/74HCT Types	2 4.5	6 5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A : GD74 Types GD54 Types	-40 -55	+85 +125	°C
Input Rise and Fall times t_r, t_f : GD54/74HC Types at 2V at 4.5V at 6V GD54/74HCT Types at 4.5V		1000 500 400 500	ns

Logic Diagram

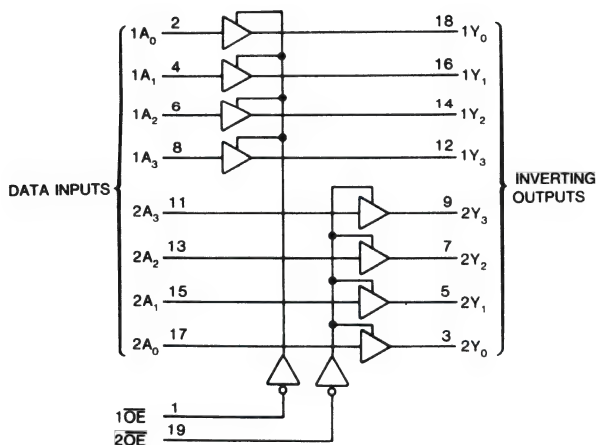


Fig. 2 Logic diagram

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A = 25°C			GD74HC240		GD54HC240		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{IH}	HIGH level input Voltage		2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2		1.5 3.15 4.2		V
V _{IL}	LOW level input voltage		2.0 4.5 6.0			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V
V _{OH}	HIGH level output voltage	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -20μA	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0	1.9 4.4 5.9		1.9 4.4 5.9		V
				I _{OH} = -6mA I _{OH} = -7.8mA	4.5 6.0	3.98 5.48	4.3	3.84 5.34	3.7 5.2		
			I _{OL} = 20μA	2.0 4.5 6.0			0.1 0.1 0.1		0.1 0.1 0.1		V
				I _{OL} = 6mA I _{OL} = 7.8mA	4.5 6.0	0.17 0.15	0.26 0.26	0.33 0.33	0.4 0.4		
I _{IN}	Input leakage Current	V _{IN} = V _{CC} or GND	6.0			0.1		1.0		1.0	μA
I _{OZ}	Three-State leakage current	V _{IN} = V _{IH} or V _{IL} V _O = V _{CC} or GND	6.0		0.01	0.5		5.0		10.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} = V _{CC} or GND I _{out} = 0μA	6.0			8		80		160	μA

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A = 25°C			GD74HCT240		GD54HCT240		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{IH}	HIGH level input Voltage		4.5 to 5.0	2.0			2.0		2.0		V
V _{IL}	LOW level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V _{OH}	HIGH level output voltage	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -20μA	4.5	4.4	4.5	4.4		4.4		V
			I _{OH} = -6mA	4.5	3.98	4.3	3.84		3.7		
V _{OL}	LOW level output voltage	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 20μA	4.5		0.1		0.1		0.1	V
			I _{OL} = 6mA	4.5		0.17	0.26	0.33		0.4	
I _{IN}	Input leakage Current	V _{IN} = V _{CC} or GND	5.5			0.1		1.0		1.0	μA
I _{OZ}	Three-State leakage current	V _{IN} = V _{IH} or V _{IL} V _O = V _{CC} or GND	5.5		0.01	0.5		5.0		10.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} = V _{CC} or GND I _{out} = 0μA	5.5			8		80		160	μA

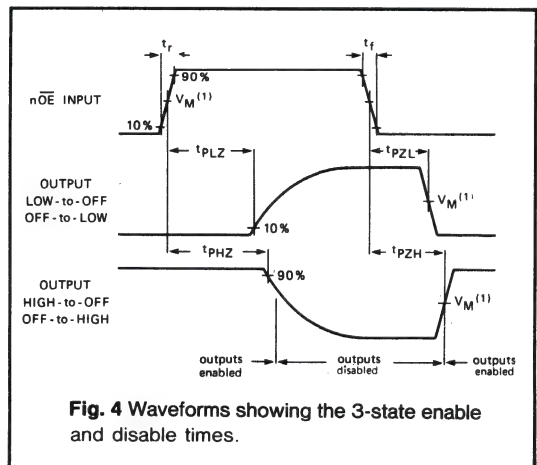
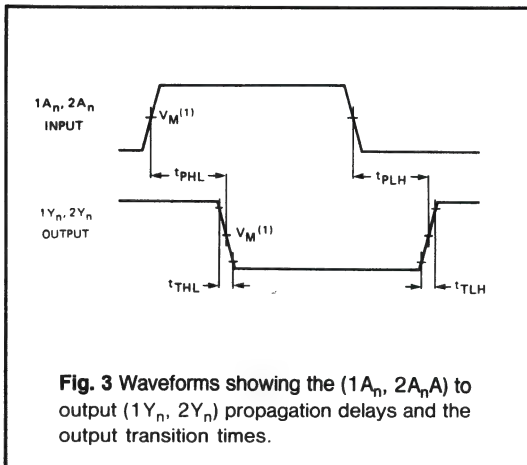
AC Characteristics for HC: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HC240		GD54HC240		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} / t_{PHL}	Propagation Delay Time nA_n to nY_n	2.0 4.5 6.0		30 9 8	100 18 16		120 24 20		140 28 25	ns
t_{PZH} / t_{PZL}	3-state Output Enable Time $n\overline{OE}$ to nY_n	2.0 4.5 6.0		36 12 10	140 28 26		180 36 32		210 42 36	ns
t_{PLZ} / t_{PHZ}	3-state Output Disable Time $n\overline{OE}$ to nY_n	2.0 4.5 6.0		35 10 9	140 28 26		180 36 32		210 42 36	ns
t_{TLH} / t_{THL}	Output Transition Time	2.0 4.5 6.0		15 6 5	60 12 10		75 15 13		90 18 15	ns

AC Characteristics for HC: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HCT240		GD54HCT240		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} / t_{PHL}	Propagation Delay Time nA_n to nY_n	4.5		12	22		26		30	ns
t_{PZH} / t_{PZL}	3-state Output Enable Time $n\overline{OE}$ to nY_n	4.5		18	30		38		45	ns
t_{PLZ} / t_{PHZ}	3-state Output Disable Time $n\overline{OE}$ to nY_n	4.5		15	25		32		38	ns
t_{TLH} / t_{THL}	Output Transition Time	4.5		7	12		15		18	ns

AC Waveforms



GD54/74HC241, GD54/74HCT241

OCTAL NONINVERTING 3-STATE BUFFERS

General Description

These devices are identical in pinout to the 54/74LS241. They contain eight noninverting buffers with one active-low and one active-high enable. Each enable independently controls 4 buffers. These octal noninverting buffers/line drivers/line receivers are designed to be used with 3-state memory address drivers, clock drivers, and other bus-oriented systems. Refer to the other devices for similar functionality:

HC/HCT 240 Inverting, active-low enables

HC/HCT 244 Noninverting, active-low enables

These devices are characterized for operation over wide temperature ranges to meet industry and military specifications.

Features

- Low Power consumption characteristic of CMOS devices
- Output drive capability: 15 LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts
for HCT 4.5 to 5.5 volts
- Low input current: $1\mu\text{A}$ Max.
- Low quiescent current: $80\mu\text{A}$ Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs

Function Table

INPUTS		OUTPUT
$1\overline{\text{OE}}$	1A_n	1Y_n
L	L	L
L	H	H
H	X	Z

INPUTS		OUTPUT
2OE	2A_n	2Y_n
H	L	L
H	H	H
L	X	Z

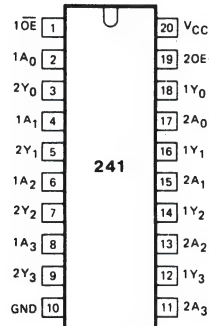
H = HIGH voltage level

L = LOW voltage level

X = don't care

Z = high impedance OFF-state

Pin Configuration



Suffix-Blank : Plastic Dual In Line Package
 Suffix-J : Ceramic Dual In Line Package
 Suffix-D : Small Outline Package

Logic Diagram

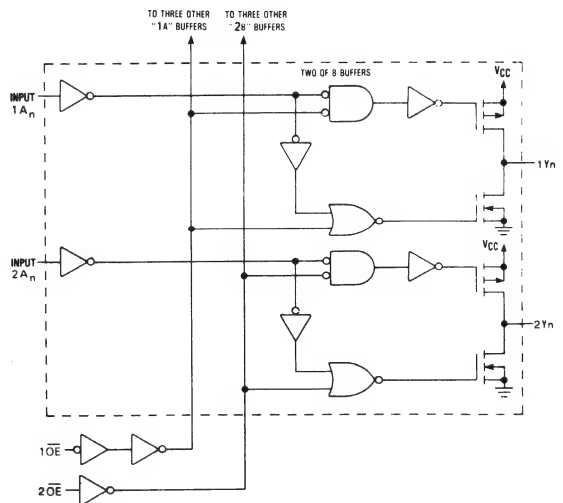


Fig. 1 Logic diagram

Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC Supply voltage		-0.5	+7	V
I_{IK}, I_{OK}	DC input or output diode current	for $V_I < -0.5$ or $V_I > V_{CC} + 0.5V$		20	mA
I_O	DC output source or sink current	for $-0.5V < V_O < V_{CC} + 0.5V$		35	mA
I_{CC}	DC V_{CC} or GND current			70	mA
T_{stg}	Storage temperature range		-65	150	°C
P_D	Power dissipation per package	above +70°C: derate linearly with 8mW/K		500	mW
T_L	Lead temperature	At distance 1/16 ± 1/32 in. from case for 60 sec(CERAMIC) 10 sec(PLASTIC)		300 260	°C

Recommended Operating Conditions

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range V_{CC} : GD54/74HC Types GD54/74HCT Types	2 4.5	6 5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A : GD74 Types GD54 Types	-40 -55	+85 +125	°C
Input Rise and Fall times t_r, t_f : GD54/74HC Types at 2V at 4.5V at 6V GD54/74HCT Types at 4.5 V		1000 500 400 500	ns

Logic Diagram

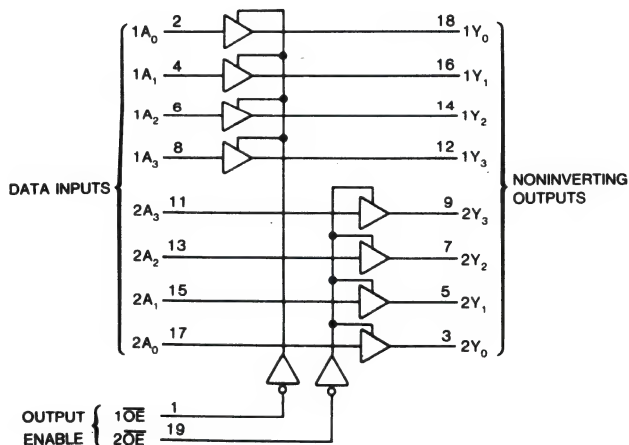


Fig. 2 Logic diagram

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A = 25°C			GD74HC241		GD54HC241		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2		1.5 3.15 4.2		V
V _{IL}	LOW level input voltage		2.0 4.5 6.0			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V
V _{OH}	HIGH level output voltage	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -20μA	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0	1.9 4.4 5.9		1.9 4.4 5.9		V
				I _{OH} = -6mA I _{OH} = -7.8mA	4.5 6.0	3.98 5.48	4.3 5.2	3.84 5.34	3.7 5.2		
			I _{OL} = 20μA	2.0 4.5 6.0			0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1		
			I _{OL} = 6mA I _{OL} = 7.8mA	4.5 6.0	0.17 0.15	0.26 0.26	0.33 0.33	0.33 0.33	0.4 0.4		
I _{IN}	Input leakage Current	V _{IN} = V _{CC} or GND	6.0			0.1		1.0		1.0	μA
I _{OZ}	Three-State leakage current	V _{IN} = V _{IH} or V _{IL} V _O = V _{CC} or GND	6.0		0.01	0.5		5.0		10.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} = V _{CC} or GND I _{out} = 0μA	6.0			8		80		160	μA

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A = 25°C			GD74HCT241		GD54HCT241		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		4.5 to 5.0	2.0			2.0		2.0		V
V _{IL}	LOW level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V _{OH}	HIGH level output voltage	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -20μA	4.5	4.4	4.5	4.4		4.4		V
			I _{OH} = -6mA	4.5	3.98	4.3	3.84		3.7		
V _{OL}	LOW level output voltage	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 20μA	4.5		0.1	0.1		0.1		V
			I _{OL} = 6mA	4.5	0.17	0.26	0.33		0.4		
I _{IN}	Input leakage Current	V _{IN} = V _{CC} or GND	5.5			0.1		1.0		1.0	μA
I _{OZ}	Three-State leakage current	V _{IN} = V _{IH} or V _{IL} V _O = V _{CC} or GND	5.5		0.01	0.5		5.0		10.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} = V _{CC} or GND I _{out} = 0μA	5.5			8		80		160	μA

AC Characteristics for HC: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HC241		GD54HC241		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
$t_{PLH}/$ t_{PHL}	Propagation Delay Time nA_n to nY_n	2.0 4.5 6.0		30 9 8	100 18 16		120 24 20		140 28 25	ns
$t_{PZH} /$ t_{PZL}	3-state Output Enable Time $1\overline{OE}$, $2OE$ to nY_n	2.0 4.5 6.0		35 10 9	140 28 26		180 36 32		210 42 36	ns
$t_{PLZ} /$ t_{PHZ}	3-state Output Disable Time $1\overline{OE}$, $2OE$ to nY_n	2.0 4.5 6.0		35 10 9	140 28 26		180 36 32		210 42 36	ns
$t_{TLH} /$ t_{THL}	Output Transition Time	2.0 4.5 6.0		15 6 5	60 12 10		75 15 13		90 18 15	ns

AC Characteristics for HCT: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HCT241		GD54HCT241		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
$t_{PLH}/$ t_{PHL}	Propagation Delay Time nA_n to nY_n	4.5		12	22		26		30	ns
$t_{PZH} /$ t_{PZL}	3-state Output Enable time $1\overline{OE}$, $2OE$ to nY_n	4.5		18	30		38		45	ns
$t_{PLZ} /$ t_{PHZ}	3-state Output Disable Time $1\overline{OE}$, $2OE$ to nY_n	4.5		15	25		32		38	ns
$t_{TLH} /$ t_{THL}	Output Transition Time	4.5		7	12		15		18	ns

AC Waveforms

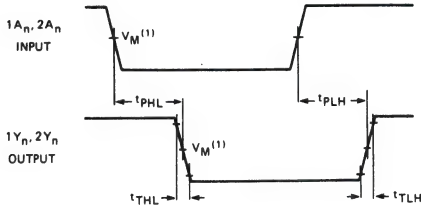


Fig. 3 Waveforms showing the ($1A_n$, $2A_n$) to output ($1Y_n$, $2Y_n$) propagation delays and the output transition times.

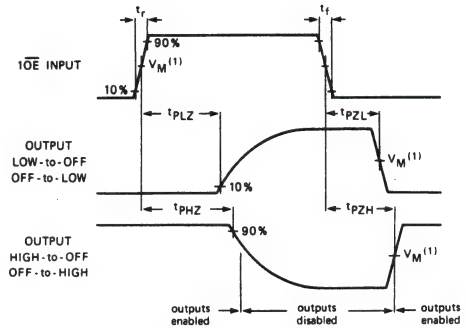


Fig. 4 Waveform showing the 3-state enable and disable times for input $1\overline{OE}$.

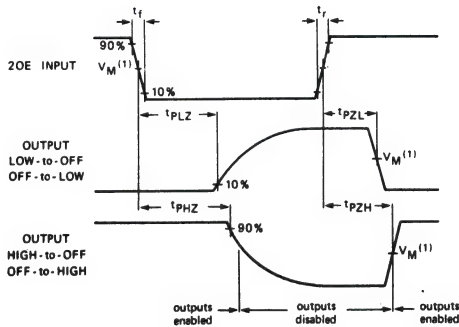


Fig. 5 Waveform showing the 3-state enable and disable times for input $2OE$.

Note to AC waveforms

- (1) HC : $V_M=50\%$; $V_I=GND$ to V_{CC} ;
HCT : $V_M=1.3V$; $V_I=GND$ to $3V$.

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Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC Supply voltage		-0.5	+7	V
I_{IK}, I_{OK}	DC input or output diode current	for $V_I < -0.5$ or $V_I > V_{CC} + 0.5V$		20	mA
I_O	DC output source or sink current	for $-0.5V < V_O < V_{CC} + 0.5V$		35	mA
I_{CC}	DC V_{CC} or GND current			70	mA
T_{stg}	Storage temperature range		-65	150	°C
P_D	Power dissipation per package	above +70°C: derate linearly with 8mW/K		500	mW
T_L	Lead temperature	At distance 1/16 ± 1/32 in. from case for 60 sec(CERAMIC) 10 sec(PLASTIC)		300 260	°C

Recommended Operating Conditions

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range V_{CC} : GD54/74HC Types GD54/74HCT Types	2 4.5	6 5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A : GD74 Types GD54 Types	-40 -55	+85 +125	°C
Input Rise and Fall times t_r, t_f : GD54/74HC Types at 2V at 4.5V at 6V GD54/74HCT Types at 4.5V		1000 500 400 500	ns

Logic Diagram

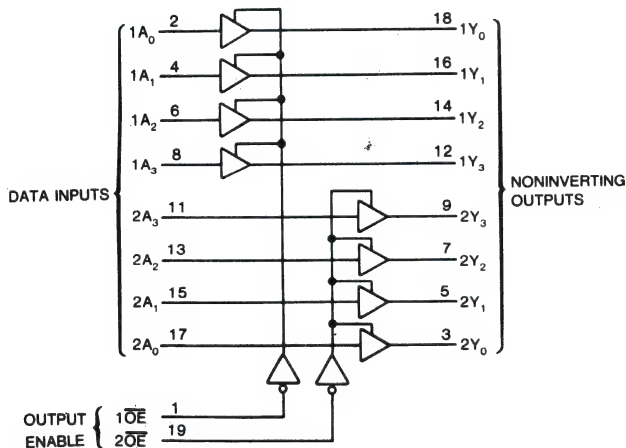


Fig. 2 Logic diagram

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION	V_{CC} (V)	$T_A = 25^\circ\text{C}$			GD74HC244		GD54HC244		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V_{IH}	HIGH level input Voltage		2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2		1.5 3.15 4.2		V
V_{IL}	LOW level input voltage		2.0 4.5 6.0			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V
V_{OH}	HIGH level output voltage	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -20\mu\text{A}$	2.0	1.9	2.0					V
				4.5	4.4	4.5	4.4		4.4		
			$I_{OH} = -6\text{mA}$ $I_{OH} = -7.8\text{mA}$	6.0	5.9	6.0	5.9		5.9		
				4.5	3.98	4.3	3.84		3.7		
V_{OL}	LOW level output voltage	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 20\mu\text{A}$	2.0			0.1	0.1		0.1	V
				4.5			0.1	0.1		0.1	
			$I_{OL} = 6\text{mA}$ $I_{OL} = 7.8\text{mA}$	6.0			0.1	0.1		0.1	
				4.5		0.17	0.26	0.33		0.4	
				6.0		0.15	0.26	0.33		0.4	
$ I_{IN} $	Input leakage Current	$V_{IN} = V_{CC}$ or GND	6.0			0.1		1.0		1.0	μA
I_{OZ}	Three-State leakage current	$V_{IN} = V_{IH}$ or V_{IL} $V_O = V_{CC}$ or GND	6.0		0.01	0.5		5.0		10.0	μA
I_{CC}	Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND $I_{out} = 0\mu\text{A}$	6.0			8		80		160	μA

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION	V_{CC} (V)	$T_A = 25^\circ\text{C}$			GD74HCT244		GD54HCT244		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V_{IH}	HIGH level input Voltage		4.5 to 5.0	2.0			2.0		2.0		V
V_{IL}	LOW level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V_{OH}	HIGH level output voltage	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -20\mu\text{A}$	4.5	4.4	4.5	4.4		4.4		V
			$I_{OH} = -6\text{mA}$	4.5	3.98	4.3	3.84		3.7		
V_{OL}	LOW level output voltage	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 20\mu\text{A}$	4.5			0.1	0.1		0.1	V
			$I_{OL} = 6\text{mA}$	4.5		0.17	0.26	0.33		0.4	
$ I_{IN} $	Input leakage Current	$V_{IN} = V_{CC}$ or GND	5.5			0.1		1.0		1.0	μA
I_{OZ}	Three-State leakage current	$V_{IN} = V_{IH}$ or V_{IL} $V_O = V_{CC}$ or GND	5.5		0.01	0.5		5.0		10.0	μA
I_{CC}	Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND $I_{out} = 0\mu\text{A}$	5.5			8		80		160	μA

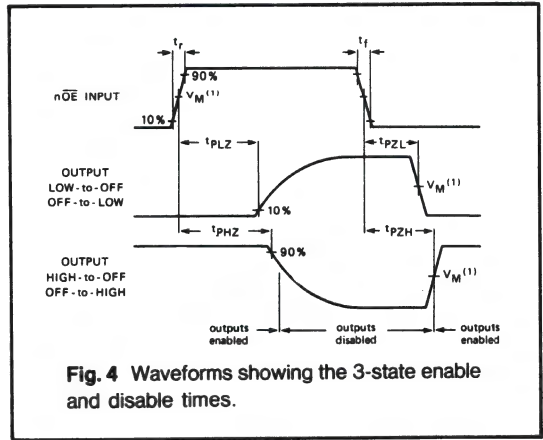
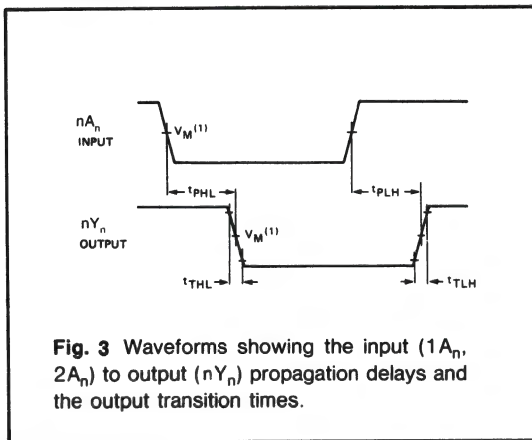
AC Characteristics for HC: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HC244		GD54HC244		UNIT*
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} / t_{PHL}	Propagation Delay Time nA_n to nY_n	2.0 4.5 6.0		30 9 8	100 18 16		120 24 20		140 28 25	ns
t_{PZH} / t_{PZL}	3-state Output Enable Time $n\overline{OE}$ to nY_n	2.0 4.5 6.0		35 10 9	140 28 26		180 36 32		210 42 36	ns
t_{PLZ} / t_{PHZ}	3-state Output Disable Time $n\overline{OE}$ to nY_n	2.0 4.5 6.0		35 10 9	140 28 26		180 36 32		210 42 36	ns
t_{TLH} / t_{THL}	Output Transition Time	2.0 4.5 6.0		15 6 5	60 12 10		75 15 13		90 18 15	ns

AC Characteristics for HCT: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HCT244		GD54HCT244		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{max}	Propagation Delay Time nA_n to nY_n	4.5		12	22		26		30	ns
t_{PLH} / t_{PHL}	Propagation Delay Time $n\overline{OE}$ to nY_n	4.5		18	30		38		45	ns
t_{PLH} / t_{PHL}	Propagation Delay Time $n\overline{OE}$ to nY_n	4.5		15	25		32		38	ns
t_{TLH} / t_{THL}	Output Transition Time	4.5		7	12		15		18	ns

AC Waveforms



GD54/74HC245, GD54/74HCT245

OCTAL NONINVERTING 3-STATE TRANSCEIVERS

General Description

These Devices are identical in pinout to the 54/74LS245. They consist of eight transceivers which are designed for asynchronous two-way communications between data buses. Each device has noninverting outputs, and has an active-low output enable which is used to place the I/O ports into high-impedance states. The direction control determines the directions of data flow. When it is high, data flow from A to B; When it is low, data flow from B to A. Refer to the other devices from similar functionalities;

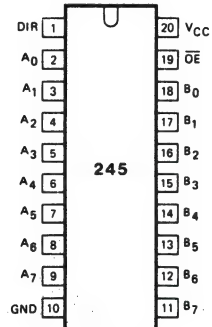
The HC/HCT 640 All Inverting outputs

The HC/HCT 643 4 Inverting &

4 Noninverting outputs.

These devices are characterized for operation over wide temperature ranges to meet industry and military specifications.

Pin Configuration



Suffix-Blank : Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package
Suffix-D : Small Outline Package

Features

- Low Power consumption characteristic of CMOS devices
- Output drive capability 15 LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts
for HCT 4.5 to 5.5 volts
- Low input current: 1 μ A Max.
- Low quiescent current: 80 μ A Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs

Function Table

INPUTS		INPUTS/OUTPUTS	
\overline{OE}	DIR	A _n	B _n
L	L	A=B	inputs
L	H	inputs	B=A
H	X	Z	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC Supply voltage		-0.5	+7	V
I_{IK}, I_{OK}	DC input or output diode current	for $V_I < -0.5$ or $V_I > V_{CC} + 0.5V$		20	mA
I_O	DC output source or sink current	for $-0.5V < V_O < V_{CC} + 0.5V$		35	mA
I_{CC}	DC V_{CC} or GND current			70	mA
T_{stg}	Storage temperature range		-65	150	°C
P_D	Power dissipation per package	above +70°C: derate linearly with 8mW/K		500	mW
T_L	Lead temperature	At distance $1/16 \pm 1/32$ in. from case for 60 sec(CERAMIC) 10 sec(PLASTIC)		300 260	°C

Recommended Operating Conditions

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range V_{CC} : GD54/74HC Types GD54/74HCT Types	2 4.5	6 5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A : GD74 Types GD54 Types	-40 -55	+85 +125	°C
Input Rise and Fall times t_r, t_f : GD54/74HC Types at 2V at 4.5V at 6V GD54/74HCT Types at 4.5V		1000 500 400 500	ns

Logic Diagram

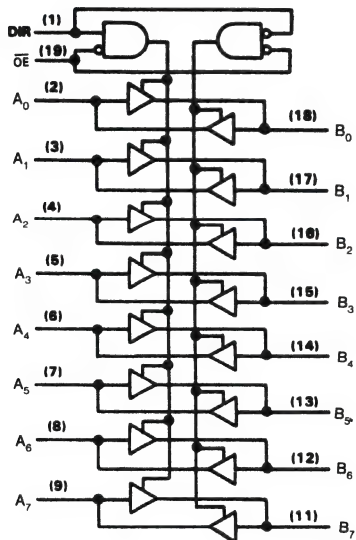


Fig. 1. Logic diagram

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION	V_{CC} (V)	$T_A = 25^\circ\text{C}$			GD74HC245		GD54HC245		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V_{IH}	HIGH level input Voltage		2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2		1.5 3.15 4.2		V
V_{IL}	LOW level input voltage		2.0 4.5 6.0			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V
V_{OH}	HIGH level output voltage	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -20\mu\text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0	1.9 4.4 5.9		1.9 4.4 5.9		V
			$I_{OH} = -6\text{mA}$	4.5 6.0	3.98 5.48	4.3 5.2	3.84 5.34		3.7 5.2		
			$I_{OH} = -7.8\text{mA}$	6.0							
V_{OL}	LOW level output voltage	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 20\mu\text{A}$	2.0 4.5 6.0			0.1 0.1 0.1		0.1 0.1 0.1		V
			$I_{OL} = 6\text{mA}$	4.5 6.0		0.17 0.15	0.26 0.26		0.33 0.33		
			$I_{OL} = 7.8\text{mA}$	6.0					0.4 0.4		
$ I_{IN} $	Input leakage Current	$V_{IN} = V_{CC}$ or GND	6.0			0.1		1.0		1.0	μA
I_{OZ}	Three-State leakage current	$V_{IN} = V_{IH}$ or V_{IL} $V_O = V_{CC}$ or GND	6.0		0.01	0.5		5.0		10.0	μA
I_{CC}	Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND $I_{out} = 0\mu\text{A}$	6.0			8		80		160	μA

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION	V_{CC} (V)	$T_A = 25^\circ\text{C}$			GD74HCT245		GD54HCT245		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V_{IH}	HIGH level input Voltage		4.5 to 5.0	2.0			2.0		2.0		V
V_{IL}	LOW level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V_{OH}	HIGH level output voltage	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -20\mu\text{A}$	4.5	4.4	4.5	4.4		4.4		V
			$I_{OH} = -6\text{mA}$	4.5	3.98	4.3	3.84		3.7		
V_{OL}	LOW level output voltage	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 20\mu\text{A}$	4.5			0.1		0.1		V
			$I_{OL} = 6\text{mA}$	4.5		0.17	0.26		0.33		
$ I_{IN} $	Input leakage Current	$V_{IN} = V_{CC}$ or GND	5.5			0.1		1.0		1.0	μA
I_{OZ}	Three-State leakage current	$V_{IN} = V_{IH}$ or V_{IL} $V_O = V_{CC}$ or GND	5.5		0.01	0.5		5.0		10.0	μA
I_{CC}	Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND $I_{out} = 0\mu\text{A}$	5.5			8		80		160	μA

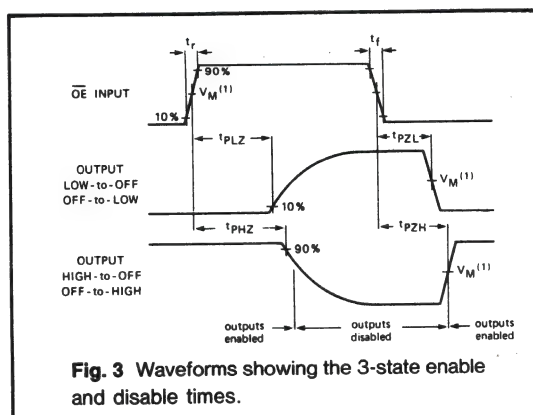
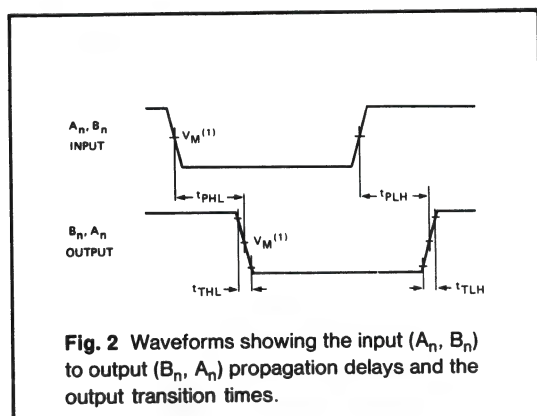
AC Characteristics for HC: $t_r = t_f = 6\text{ns}$ $C_L = 50\text{ pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A = 25^\circ\text{C}$			GD74HC245		GD54HC245		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} / t_{PHL}	Propagation Delay Time An to Bn, Bn to An	2.0 4.5 6.0		25 9 7	90 18 15		115 23 20		135 27 23	ns
t_{PLZ} / t_{PHZ}	3-state Output Enable Time \overline{OE} to An or Bn	2.0 4.5 6.0		30 11 9	150 30 26		190 38 33		225 45 38	ns
t_{PZH} / t_{PZL}	3-state Output Disable Time \overline{OE} to An or Bn	2.0 4.5 6.0		41 15 12	150 30 26		190 38 32		225 45 33	ns
t_{TLH} / t_{THL}	Output Transition Time	2.0 4.5 6.0		14 7 6	60 12 10		75 15 13		90 18 15	ns

AC Characteristics for HCT: $t_r = t_f = 6\text{ns}$ $C_L = 50\text{ pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A = 25^\circ\text{C}$			GD74HCT245		GD54HCT245		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} / t_{PHL}	Propagation Delay Time An to Bn, Bn to An	4.5		13	25		29		35	ns
t_{PZH} / t_{PZL}	3-state Output Enable Time \overline{OE} to An or Bn	4.5		16	32		38		45	ns
t_{PLZ} / t_{PHZ}	3-state Output Disable Time \overline{OE} to An or Bn	4.5		15	32		38		45	ns
t_{TLH} / t_{THL}	Output Transition Time	4.5		7	12		15		18	ns

AC Waveforms



GD54/74HC251, GD54/74HCT251

8-TO-1 LINE DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUTS

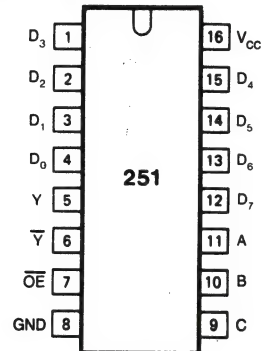
General Description

These devices are identical in pinout to the 54/74LS251. This circuit selects one of the 8 binary data inputs, depending on the address presented on the A, B, and C inputs. It features both true(Y) and complementary (\bar{Y}) outputs. The enable input must be at a low logic level to enable this multiplexing. A high logic level at the enable forces the Y and \bar{Y} outputs the high impedance state. The HC/HCT 251 are similar in function to the HC/HCT 151 which do not have 3-state outputs. These devices are characterized for operation over wide temperature ranges to meet industry and military specifications.

Features

- Low Power consumption characteristic of CMOS devices
- Output drive capability: 15 LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts
for HCT 4.5 to 5.5 volts
- Low input current: 1 μ A Max.
- Low quiescent current: 80 μ A Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs

Pin Configuration



Suffix-Blank : Plastic Dual In Line Package
 Suffix-J : Ceramic Dual In Line Package
 Suffix-D : Small Outline Package

INPUTS												OUTPUTS	
\overline{OE}	C	B	A	D ₀	D ₁	D ₂	D ₃	D ₄	D ₅	D ₆	D ₇	\bar{Y}	Y
H	X	X	X	X	X	X	X	X	X	X	X	Z	Z
L	L	L	L	L	X	X	X	X	X	X	X	H	L
L	L	L	L	H	X	X	X	X	X	X	X	L	H
L	L	L	H	X	L	X	X	X	X	X	X	H	L
L	L	L	H	X	H	X	X	X	X	X	X	L	H
L	L	H	L	X	X	L	X	X	X	X	X	H	L
L	L	H	L	X	X	H	X	X	X	X	X	L	H
L	L	H	H	X	X	X	L	X	X	X	X	H	L
L	L	H	H	X	X	X	X	X	X	X	X	L	H
L	L	H	H	X	X	X	H	X	X	X	X	H	L
L	L	H	H	X	X	X	X	X	X	X	X	L	H
L	L	H	H	X	X	X	X	X	X	X	X	H	L
L	L	H	H	X	X	X	X	X	X	X	X	L	H
L	L	H	H	X	X	X	X	X	X	X	X	H	L
L	L	H	H	X	X	X	X	X	X	X	X	L	H

H = HIGH voltage level
 L = LOW voltage level
 X = don't care
 Z = high impedance OFF-state

Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC Supply voltage		-0.5	+7	V
I_{IK}, I_{OK}	DC input or output diode current	for $V_I < -0.5$ or $V_I > V_{CC} + 0.5V$		20	mA
I_O	DC output source or sink current	for $-0.5V < V_O < V_{CC} + 0.5V$		35	mA
I_{CC}	DC V_{CC} or GND current			70	mA
T_{stg}	Storage temperature range		-65	150	°C
P_D	Power dissipation per package	above +70°C: derate linearly with 8mW/K		500	mW
T_L	Lead temperature	At distance 1/16 ± 1/32 in. from case for 60 sec(CERAMIC) 10 sec(PLASTIC)		300 260	°C

Recommended Operating Conditions

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range V_{CC} : GD54/74HC Types GD54/74HCT Types	2 4.5	6 5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A : GD74 Types GD54 Types	-40 -55	+85 +125	°C
Input Rise and Fall times t_r, t_f : GD54/74HC Types at 2V at 4.5V at 6V GD54/74HCT Types at 4.5 V		1000 500 400 500	ns

Logic Diagram

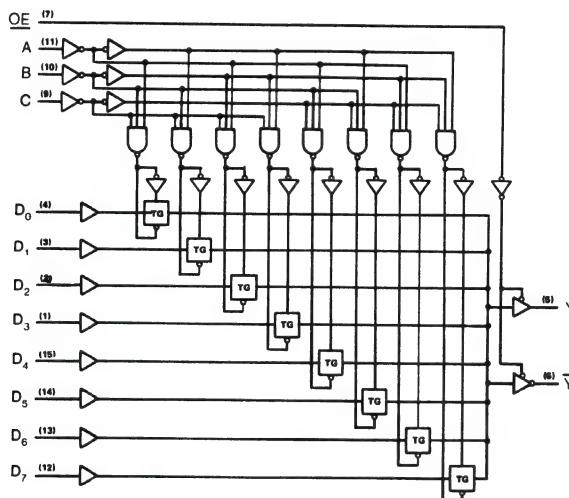


Fig. 1 Logic diagram

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HC251		GD54HC251		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2		1.5 3.15 4.2		V
V _{IL}	LOW level input voltage		2.0 4.5 6.0			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH}	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V
		or V _{IL}	4.5 6.0	3.98 5.48	4.3 5.2		3.84 5.34		3.7 5.2		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH}	2.0 4.5 6.0			0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V
		or V _{IL}	4.5 6.0		0.17 0.15	0.26 0.26		0.33 0.33		0.4 0.4	
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	6.0			0.1		1.0		1.0	μA
I _{OZ}	Three-State leakage current	V _{IN} =V _{IH} or V _{IL} V _O =V _{CC} or GND	6.0		0.01	0.5		5.0		10.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0 μA	6.0			8		80		160	μA

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HCT251		GD54HCT251		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		4.5 to 5.0	2.0			2.0		2.0		V
V _{IL}	LOW level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH}	4.5	4.4	4.5		4.4		4.4		V
		or V _{IL}	4.5	3.98	4.3		3.84		3.7		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH}	4.5			0.1		0.1		0.1	V
		or V _{IL}	4.5		0.17	0.26		0.33		0.4	
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	5.5			0.1		1.0		1.0	μA
I _{OZ}	Three-State leakage current	V _{IN} =V _{IH} or V _{IL} V _O =V _{CC} or GND	5.5		0.01	0.5		5.0		10.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0 μA	5.5			8		80		160	μA

AC Characteristics for HC: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HC251		GD54HC251		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
$t_{PLH}/$ t_{PHL}	Propagation Delay Time A,B,C to Y	2.0 4.5 6.0		58 21 19	205 41 35		256 51 44		300 60 51	ns
$t_{PLH}/$ t_{PHL}	Propagation Delay Time A,B,C to \bar{Y}	2.0 4.5 6.0		58 22 20	205 42 36		256 51 44		300 60 51	ns
$t_{PLH}/$ t_{PHL}	Propagation Delay Time D_n to Y	2.0 4.5 6.0		47 17 14	170 34 29		215 43 37		255 51 43	ns
$t_{PLH}/$ t_{PHL}	Propagation Delay Time D_n to \bar{Y}	2.0 4.5 6.0		49 19 14	170 35 31		215 44 38		255 54 44	ns
t_{PZH} t_{PZL}	3-state Output Enable Time \overline{OE} to Y, \bar{Y}	2.0 4.5 6.0		30 10 9	140 27 23		175 35 30		210 42 36	ns
$t_{PLZ}/$ t_{PHZ}	3-state Output Disable Time \overline{OE} to Y, \bar{Y}	2.0 4.5 6.0		36 13 10	140 28 24		170 35 30		210 42 36	ns
$t_{TLH}/$ t_{THL}	Output Transition Time	2.0 4.5 6.0		19 7 6	75 15 13		95 19 16		110 22 19	ns

AC Characteristics for HCT: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HCT251		GD54HCT251		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
$t_{PLH}/$ t_{PHL}	Propagation Delay Time A,B,C to Y	4.5		28	48		60		72	ns
$t_{PLH}/$ t_{PHL}	Propagation Delay Time A,B,C to \bar{Y}	4.5		28	48		60		72	ns
$t_{PLH}/$ t_{PHL}	Propagation Delay Time D_n to Y	4.5		21	35		44		53	ns
$t_{PLH}/$ t_{PHL}	Propagation Delay Time D_n to \bar{Y}	4.5		21	35		44		53	ns
t_{PZH} t_{PZL}	3-state Output Enable Time \overline{OE} to Y, \bar{Y}	4.5		14	28		35		42	ns
$t_{PLZ}/$ t_{PHZ}	3-state Output Disable Time \overline{OE} to Y, \bar{Y}	4.5		15	30		38		45	ns
$t_{TLH}/$ t_{THL}	Output Transition Time	4.5		7	15		19		22	ns

AC Waveforms

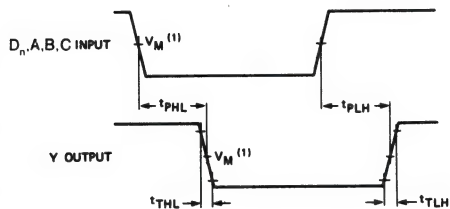


Fig. 2 Waveforms showing the multiplexer input (D_n) and select input (A, B, C) to output (Y) propagation delays and the output transition times.

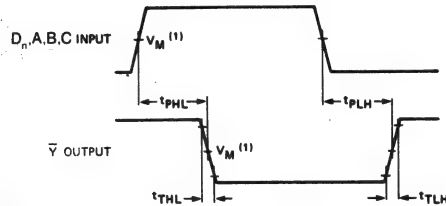


Fig. 3 Waveforms showing the multiplexer input (D_n) and select input (A, B, C) to out (Y) propagation delays and the output transition times.

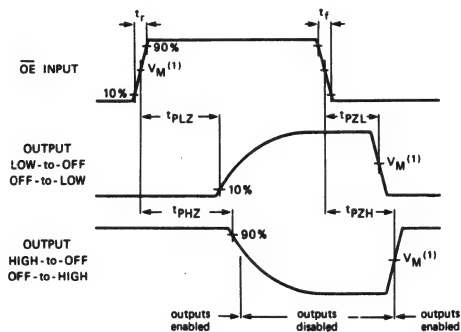


Fig. 4 Waveforms showing the 3-state enable and disable times.

Note to AC waveforms

(1) HC : $V_M = 50\%$, $V_I = \text{GND to } V_{CC}$

HCT: $V_M = 1.3V$, $V_I = \text{GND to } 3V$.

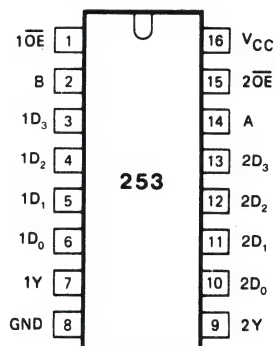
GD54/74HC253, GD54/74HCT253

DUAL 4-TO-1 LINE SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS

General Description

These devices are identical in pinout to the 54/74LS253. They contain two multiplexers, where each multiplexer is selected by two-bit address. Each multiplexer has an enable input which enables it when taken to a low logic level. When a high logic level is applied to an enable input, the outputs of its associated multiplexer are sent into a high impedance state. The HC/HCT253 are similar in function to the HC/HCT153 which do not have 3-state outputs. These devices are characterized for operation over wide temperature ranges to meet industry and military specifications.

Pin Configuration



Suffix-Blank : Plastic Dual In Line Package
 Suffix-J : Ceramic Dual In Line Package
 Suffix-D : Small Outline Package

Features

- Low Power consumption characteristic of CMOS devices
- Output drive capability: 15 LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts
for HCT 4.5 to 5.5 volts
- Low input current: 1μA Max.
- Low quiescent current: 80μA Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs

Function Table

SELECT INPUTS		DATA INPUTS				OUTPUT ENABLE	OUTPUT
A	B	nD ₀	nD ₁	nD ₂	nD ₃	nOE	nY
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
H	L	X	L	X	X	L	L
H	L	X	H	X	X	L	H
L	H	X	X	L	X	L	L
L	H	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC Supply voltage		-0.5	+7	V
I_{IK}, I_{OK}	DC input or output diode current	for $V_I < -0.5$ or $V_I > V_{CC} + 0.5V$		20	mA
I_O	DC output source or sink current	for $-0.5V < V_O < V_{CC} + 0.5V$		35	mA
I_{CC}	DC V_{CC} or GND current			70	mA
T_{stg}	Storage temperature range		-65	150	°C
P_D	Power dissipation per package	above +70°C: derate linearly with 8mW/K		500	mW
T_L	Lead temperature	At distance 1/16 ± 1/32 in. from case for 60 sec(CERAMIC) 10 sec(PLASTIC)		300 260	°C

Recommended Operating Conditions

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range V_{CC} : GD54/74HC Types GD54/74HCT Types	2 4.5	6 5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A : GD74 Types GD54 Types	-40 -55	+85 +125	°C
Input Rise and Fall times t_r, t_f : GD54/74HC Types at 2V at 4.5V at 6V GD54/74HCT Types at 4.5 V		1000 500 400 500	ns

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A = 25 °C			GD74HC253		GD54HC253		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2		1.5 3.15 4.2		V
V _{IL}	LOW level input voltage		2.0 4.5 6.0			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V
V _{OH}	HIGH level output voltage	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -20 μA	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0	1.9 4.4 5.9		1.9 4.4 5.9		V
			I _{OH} = -6 mA	4.5	3.98	4.3	3.84		3.7		
			I _{OH} = -7.8 mA	6.0	5.48	5.2	5.34		5.2		
V _{OL}	LOW level output voltage	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 20 μA	2.0 4.5 6.0			0.1 0.1 0.1	0.1 0.1 0.1		0.1 0.1 0.1	V
			I _{OL} = 6 mA	4.5		0.17	0.26	0.33		0.4	
			I _{OL} = 7.8 mA	6.0		0.15	0.26	0.33		0.4	
I _{IN}	Input leakage Current	V _{IN} = V _{CC} or GND	6.0			0.1		1.0		1.0	μA
I _{OZ}	Three-State leakage current	V _{IN} = V _{IH} or V _{IL} V _O = V _{CC} or GND	6.0		0.01	0.5		5.0		10.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} = V _{CC} or GND I _{out} = 0 μA	6.0			8		80		160	μA

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A = 25 °C			GD74HCT253		GD54HCT253		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		4.5 to 5.0	2.0			2.0		2.0		V
V _{IL}	LOW level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V _{OH}	HIGH level output voltage	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -20 μA	4.5	4.4	4.5	4.4		4.4		V
			I _{OH} = -6 mA	4.5	3.98	4.3	3.84		3.7		
V _{OL}	LOW level output voltage	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 20 μA	4.5			0.1	0.1		0.1	V
			I _{OL} = 6 mA	4.5		0.17	0.26	0.33		0.4	
I _{IN}	Input leakage Current	V _{IN} = V _{CC} or GND	5.5			0.1		1.0		1.0	μA
I _{OZ}	Three-State leakage current	V _{IN} = V _{IH} or V _{IL} V _O = V _{CC} or GND	5.5		0.01	0.5		5.0		10.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} = V _{CC} or GND I _{out} = 0 μA	5.5			8		80		160	μA

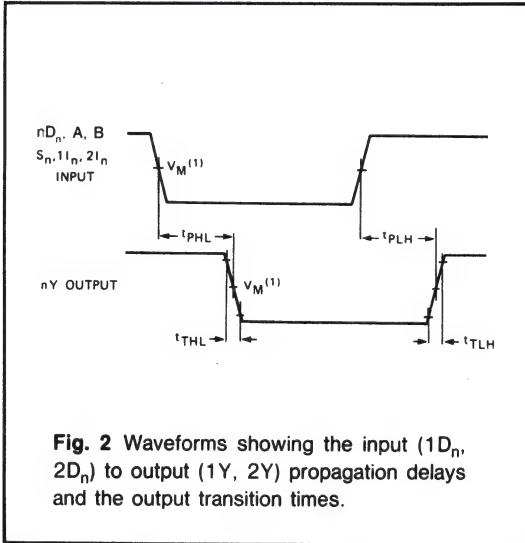
AC Characteristics for HC: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER	V_{CC}	$T_A=25^\circ\text{C}$			GD74HC253		GD54HC253		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
$t_{PLH} /$ t_{PHL}	Propagation Delay Time A, B to nY	2.0		55	175		190		225	ns
		4.5		19	30		38		45	
		6.0		15	26		32		38	
$t_{PLH} /$ t_{PHL}	Propagation Delay Time nD_n to nY	2.0		54	126		175		210	ns
		4.5		16	28		35		42	
		6.0		13	23		30		36	
$t_{PZH} /$ t_{PZL}	3-state Output Enable Time $n\overline{OE}$ to nY	2.0		28	100		125		150	ns
		4.5		11	20		25		30	
		6.0		9	17		21		26	
$t_{PLZ} /$ t_{PHZ}	3-state Output Disable Time $n\overline{OE}$ to nY	2.0		29	135		170		203	ns
		4.5		14	30		38		45	
		6.0		12	25		31		38	
$t_{TLH} /$ t_{THL}	Output Transition Time	2.0		28	60		75		90	ns
		4.5		7	12		15		18	
		6.0		6	10		13		15	

AC Characteristics for HC: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER	V_{CC}	$T_A=25^\circ\text{C}$			GD74HCT253		GD54HCT253		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
$t_{PLH} /$ t_{PHL}	Propagation Delay Time A, B to nY	4.5		22	40		50		60	ns
$t_{PLH} /$ t_{PHL}	Propagation Delay Time nD_n to nY	4.5		20	38		48		57	ns
$t_{PZH} /$ t_{PZL}	3-state Output Enable Time $n\overline{OE}$ to nY	4.5		15	25		30		35	ns
$t_{PLZ} /$ t_{PHZ}	3-state Output Disable Time $n\overline{OE}$ to nY	4.5		19	35		42		50	ns
$t_{TLH} /$ t_{THL}	Output Transition Time	4.5		7	12		15		18	ns

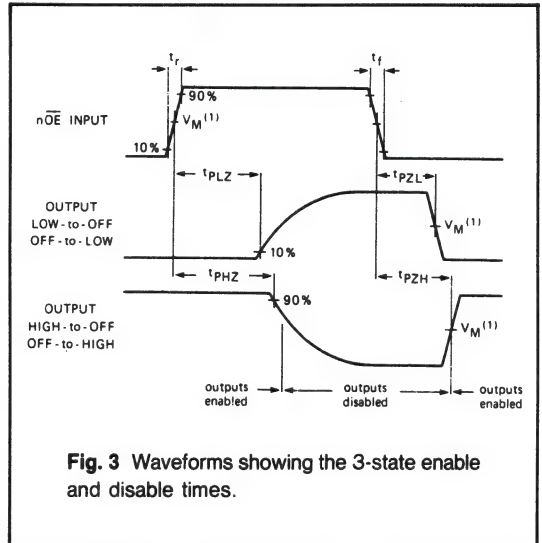
AC Waveforms



Note to AC waveforms

(1) HC : $V_M = 50\%$; $V_I = \text{GND to } V_{CC}$.

HCT : $V_M = 1.3V$; $V_I = \text{GND to } 3V$.



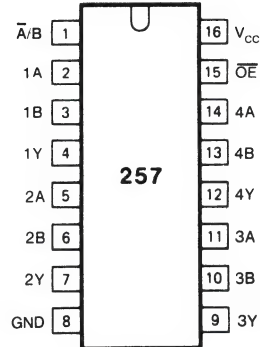
GD54/74HC257, GD54/74HCT257

QUAD 2-INPUT SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS

General Description

These devices are identical in pinout to the 54/74LS257. They consist of four 2-input multiplexers with common select and enable inputs, and noninverted outputs. When the enable input is low the four outputs assume the value as selected from the inputs. When the enable input is high, The outputs become high impedance state regardless of any other input values. Select decoding is done internally resulting in a single select input only. The HC/HCT 257 are similar in function to the HC/HCT 157 & 158 which do not have 3-state outputs, and to the HC/HCT 258 which have inverted outputs. These devices are characterized for operation over wide temperature ranges to meet industry and military specifications.

Pin Configuration



Suffix-Blank : Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package
Suffix-D : Small Outline Package

Features

- Low Power consumption characteristic of CMOS devices
- Output drive capability: 15 LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts
for HCT 4.5 to 5.5 volts
- Low input current: $1\mu\text{A}$ Max.
- Low quiescent current: $80\mu\text{A}$ Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs

Function Table

INPUTS				OUTPUT
$\overline{\text{OE}}$	$\overline{\text{A/B}}$	nA	nB	nY
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC Supply voltage		-0.5	+7	V
I_{IK}, I_{OK}	DC input or output diode current	for $V_I < -0.5$ or $V_I > V_{CC} + 0.5V$		20	mA
I_O	DC output source or sink current	for $-0.5V < V_O < V_{CC} + 0.5V$		35	mA
I_{CC}	DC V_{CC} or GND current			70	mA
T_{stg}	Storage temperature range		-65	150	°C
P_D	Power dissipation per package	above +70°C: derate linearly with 8mW/K		500	mW
T_L	Lead temperature	At distance $1/16 \pm 1/32$ in. from case for 60 sec(CERAMIC) 10 sec(PLASTIC)		300 260	°C

Recommended Operating Conditions

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range V_{CC} : GD54/74HC Types GD54/74HCT Types	2 4.5	6 5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A : GD74 Types GD54 Types	-40 -55	+85 +125	°C
Input Rise and Fall times t_r, t_f : GD54/74HC Types at 2V at 4.5V at 6V GD54/74HCT Types at 4.5V		1000 500 400 500	ns

Logic Diagram

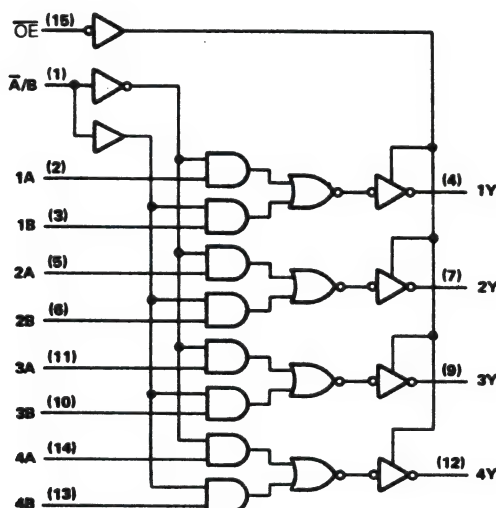


Fig. 1 Logic diagram

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A = 25°C			GD74HC257		GD54HC257		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2		1.5 3.15 4.2		V
V _{IL}	LOW level input voltage		2.0 4.5 6.0			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V
V _{OH}	HIGH level output voltage	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -20μA	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9	V
			I _{OH} = -6mA I _{OH} = -7.8mA	4.5 6.0	3.98 5.48	4.3 5.2		3.84 5.34		3.7 5.2	
		V _{IN} = V _{IH} or V _{IL}	I _{OL} = 20μA	2.0 4.5 6.0			0.1 0.1 0.1	0.1 0.1 0.1		0.1 0.1 0.1	V
			I _{OL} = 6mA I _{OL} = 7.8mA	4.5 6.0		0.17 0.15	0.26 0.26	0.33 0.33		0.4 0.4	
I _{IN}	Input leakage Current	V _{IN} = V _{CC} or GND	6.0			0.1		1.0		1.0	μA
I _{OZ}	Three-State leakage current	V _{IN} = V _{IH} or V _{IL}	V _O = V _{CC} or GND	6.0		0.01	0.5		5.0	10.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} = V _{CC} or GND I _{out} = 0μA	6.0			8		80		160	μA

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A = 25°C			GD74HCT257		GD54HCT257		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		4.5 to 5.0	2.0			2.0		2.0		V
V _{IL}	LOW level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V _{OH}	HIGH level output voltage	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -20μA	4.5	4.4	4.5		4.4		4.4	V
			I _{OH} = -6mA	4.5	3.98	4.3		3.84		3.7	
V _{OL}	LOW level output voltage	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 20μA	4.5		0.1		0.1		0.1	V
			I _{OL} = 6mA	4.5		0.17	0.26	0.33		0.4	
I _{IN}	Input leakage Current	V _{IN} = V _{CC} or GND	5.5			0.1		1.0		1.0	μA
I _{OZ}	Three-State leakage current	V _{IN} = V _{IH} or V _{IL}	V _O = V _{CC} or GND	5.5		0.01	0.5		5.0	10.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} = V _{CC} or GND I _{out} = 0μA	5.5			8		80		160	μA

AC Characteristics for HC: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HC257		GD54HC257		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} / t_{PHL}	Propagation Delay Time nA,nB to nY	2.0 4.5 6.0		36 10 9	100 20 17		125 25 21		150 30 25	ns
t_{PLH} / t_{PHL}	Propagation Delay Time \overline{A}/B to nY	2.0 4.5 6.0		47 12 10	100 24 20		125 29 25		150 34 29	ns
t_{PZH} / t_{PZL}	3-state Output Enable Time \overline{OE} to nY	2.0 4.5 6.0		33 12 10	150 30 26		190 38 32		225 45 38	ns
t_{PLZ} / t_{PHZ}	3-state Output Disable Time \overline{OE} to nY	2.0 4.5 6.0		41 15 12	150 30 26		190 38 32		225 45 38	ns
t_{TLH} / t_{THL}	Output Transition Time	2.0 4.5 6.0		28 7 6	60 12 10		75 15 13		90 18 15	ns

AC Characteristics for HCT: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HCT257		GD54HCT257		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} / t_{PHL}	Propagation Delay Time nA,nB to nY	4.5		16	30		38		45	ns
t_{PLH} / t_{PHL}	Propagation Delay Time \overline{A}/B to nY	4.5		18	32		44		50	ns
t_{PZH} / t_{PZL}	3-state Output Enable Time \overline{OE} to nY	4.5		15	30		38		45	ns
t_{PLZ} / t_{PHZ}	3-state Output Disable Time \overline{OE} to nY	4.5		16	30		38		45	ns
t_{TLH} / t_{THL}	Output Transition Time	4.5		7	12		15		18	ns

AC Waveforms

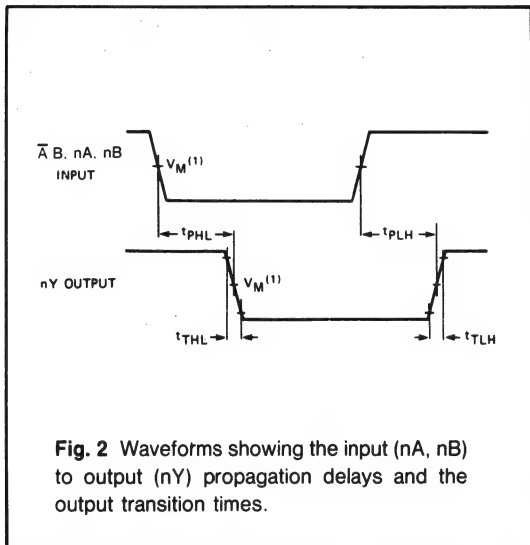


Fig. 2 Waveforms showing the input (nA, nB) to output (nY) propagation delays and the output transition times.

Note to AC waveforms

- (1) HC : $V_M=50\%$; $V_I=GND$ to V_{CC} .
HCT : $V_M=1.3V$; $V_I=GND$ to $3V$.

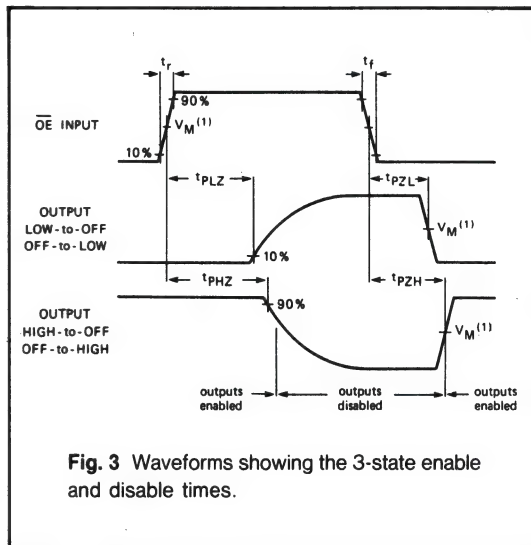


Fig. 3 Waveforms showing the 3-state enable and disable times.

GD54/74HC258, GD54/74HCT258

QUAD 2-INPUT SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS

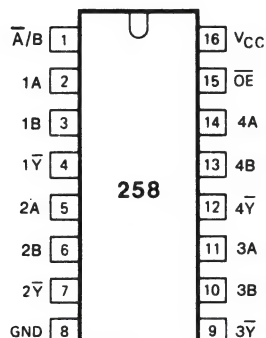
General Description

These devices are identical in pinout to the 54/74LS258. They consist of four 2-input multiplexers with common select and enable inputs, and inverted outputs. When the enable input is low, the four outputs assume the value as selected from the inputs. When the enable input is high, The outputs become high impedance state regardless of any other input values. Select decoding is done internally resulting in a single select input only. The HC/HCT 258 are similar in function to the HC/HCT 157 & 158 which do not have 3 state outputs, and to the HC/HCT 257 which have noninverted outputs. These devices are characterized for operation over wide temperature ranges to meet industry and military specifications.

Features

- Low Power consumption characteristic of CMOS devices
- Output drive capability: 15 LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts
for HCT 4.5 to 5.5 volts
- Low input current: 1 μ A Max.
- Low quiescent current: 80 μ A Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs

Pin Configuration



Suffix-Blank : Plastic Dual In Line Package
 Suffix-J : Ceramic Dual In Line Package
 Suffix-D : Small Outline Package

Function Table

\overline{OE}	INPUTS			OUTPUT
	$\overline{A/B}$	nA	nB	nY
H	X	X	X	Z
L	H	X	L	H
L	H	X	H	L
L	L	L	X	H
L	L	H	X	L

H = HIGH voltage level
 L = LOW voltage level
 X = don't care
 Z = high impedance OFF-state

Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC Supply voltage		-0.5	+7	V
I_{IK}, I_{OK}	DC input or output diode current	for $V_I < -0.5$ or $V_I > V_{CC} + 0.5V$		20	mA
I_O	DC output source or sink current	for $-0.5V < V_O < V_{CC} + 0.5V$		35	mA
I_{CC}	DC V_{CC} or GND current			70	mA
T_{stg}	Storage temperature range		-65	150	°C
P_D	Power dissipation per package	above +70°C: derate linearly with 8mW/K		500	mW
T_L	Lead temperature	At distance $1/16 \pm 1/32$ in. from case for 60 sec(CERAMIC) 10 sec(PLASTIC)		300 260	°C

Recommended Operating Conditions

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range V_{CC} : GD54/74HC Types GD54/74HCT Types	2 4.5	6 5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A : GD74 Types GD54 Types	-40 -55	+85 +125	°C
Input Rise and Fall times t_r, t_f : GD54/74HC Types at 2V at 4.5V at 6V GD54/74HCT Types at 4.5V		1000 500 400 500	ns

Logic Diagram

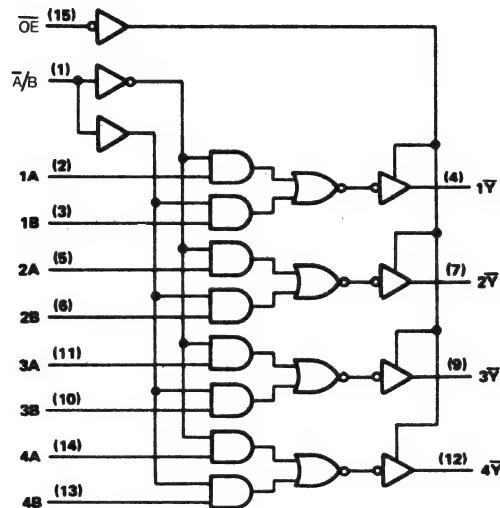


Fig. 1 Logic diagram

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HC258		GD54HC258		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2		1.5 3.15 4.2		V
V _{IL}	LOW level input voltage		2.0 4.5 6.0			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH} or V _{IL}	I _{OH} =-20μA I _{OH} =-6mA I _{OH} =-7.8mA	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0	1.9 4.4 5.9		1.9 4.4 5.9		V
				4.5 6.0	3.98 5.48	4.3 5.2	3.84 5.34		3.7 5.2		
				2.0 4.5 6.0			0.1 0.1 0.1	0.1 0.1 0.1		0.1 0.1 0.1	
V _{OL}	LOW level output voltage	V _{IN} =V _{IH} or V _{IL}	I _{OL} =20μA I _{OL} =6mA I _{OL} =7.8mA	2.0 4.5 6.0				0.1 0.1 0.1		0.1 0.1 0.1	V
				4.5 6.0		0.17 0.15	0.26 0.26	0.33 0.33		0.4 0.4	
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	6.0			0.1		1.0		1.0	μA
I _{OZ}	Three-State leakage current	V _{IN} =V _{IH} or V _{IL} V _O =V _{CC} or GND	6.0		0.01	0.5		5.0		10.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	6.0			8		80		160	μA

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HCT258		GD54HCT258		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		4.5 to 5.0	2.0			2.0		2.0		V
V _{IL}	LOW level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH} or V _{IL}	I _{OH} =-20μA	4.5	4.4	4.5	4.4		4.4		V
			I _{OH} =-6mA	4.5	3.98	4.3	3.84		3.7		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH} or V _{IL}	I _{OL} =20μA	4.5		0.1		0.1		0.1	V
			I _{OL} =6mA	4.5		0.17	0.26	0.33		0.4	
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	5.5			0.1		1.0		1.0	μA
I _{OZ}	Three-State leakage current	V _{IN} =V _{IH} or V _{IL} V _O =V _{CC} or GND	5.5		0.01	0.5		5.0		10.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	5.5			8		80		160	μA

AC Characteristics for HC: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HC258		GD54HC258		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
$t_{PLH} /$ t_{PHL}	Propagation Delay Time nA,nB to $n\bar{Y}$	2.0 4.5 6.0		38 12 11	100 22 19		125 27 23		150 32 25	ns
$t_{PLH} /$ t_{PHL}	Propagation Delay Time \bar{A}/B to $n\bar{Y}$	2.0 4.5 6.0		49 14 12	100 26 22		125 31 27		150 34 31	ns
$t_{PZH} /$ t_{PZL}	3-state Output Enable Time \overline{OE} to $n\bar{Y}$	2.0 4.5 6.0		35 14 12	150 32 28		190 40 34		225 45 40	ns
$t_{PLZ} /$ t_{PHZ}	3-state Output Disable Time \overline{OE} to $n\bar{Y}$	2.0 4.5 6.0		45 17 14	150 32 28		190 40 34		225 45 40	ns
$t_{TLH} /$ t_{THL}	Output Transition Time	2.0 4.5 6.0		28 7 6	60 12 10		75 15 13		90 18 15	ns

AC Characteristics for HCT: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HCT258		GD54HCT258		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
$t_{PLH} /$ t_{PHL}	Propagation Delay Time nA,nB to $n\bar{Y}$	4.5		17	32		40		45	ns
$t_{PLH} /$ t_{PHL}	Propagation Delay Time \bar{A}/B to $n\bar{Y}$	4.5		19	34		46		53	ns
$t_{PZH} /$ t_{PZL}	3-state Output Enable Time \overline{OE} to $n\bar{Y}$	4.5		16	32		40		45	ns
$t_{PLZ} /$ t_{PHZ}	3-state Output Disable Time \overline{OE} to $n\bar{Y}$	4.5		17	32		40		45	ns
$t_{TLH} /$ t_{THL}	Output Transition Time	4.5		7	12		15		18	ns

AC Waveforms

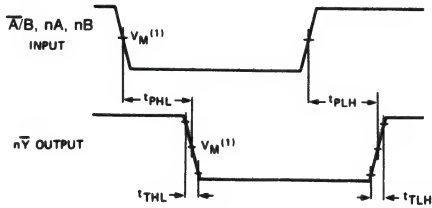


Fig. 2 Waveforms showing the input ($n\bar{A}$, $n\bar{B}$) to output ($n\bar{Y}$) propagation delays and the output transition times.

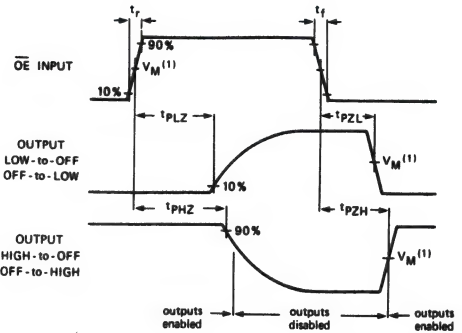


Fig. 3 Waveforms showing the 3-state enable and disable times.

Note to AC waveforms

(1) HC : $V_M = 50\%$; $V_I = \text{GND to } V_{CC}$.

HCT : $V_M = 1.3V$; $V_I = \text{GND to } 3V$.

GD54/74HC259, GD54/74HCT259

8-BIT ADDRESSABLE LATCH/3-TO-8 LINE DECODER

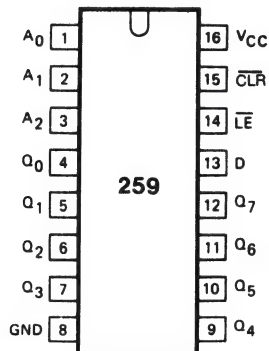
General Description

These devices are identical in pinout to the 54/74LS259. This 8-Bit Addressable latch can perform four basic functions in the addressable latch mode, data is read into the addressed stage of the latch. In the memory mode, the latch contents are stored regardless of any other inputs. in the 8-line decoder mode, data flows through to the addressed output. And in the clear mode, all stages are cleared to the low state. To eliminate the possibility of entering erroneous data into the latches, the enable should be held high (inactive) while the address lines are changing.

Features

- Low Power consumption characteristic of CMOS devices
- Output drive capability: 10 LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts
for HCT 4.5 to 5.5 volts
- Low input current: $1\mu\text{A}$ Max.
- Low quiescent current: $80\mu\text{A}$ Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs

Pin Configuration



Suffix-Blank : Plastic Dual In Line Package
 Suffix-J : Ceramic Dual In Line Package
 Suffix-D : Small Outline Package

Logic Diagram

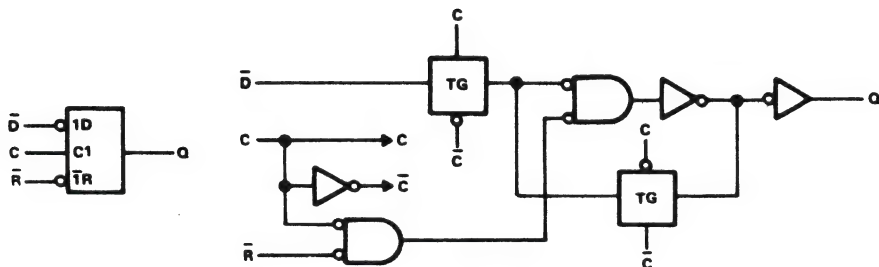


Fig. 1 Logic diagram (each latch)

Function Table

OPERATING MODES	INPUTS						OUTPUTS							
	CLR	LE	D	A ₀	A ₁	A ₂	Q ₀	Q ₁	Q ₂	Q ₃	Q ₄	Q ₅	Q ₆	Q ₇
master clear	L	H	X	X	X	X	L	L	L	L	L	L	L	L
demultiplex (active HIGH) decoder (when D = H)	L	L	d	L	L	L	Q=d	L	L	L	L	L	L	L
	L	L	d	L	L	L	L	Q=d	L	L	L	L	L	L
	L	L	d	L	L	L	L	L	Q=d	L	L	L	L	L
	L	L	d	L	L	L	L	L	L	Q=d	L	L	L	L
	L	L	d	L	L	L	L	L	L	L	Q=d	L	L	L
store (do nothing)	H	H	X	X	X	X	q ₀	q ₁	q ₂	q ₃	q ₄	q ₅	q ₆	q ₇
addressable latch	H	L	d	L	L	L	Q=d	q ₁	q ₂	q ₃	q ₄	q ₅	q ₆	q ₇
	H	L	d	L	L	L	q ₀	Q=d	q ₂	q ₃	q ₄	q ₅	q ₆	q ₇
	H	L	d	L	L	L	q ₀	q ₁	Q=d	q ₃	q ₄	q ₅	q ₆	q ₇
	H	L	d	L	L	L	q ₀	q ₁	q ₂	Q=d	q ₄	q ₅	q ₆	q ₇
	H	L	d	L	L	L	q ₀	q ₁	q ₂	q ₃	Q=d	q ₅	q ₆	q ₇
	H	L	d	L	L	L	q ₀	q ₁	q ₂	q ₃	q ₄	Q=d	q ₆	q ₇
	H	L	d	L	L	L	q ₀	q ₁	q ₂	q ₃	q ₄	q ₅	Q=d	q ₇
	H	L	d	L	L	L	q ₀	q ₁	q ₂	q ₃	q ₄	q ₅	q ₆	Q=d

H = HIGH voltage level
L = LOW voltage level
X = don't care
d = HIGH or LOW data one set-up time prior to the LOW-to-HIGH LE transition
q = lower case letters indicate the state of the referenced output established during the last cycle in which it was addressed or cleared

Logic Diagram

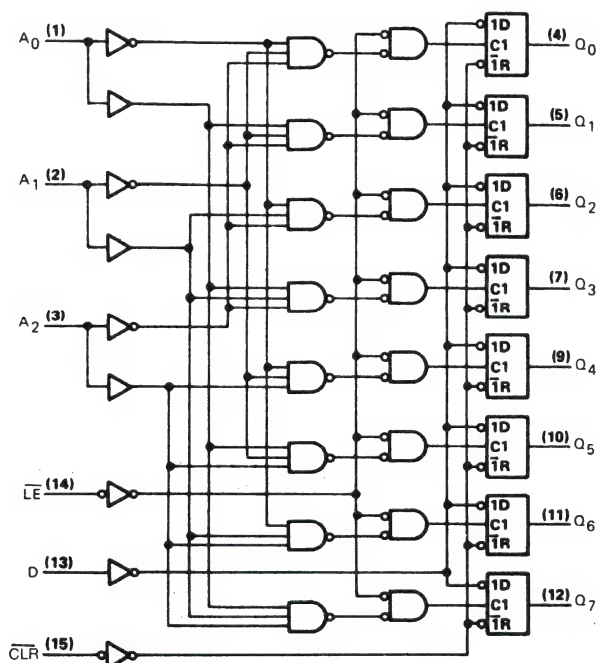


Fig. 2 Logic diagram

Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC Supply voltage		-0.5	+7	V
I_{IK}, I_{OK}	DC input or output diode current	for $V_I < -0.5$ or $V_I > V_{CC} + 0.5V$		20	mA
I_O	DC output source or sink current	for $-0.5V < V_O < V_{CC} + 0.5V$		25	mA
I_{CC}	DC V_{CC} or GND current			50	mA
T_{stg}	Storage temperature range		-65	150	°C
P_D	Power dissipation per package	above +70°C: derate linearly with 8mW/K		500	mW
T_L	Lead temperature	At distance 1/16 ± 1/32 in. from case for 60 sec(CERAMIC) 10 sec(PLASTIC)		300 260	°C

Recommended Operating Conditions

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range V_{CC} : GD54/74HC Types	2	6	V
GD54/74HCT Types	4.5	5.5	
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A : GD74 Types	-40	+85	°C
GD54 Types	-55	+125	
Input Rise and Fall times t_r, t_f : GD54/74HC Types at 2V		1000	ns
at 4.5V		500	
at 6V		400	
GD54/74HCT Types at 4.5V		500	

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HC259		GD54HC259		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2		1.5 3.15 4.2		V
V _{IL}	LOW level input voltage		2.0 4.5 6.0			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH}	I _{OH} =-20μA	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0	1.9 4.4 5.9		1.9 4.4 5.9		V
			I _{OH} =-4mA	4.5 6.0	3.98 5.48	4.3 5.2	3.84 5.34		3.7 5.2		
		or V _{IL}	I _{OH} =-4mA	4.5 6.0	3.98 5.48	4.3 5.2	3.84 5.34		3.7 5.2		
			I _{OH} =-5.2mA	4.5 6.0	3.98 5.48	4.3 5.2	3.84 5.34		3.7 5.2		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH}	I _{OL} =20μA	2.0 4.5 6.0			0.1 0.1 0.1	0.1 0.1 0.1		0.1 0.1 0.1	V
			I _{OL} =4mA	4.5 6.0		0.17 0.15	0.26 0.26	0.33 0.33		0.4 0.4	
		or V _{IL}	I _{OL} =4mA	4.5 6.0		0.17 0.15	0.26 0.26	0.33 0.33		0.4 0.4	
			I _{OL} =5.2mA	4.5 6.0		0.17 0.15	0.26 0.26	0.33 0.33		0.4 0.4	
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	6.0			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	6.0			8		80		160	μA

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HCT259		GD54HCT259		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		4.5 to 5.5	2.0			2.0		2.0		V
V _{IL}	LOW level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH}	I _{OH} =-20μA	4.5	4.4	4.5	4.4		4.4		V
		or V _{IL}	I _{OH} =-4mA	4.5	3.98	4.3	3.84		3.7		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH}	I _{OL} =20μA	4.5			0.1	0.1		0.1	V
		or V _{IL}	I _{OL} =4mA	4.5		0.17	0.26	0.33		0.4	
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	5.5			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	5.5			8		80		160	μA

Timing Requirements for HC: $t_r = t_f = 6\text{ns}$ $C_L = 50\text{ pF}$

SYMBOL	PARAMETER		V _{CC} (V)	T _A = 25°C			GD74HCT259		GD54HCT259		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t _W	Pulse width	$\overline{\text{LE}}$, $\overline{\text{CLR}}$ high or low	2.0	80	30		100		120		ns
			4.5	16	10		20		25		
			6.0	14	8		18		22		
t _{SU}	Setup time	Data after $\overline{\text{LE}}\downarrow$	2.0	60	30		100		120		ns
			4.5	12	10		20		25		
			6.0	10	8		18		22		
t _H	Hold time	Data before $\overline{\text{LE}}\downarrow$	2.0	3	0		3		3		ns
			4.5	3	0		3		3		
			6.0	3	0		3		3		

AC Characteristics for HC: $t_r = t_f = 6\text{ns}$ $C_L = 50\text{ pF}$

SYMBOL	PARAMETER		V _{CC} (V)	T _A = 25°C			GD74HCT259		GD54HCT259		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t _{PLH} / t _{PHL}	Propagation Delay Time D to Qn		2.0		50	160		210		260	ns
			4.5		18	35		42		50	
			6.0		17	30		38		46	
t _{PLH} / t _{PHL}	Propagation Delay Time An to Qn		2.0		50	160		210		260	ns
			4.5		18	35		42		50	
			6.0		17	30		38		46	
t _{PLH} / t _{PHL}	Propagation Delay Time $\overline{\text{LE}}$ to Qn		2.0		48	150		200		250	ns
			4.5		17	33		40		48	
			6.0		16	28		36		42	
t _{PHL}	Propagation Delay Time $\overline{\text{CLR}}$ to Qn		2.0		48	150		200		250	ns
			4.5		17	32		40		48	
			6.0		16	28		36		42	
t _{TLH} / t _{THL}	Output Transition Time		2.0		25	70		85		100	ns
			4.5		8	15		18		22	
			6.0		7	13		16		19	

Timing Requirements for HCT : $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER		V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HCT259		GD54HCT259		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_w	Pulse width	\overline{LE} , \overline{CLR} high or low	4.5	16	10		20		25		ns
t_{su}	Setup time	Data after $\overline{LE} \downarrow$	4.5	12	10		20		25		ns
t_h	Hold time	Data before $\overline{LE} \downarrow$	4.5	3	0		3		3		ns

AC Characteristics for HCT: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HCT259		GD54HCT259		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation Delay Time D to Qn	4.5		20	38		46		55	ns
$t_{PLH}/$ t_{PHL}	Propagation Delay Time An to Qn	4.5		20	38		46		55	ns
$t_{PLH}/$ t_{PHL}	Propagation Delay Time \overline{LE} to Qn	4.5		19	36		44		52	ns
t_{PHL}	Propagation Delay Time \overline{CLR} to Qn	4.5		19	36		44		52	ns
$t_{TLH}/$ t_{THL}	Output Transition Time	4.5		8	15		18		22	ns

AC Waveforms

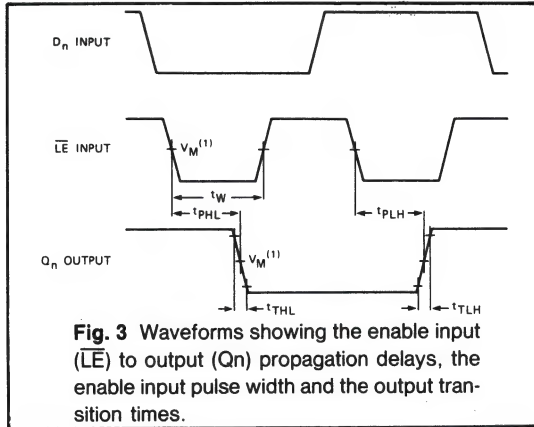


Fig. 3 Waveforms showing the enable input (\overline{LE}) to output (Q_n) propagation delays, the enable input pulse width and the output transition times.

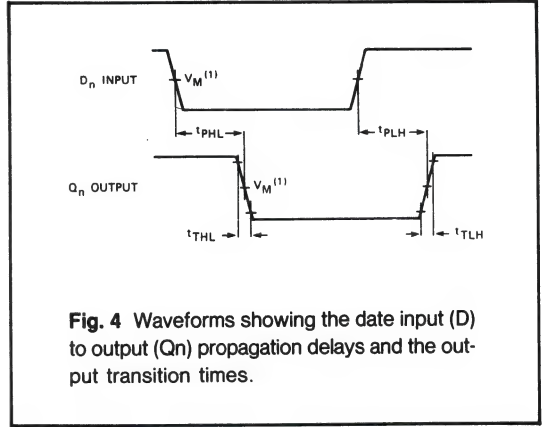


Fig. 4 Waveforms showing the data input (D) to output (Q_n) propagation delays and the output transition times.

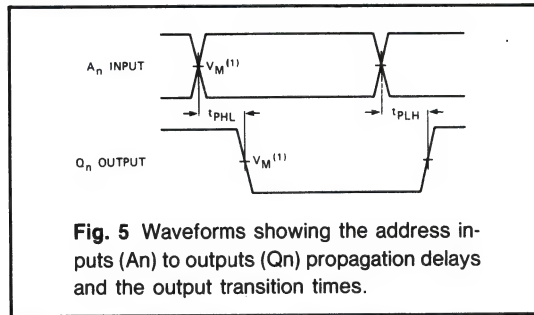


Fig. 5 Waveforms showing the address inputs (A_n) to outputs (Q_n) propagation delays and the output transition times.

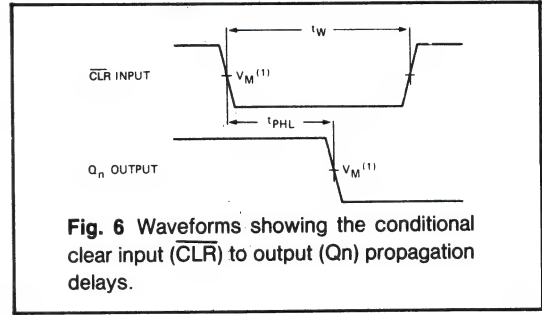


Fig. 6 Waveforms showing the conditional clear input (\overline{CLR}) to output (Q_n) propagation delays.

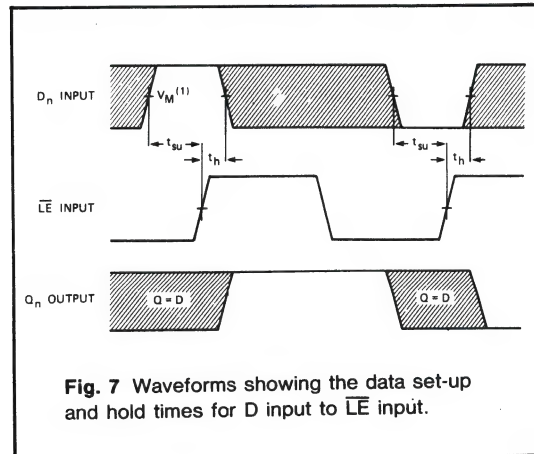


Fig. 7 Waveforms showing the data set-up and hold times for D input to \overline{LE} input.

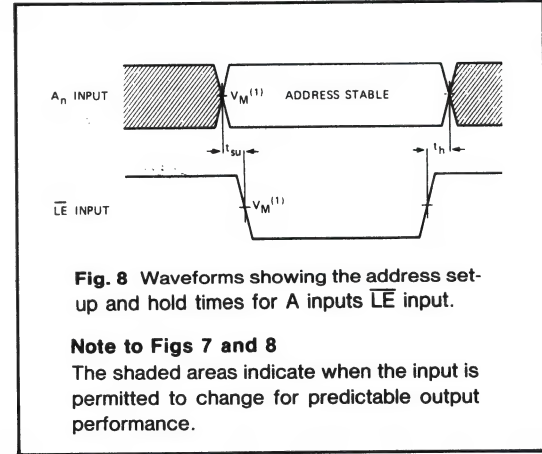


Fig. 8 Waveforms showing the address set-up and hold times for A inputs \overline{LE} input.

Note to Figs 7 and 8

The shaded areas indicate when the input is permitted to change for predictable output performance.

Note to AC waveforms

- (1) HC : $V_M = 50\%$; $V_I = \text{GND to } V_{CC}$.
HCT : $V_M = 1.3V$; $V_I = \text{GND to } 3V$.

GD54/74HC266, GD54/74HCT266

QUAD 2-INPUT EXCLUSIVE NOR GATES

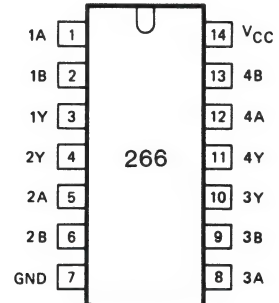
General Description

These devices are identical in pinout to the 54/74LS266. These circuits contain four independent 2-input Exclusive NOR gates. Unlike the 54/74LS266 which is an open collector gate, the HC/HCT 266 has standard CMOS push-pull outputs. These devices are characterized for operation over wide temperature ranges to meet industry and military specifications.

Features

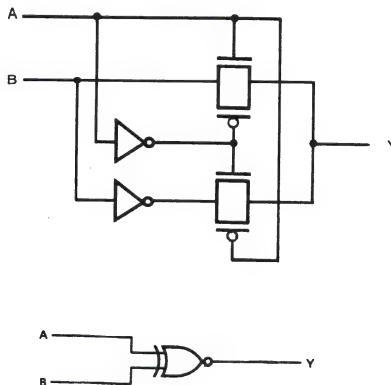
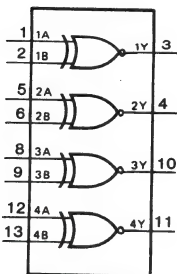
- Low Power consumption characteristic of CMOS devices
- Output drive capability: 10 LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts
for HCT 4.5 to 5.5 volts
- Low input current: $1\mu\text{A}$ Max.
- Low quiescent current: $20\mu\text{A}$ Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs

Pin Configuration



Suffix-Blank : Plastic Dual In Line Package
 Suffix-J : Ceramic Dual In Line Package
 Suffix-D : Small Outline Package

Logic Symbol and Diagram



Function Table

INPUTS		OUTPUT
nA	nB	nY
L	L	H
L	H	L
H	L	L
H	H	H

H=HIGH voltage level
 L=LOW voltage level

Fig. 1 Logic symbol

Fig. 2 Logic diagram (one gate)

Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V _{CC}	DC Supply voltage		-0.5	+7	V
I _{IK} , I _{OK}	DC input or output diode current	for V _I < -0.5 or V _I > V _{CC} + 0.5V		20	mA
I _O	DC output source or sink current	for -0.5V < V _O < V _{CC} + 0.5V		25	mA
I _{CC}	DC V _{CC} or GND current			50	mA
T _{stg}	Storage temperature range		-65	150	°C
P _D	Power dissipation per package	above +70°C: derate linearly with 8mW/K		500	mW
T _L	Lead temperature	At distance 1/16 ± 1/32 in. from case for 60 sec(CERAMIC) 10 sec(PLASTIC)		300 260	°C

Recommended Operating Conditions

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range V_{CC} : GD54/74HC Types GD54/74HCT Types	2 4.5	6 5.5	V
DC Input or Output Voltage V_I , V_O	0	V_{CC}	V
Operating Temperature T_A : GD74 Types GD54 Types	-40 -55	+85 +125	°C
Input Rise and Fall times t_r , t_f : GD54/74HC Types at 2V at 4.5V at 6V GD54/74HCT Types at 4.5V		1000 500 400 500	ns

Logic Diagram

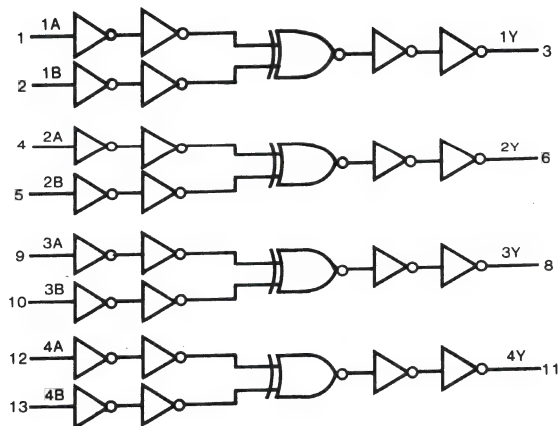


Fig. 3 Circuit diagram

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HC266		GD54HC266		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2		1.5 3.15 4.2		V
V _{IL}	LOW level input voltage		2.0 4.5 6.0			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH} I _{OH} =-20μA	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V
		or V _{IL} I _{OH} =-4mA I _{OH} =-5.2mA	4.5 6.0	3.98 5.48	4.3 5.2		3.84 5.34		3.7 5.2		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH} I _{OL} =20μA	2.0 4.5 6.0			0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V
		or V _{IL} I _{OL} =4mA I _{OL} =5.2mA	4.5 6.0		0.17 0.15	0.26 0.26		0.33 0.33		0.4 0.4	
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	6.0			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	6.0			2		20		40	μA

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HCT266		GD54HCT266		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		4.5 to 5.5	2.0			2.0		2.0		V
V _{IL}	LOW level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH} I _{OH} =-20μA	4.5	4.4	4.5		4.4		4.4		V
		or V _{IL} I _{OH} =-4mA	4.5	3.98	4.3		3.84		3.7		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH} I _{OL} =20μA	4.5			0.1		0.1		0.1	V
		or V _{IL} I _{OL} =4mA	4.5		0.17	0.26		0.33		0.4	
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	5.5			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	5.5			2		20		40	μA

AC Characteristics for HC: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HC266		GD54HC266		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
$t_{PLH}/$ t_{PHL}	Propagation Delay Time nA, nB to nY	2.0 4.5 6.0		39 14 11	120 24 20		150 30 26		180 36 31	ns
$t_{TLH}/$ t_{THL}	Output Transition Time	2.0 4.5 6.0		19 7 6	75 15 13		95 19 16		110 22 19	ns

AC Characteristics for HCT: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HCT266		GD54HCT266		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
$t_{PLH}/$ t_{PHL}	Propagation Delay Time nA, nB to nY	4.5		16	26		32		38	ns
$t_{TLH}/$ t_{THL}	Output Transition Time	4.5		7	15		19		22	ns

AC Waveform

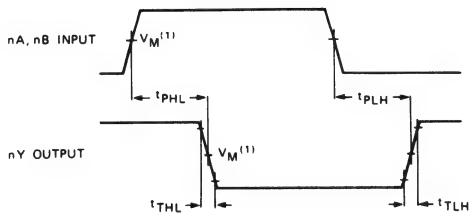


Fig. 4 Waveforms showing the input (nA, nB) to output (nY) propagation delays and the output transition times.

Note to AC waveform

- (1) HC : $V_M=50\%$, $V_I=\text{GND to } V_{CC}$
HCT: $V_M=1.3\text{V}$; $V_I=\text{GND to } 3\text{V}$.

GD54/74HC273, GD54/74HCT273

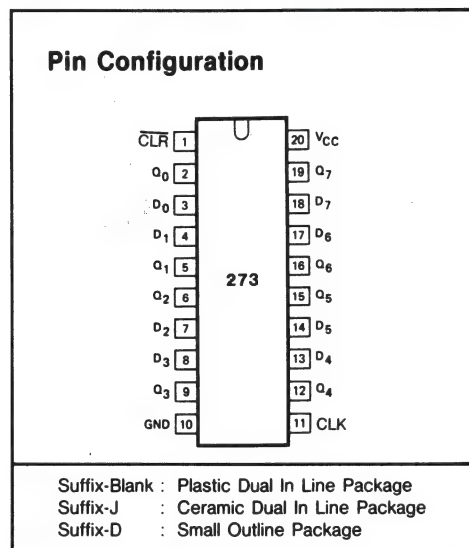
OCTAL D-TYPE FLIP-FLOPS WITH COMMON CLOCK & CLEAR

General Description

These devices are identical in pinout to the 54/74LS273. They consist of eight master/slave D-type flip-flops with a common Clock and common Clear. Data on the D input having the specified setup and hold times is transferred to the Q output on the rising edge of the Clock input. The Clear input when low, sets all outputs to a low state. These devices are characterized for operation over wide temperature ranges to meet industry and military specifications.

Features

- Low Power consumption characteristic of CMOS devices
- Output drive capability: 10 LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts
for HCT 4.5 to 5.5 volts
- Low input current: $1\mu\text{A}$ Max.
- Low quiescent current: $80\mu\text{A}$ Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs



Function Table

OPERATING MODES	INPUTS			OUTPUTS
	CLR	CLK	D _n	Q _n
reset (clear)	L	X	X	L
load "1"	H	↑	h	H
load "0"	H	↑	l	L

H = HIGH voltage level
 h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CLK transition
 L = LOW voltage level
 l = LOW voltage level one set-up time prior to the LOW-to-HIGH CLK transition
 ↑ = LOW-to-HIGH transition
 X = don't care

Logic Diagram

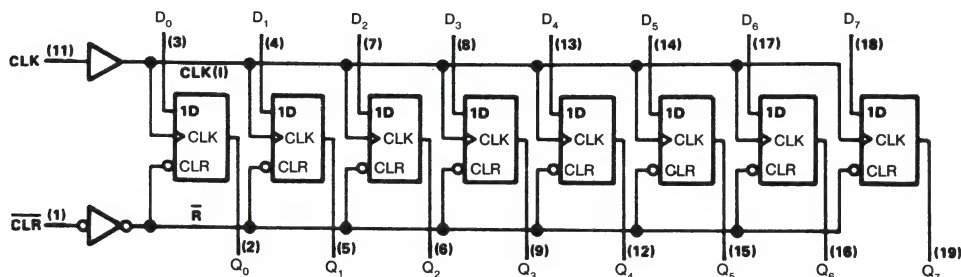


Fig. 1 Logic diagram

Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC Supply voltage		-0.5	+7	V
I_{IK}, I_{OK}	DC input or output diode current	for $V_I < -0.5$ or $V_I > V_{CC} + 0.5V$		20	mA
I_O	DC output source or sink current	for $-0.5V < V_O < V_{CC} + 0.5V$		25	mA
I_{CC}	DC V_{CC} or GND current			50	mA
T_{stg}	Storage temperature range		-65	150	°C
P_D	Power dissipation per package	above +70°C: derate linearly with 8mW/K		500	mW
T_L	Lead temperature	At distance 1/16±1/32 in. from case for 60 sec(CERAMIC) 10 sec(PLASTIC)		300 260	°C

Recommended Operating Conditions

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range V_{CC} : GD54/74HC Types GD54/74HCT Types	2 4.5	6 5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A : GD74 Types GD54 Types	-40 -55	+85 +125	°C
Input Rise and Fall times t_r, t_f : GD54/74HC Types at 2V at 4.5V at 6V GD54/74HCT Types at 4.5 V		1000 500 400 500	ns

Logic Diagram

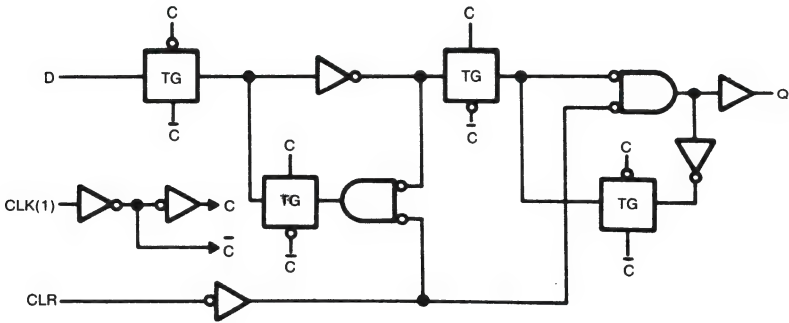


Fig. 2 Logic diagram (one gate)

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HC273		GD54HC273		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2		1.5 3.15 4.2		V
V _{IL}	LOW level input voltage		2.0 4.5 6.0			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH}	I _{OH} =-20μA	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0	1.9 4.4 5.9		1.9 4.4 5.9		V
		or V _{IL}	I _{OH} =-4mA I _{OH} =-5.2mA	4.5 6.0	3.98 5.48	4.3 5.2	3.84 5.34		3.7 5.2		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH}	I _{OL} =20μA	2.0 4.5 6.0			0.1 0.1 0.1	0.1 0.1 0.1		0.1 0.1 0.1	V
		or V _{IL}	I _{OL} =4mA I _{OL} =5.2mA	4.5 6.0		0.17 0.15	0.26 0.26	0.33 0.33		0.4 0.4	
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	6.0			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	6.0			8		80		160	μA

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HCT273		GD54HCT273		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		4.5 to 5.5	2.0			2.0		2.0		V
V _{IL}	LOW level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH}	I _{OH} =-20μA	4.5	4.4	4.5	4.4		4.4		V
		or V _{IL}	I _{OH} =-4mA	4.5	3.98	4.3	3.84		3.7		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH}	I _{OL} =20μA	4.5		0.1	0.1		0.1		V
		or V _{IL}	I _{OL} =4mA	4.5		0.17	0.26		0.33		
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	5.5			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	5.5			8		80		160	μA

Timing Requirements for HC: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER		V_{CC}	$T_A=25^\circ\text{C}$			GD74HC273		GD54HC273		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_w	Pulse duration	$\overline{\text{CLR}}$ (low)	2.0	80	30		100		120		ns
			4.5	16	10		20		25		
			6.0	14	8		18		22		
		CLK (high or low)	2.0	80	30		100		120		ns
			4.5	16	10		20		25		
			6.0	14	8		18		22		
t_{su}	Set up time	Data before CLK \uparrow	2.0	60	30		80		100		ns
			4.5	15	10		18		20		
			6.0	14	8		16		18		
t_{rec}	Recovery time	$\overline{\text{CLR}}$ inactive	2.0	5	0		5		5		ns
			4.5	5	0		5		5		
			6.0	5	0		5		5		
t_h	Hold time	data after CLK \uparrow	2.0	3	0		3		3		ns
			4.5	3	0		3		3		
			6.0	3	0		3		3		

AC Characteristics for HC: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER		V_{CC}	$T_A=25^\circ\text{C}$			GD74HC273		GD54HC273		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
f_{max}	Pulse frequency Maximum clock		2.0	6	20		5		4		MHz
			4.5	30	65		25		20		
			6.0	35	75		30		25		
$t_{PLH} /$ t_{PHL}	Propagation Delay Time CLK to Q_n		2.0		46	160		200		240	ns
			4.5		15	30		40		50	
			6.0		14	28		35		45	
$t_{PLH} /$ t_{PHL}	Propagation Delay Time $\overline{\text{CLR}}$ to Q_n		2.0		45	155		190		230	ns
			4.5		15	28		38		45	
			6.0		14	26		34		40	
$t_{TLH} /$ t_{THL}	Output Transition Time		2.0		25	70		85		100	ns
			4.5		8	15		18		22	
			6.0		7	13		16		18	

Timing Requirements for HCT: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER		V_{CC}	$T_A=25^\circ\text{C}$			GD74HCT273		GD54HCT273		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_w	pulse duration	$\overline{\text{CLR}}$ (low)	4.5	18	10		20		25		ns
		CLK (high or low)	4.5	17	10		20		25		ns
t_{su}	Set up time	Data before CLK \uparrow	4.5	15	10		18		20		ns
t_{rec}	Recovery time	CLR inactive	4.5	5	0		5		5		ns
t_h	Hold time / hold time	data after CLK \uparrow	4.5	3	0		3		3		ns

AC Characteristics for HCT: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER	V_{CC}	$T_A=25^\circ\text{C}$			GD74HCT273		GD54HCT273		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
f_{max}	Pulse frequency Maximum clock	4.5	27	54		22		18		MHz
t_{PLH} / t_{PHL}	Propagation Delay Time CLK to Q_n	4.5		16	30		40		50	ns
t_{PLH} / t_{PHL}	Propagation Delay Time $\overline{\text{CLR}}$ to Q_n	4.5		17	30		40		50	ns
t_{TLH} / t_{THL}	Output Transition Time	4.5		8	15		18		22	ns

AC Waveforms

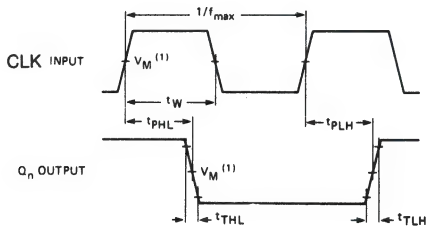


Fig. 3 Waveforms showing the clock (CLK) to output (Q_n) propagation delays, the clock pulse width output transition times and the maximum clock pulse frequency.

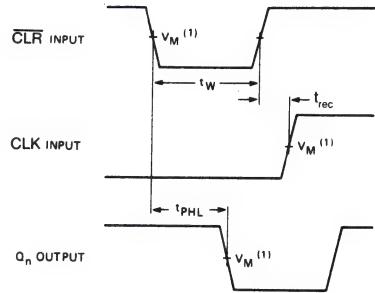


Fig. 4 Waveforms showing the master clear ($\overline{\text{CLR}}$) pulse width, the master clear to output (Q_n) propagation delays and the master clear to clock (CLK) recovery time.

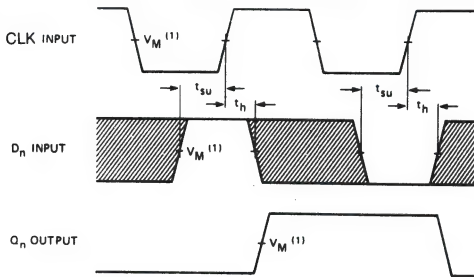


Fig. 5 Waveforms showing the data set-up and hold times for the data input (D_n).

Note to Fig. 5

The staded areas indicate when the input is permitted to change for predictable output performance.

Note to AC waveforms

- (1) HC : V_M=50%; V_I=GND to V_{CC}.
HCT : V_M=1.3V; V_I=GND to 3V.

GD54/74HC280, GD54/74HCT280

9-BIT EVEN/ODD PARITY GENERATOR/CHECKER

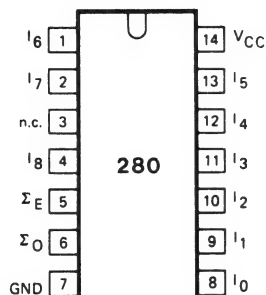
General Description

These devices are identical in pinout to the 54/74LS280. They contain 9-bit inputs and 2 outputs (even and odd parities) to facilitate operation of either even or odd parity applications. Words of greater than 9 bits can be accommodated by cascading other HC/HCT 280 devices. These devices are characterized for operation over wide temperature ranges to meet industry and military specifications.

Features

- Low Power consumption characteristic of CMOS devices
- Output drive capability: 10 LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts
for HCT 4.5 to 5.5 volts
- Low input current: 1 μ A Max.
- Low quiescent current: 80 μ A Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs

Pin Configuration



Suffix-Blank : Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package
Suffix-D : Small Outline Package

Function Table

INPUTS	OUTPUTS	
number of HIGH data inputs (I_0 to I_8)	Σ_E	Σ_O
even	H	L
odd	L	H

H=HIGH voltage level
L=LOW voltage level

Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC Supply voltage		-0.5	+7	V
I_{IK}, I_{OK}	DC input or output diode current	for $V_I < -0.5$ or $V_I > V_{CC} + 0.5V$		20	mA
I_O	DC output source or sink current	for $-0.5V < V_O < V_{CC} + 0.5V$		25	mA
I_{CC}	DC V_{CC} or GND current			50	mA
T_{stg}	Storage temperature range		-65	150	°C
P_D	Power dissipation per package	above +70°C: derate linearly with 8mW/K		500	mW
T_L	Lead temperature	At distance 1/16 ± 1/32 in. from case for 60 sec(CERAMIC) 10 sec(PLASTIC)		300 260	°C

Recommended Operating Conditions

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range V_{CC} : GD54/74HC Types GD54/74HCT Types	2 4.5	6 5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A : GD74 Types GD54 Types	-40 -55	+85 +125	°C
Input Rise and Fall times t_r, t_f : GD54/74HC Types at 2V at 4.5V at 6V GD54/74HCT Types at 4.5V		1000 500 400 500	ns

Logic Diagram

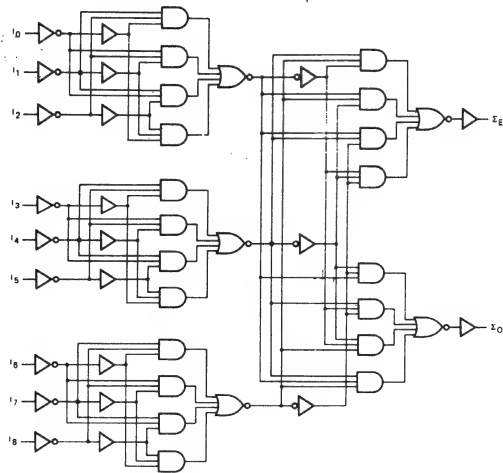


Fig. 1 Logic diagram

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HC280		GD54HC280		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2		1.5 3.15 4.2		V
V _{IL}	LOW level input voltage		2.0 4.5 6.0			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH}	I _{OH} =-20μA	2.0	1.9	2.0	1.9		1.9		V
				4.5	4.4	4.5	4.4		4.4		
		or V _{IL}	I _{OH} =-4mA I _{OH} =-5.2mA	6.0	5.9	6.0	5.9		5.9		
				4.5	3.98	4.3	3.84		3.7		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH}	I _{OL} =20μA	2.0			0.1		0.1		V
				4.5			0.1		0.1		
		or V _{IL}	I _{OL} =4mA I _{OL} =5.2mA	6.0			0.1		0.1		
				4.5		0.17	0.26		0.33		
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	6.0			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	6.0			8		80		160	μA

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HCT280		GD54HCT280		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		4.5 to 5.5	2.0			2.0		2.0		V
V _{IL}	LOW level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH}	I _{OH} =-20μA	4.5	4.4	4.5	4.4		4.4		V
		or V _{IL}	I _{OH} =-4mA	4.5	3.98	4.3	3.84		3.7		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH}	I _{OL} =20μA	4.5			0.1		0.1		V
		or V _{IL}	I _{OL} =4mA	4.5		0.17	0.26		0.33		
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	5.5			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	5.5			8		80		160	μA

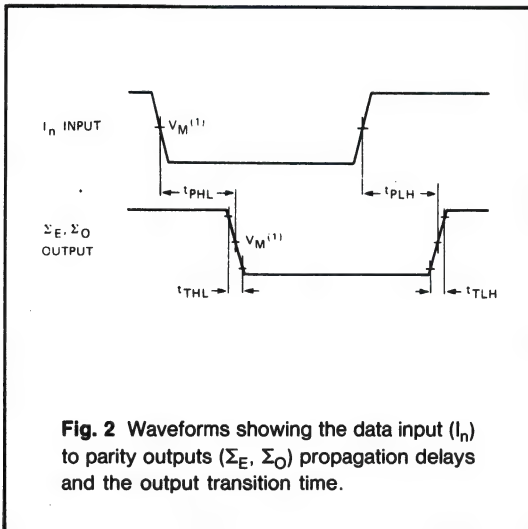
AC Characteristics for HC: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HC280		GD54HC280		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
$t_{PLH} /$ t_{PHL}	Propagation Delay Time I to Σ_E	2.0 4.5 6.0		50 18 16	160 35 30		210 42 38		260 50 40	ns
$t_{PLH} /$ t_{PHL}	Propagation Delay Time I to Σ_O	2.0 4.5 6.0		60 20 18	180 38 32		230 50 42		280 58 49	ns
$t_{TLH} /$ t_{THL}	Output Transition Time	2.0 4.5 6.0		25 8 7	70 15 13		85 18 16		100 22 19	ns

AC Characteristics for HCT: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HCT280		GD54HCT280		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
$t_{PLH} /$ t_{PHL}	Propagation Delay Time I to Σ_E	4.5		20	38		46		55	ns
$t_{PLH} /$ t_{PHL}	Propagation Delay Time I to Σ_O	4.5		22	40		52		60	ns
$t_{TLH} /$ t_{THL}	Output Transition Time	4.5		8	15		18		22	ns

AC Waveform



Note to AC waveform

(1) HC : $V_M=50\%$; $V_I=GND$ to V_{CC} .

HCT: $V_M=1.3\%$; $V_I=GND$ to $3V$.

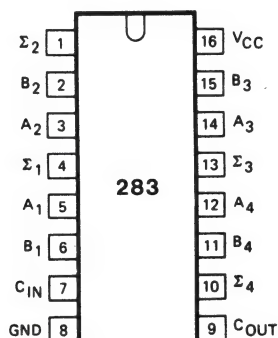
GD54/74HC283, GD54/74HCT283

4-BIT BINARY FULL ADDER WITH FAST CARRY

General Description

These devices are identical in pinout to the 54/74LS283. This full adder performs the addition of two 4-bit binary numbers with internal carry lookahead. The device adds two 4-bit words plus the carry-in bit. The binary sum appears at the sum outputs, and any resulting carries appear at the carry-out output. This adder features full internal look-ahead across all four bits. This provides the system designer with partial look-ahead performance at reduced package count of a ripple-carry implementation. The adder logic, including the carry, is implemented in its true form meaning that the end-around carry can be accomplished without the need for logic or level inversion. These devices are characterized for operation over wide temperature ranges to meet industry and military specifications.

Pin Configuration



Suffix-Blank : Plastic Dual In Line Package
 Suffix-J : Ceramic Dual In Line Package
 Suffix-D : Small Outline Package

Features

- Low Power consumption characteristic of CMOS devices
- Output drive capability: 10 LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts
for HCT 4.5 to 5.5 volts
- Low input current: 1μA Max.
- Low quiescent current: 80μA Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs

Function Table

PINS	C _{IN}	A ₁	A ₂	A ₃	A ₄	B ₁	B ₂	B ₃	B ₄	Σ ₁	Σ ₂	Σ ₃	Σ ₄	C _{OUT}	EXAMPLE
logic levels	L	L	H	L	H	H	L	L	H	H	H	L	L	H	
active HIGH	0	0	1	0	1	1	0	0	1	1	1	0	0	1	(a)
active LOW	1	1	0	1	0	0	1	1	0	0	0	1	1	0	(b)

H=HIGH voltage level
 L=LOW voltage level

Example 1001
 1010
 10011

(a) for active HIGH,
 example=(9+10=19)
 (b) for active LOW,
 example=(carry+6+5=12)

Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC Supply voltage		-0.5	+7	V
I_{IK}, I_{OK}	DC input or output diode current	for $V_I < -0.5$ or $V_I > V_{CC} + 0.5V$		20	mA
I_O	DC output source or sink current	for $-0.5V < V_O < V_{CC} + 0.5V$		25	mA
I_{CC}	DC V_{CC} or GND current			50	mA
T_{stg}	Storage temperature range		-65	150	°C
P_D	Power dissipation per package	above +70°C: derate linearly with 8mW/K		500	mW
T_L	Lead temperature	At distance 1/16 ± 1/32 in. from case for 60 sec(CERAMIC) 10 sec(PLASTIC)		300 260	°C

Recommended Operating Conditions

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range V_{CC} : GD54/74HC Types GD54/74HCT Types	2 4.5	6 5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A : GD74 Types GD54 Types	-40 -55	+85 +125	°C
Input Rise and Fall times t_r, t_f : GD54/74HC Types at 2V at 4.5V at 6V GD54/74HCT Types at 4.5V		1000 500 400 500	ns

Logic Diagram

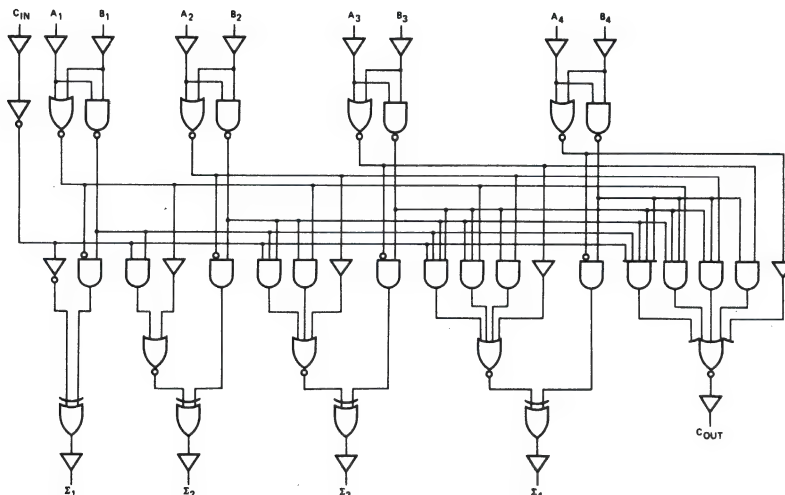


Fig. 1 Logic diagram

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION	V _{CC}	T _A =25°C			GD74HC283		GD54HC283		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2		1.5 3.15 4.2		V
V _{IL}	LOW level output voltage		2.0 4.5 6.0			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH}	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V
		or V _{IL}									
V _{OL}	LOW level output voltage	V _{IN} =V _{IH}	2.0 4.5 6.0			0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V
		or V _{IL}									
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	6.0			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	6.0			8		80		160	μA

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION	V _{CC}	T _A =25°C			GD74HCT283		GD54HCT283		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		4.5 to 5.5	2.0			2.0		2.0		V
V _{IL}	LOW level output voltage		4.5 to 5.5			0.8		0.8		0.8	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH}	4.5	4.4	4.5		4.4		4.4		V
		or V _{IL}	4.5	3.98	4.3		3.84		3.7		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH}	4.5			0.1		0.1		0.1	V
		or V _{IL}	4.5		0.17	0.26		0.33		0.4	
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	5.5			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	5.5			8		80		160	μA

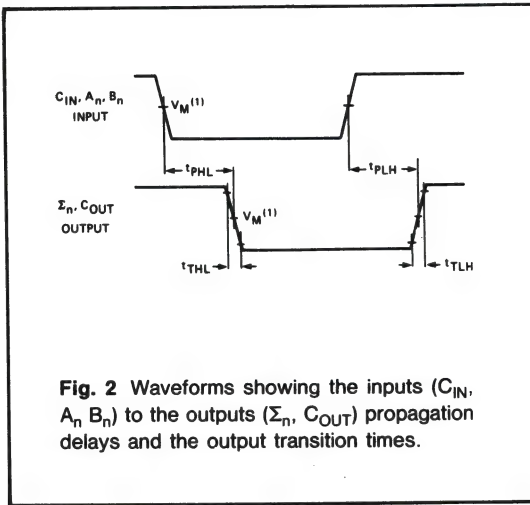
AC Characteristics for HC: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HC283		GD54HC283		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
$t_{PLH}/$ t_{PHL}	Propagation Delay Time C_{IN} to $\Sigma 1$	2.0 4.5 6.0		50 18 16	150 35 30		210 42 38		260 50 46	ns
$t_{PLH}/$ t_{PHL}	Propagation Delay Time C_{IN} to $\Sigma 2$	2.0 4.5 6.0		55 19 17	160 36 30		220 46 40		270 54 52	ns
$t_{PLH}/$ t_{PHL}	Propagation Delay Time C_{IN} to $\Sigma 3$	2.0 4.5 6.0		60 20 18	180 38 32		230 50 42		280 58 49	ns
$t_{PLH}/$ t_{PHL}	Propagation Delay Time C_{IN} to $\Sigma 4$	2.0 4.5 6.0		63 22 20	190 40 36		240 52 46		290 60 54	ns
$t_{PLH}/$ t_{PHL}	Propagation Delay Time A_n or B_n to Σn	2.0 4.5 6.0		60 21 19	180 38 36		230 50 45		280 58 52	ns
$t_{PLH}/$ t_{PHZ}	Propagation Delay Time C_{IN} to C_{OUT}	2.0 4.5 6.0		60 20 18	180 38 32		230 50 42		280 55 46	ns
$t_{PLH}/$ t_{PHL}	Propagation Delay Time A_n or B_n to C_{OUT}	2.0 4.5 6.0		60 20 18	180 38 32		230 50 42		280 58 46	ns
$t_{TLH}/$ t_{THL}	Output Transition Time	2.0 4.5 6.0		25 8 7	70 15 13		85 18 16		100 22 19	ns

AC Characteristics for HCT: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HCT283		GD54HCT283		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
$t_{PLH}/$ t_{PHL}	Propagation Delay Time C_{IN} to $\Sigma 1$	4.5		20	38		50		58	ns
$t_{PLH}/$ t_{PHL}	Propagation Delay Time C_{IN} to $\Sigma 2$	4.5		21	38		50		58	ns
$t_{PLH}/$ t_{PHL}	Propagation Delay Time C_{IN} to $\Sigma 3$	4.5		22	40		52		60	ns
$t_{PLH}/$ t_{PHL}	Propagation Delay Time C_{IN} to $\Sigma 4$	4.5		24	42		54		65	ns
$t_{PLH}/$ t_{PHL}	Propagation Delay Time A_n or B_n to Σn	4.5		23	42		54		65	ns
$t_{PLH}/$ t_{PHZ}	Propagation Delay Time C_{IN} to C_{OUT}	4.5		22	40		52		60	ns
$t_{PLH}/$ t_{PHL}	Propagation Delay Time A_n or B_n to C_{OUT}	4.5		22	40		52		60	ns
$t_{TLH}/$ t_{THL}	Output Transition Time	4.5		8	15		18		22	ns

AC Waveform



Note to AC waveform

- (1) HC = $V_M=50\%$; $V_I=GND$ to V_{CC} .
 HCT: $V_M=1.3V$; $V_I=GND$ to $3V$.

GD54/74HC298, GD54/74HCT298

QUAD 2-INPUT MULTIPLEXERS WITH OUTPUT LATCH

General Description

These devices are identical in pinout to the 54/74LS298. They select one of two 4-bit words to be stored in the output latch according to clock timing. When the word select input is taken low word 1 (A₁, B₁, C₁ and D₁) is presented to the inputs of the flip-flops, and when it is taken high word 2 (A₂, B₂, C₂ and D₂) is presented to the inputs of the flip-flops. The selected word is clocked to the output terminals on the falling edge of the clock pulse. This device is the equivalent of a quad 2-input multiplexer followed by a 4-bit edge-triggered latch. These devices are characterized for operation over wide temperature ranges to meet industry and military specifications.

Features

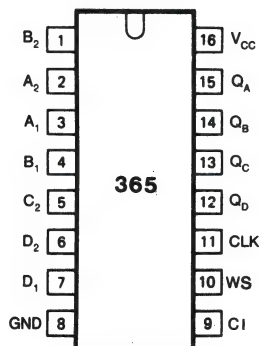
- Low Power consumption characteristic of CMOS devices
- Output drive capability: 10 LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts
for HCT 4.5 to 5.5 volts
- Low input current: 1 μ A Max.
- Low quiescent current: 80 μ A Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs

Function Table

INPUTS		OUTPUTS			
WORD SELECT	CLOCK	Q _A	Q _B	Q _C	Q _D
		a1	b1	c1	d1
L	↓	a1	b1	c1	d1
H	↓	a2	b2	c2	d2
X	H	Q _{A0}	Q _{B0}	Q _{C0}	Q _{D0}

H = High level (steady state)
L = LOW level (steady state)
X = Irrelevant (any input, including transitions)
↓ = transition from high to low level
a1, a2, etc. = the level of steady-state input at
A1, A2, etc.
Q_{A0}, Q_{B0}, etc. = the level of Q_A, Q_B, etc.
entered on the most-
recent, ↓ transition of the
clock input.

Pin Configuration



Suffix-Blank : Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package
Suffix-D : Small Outline Package

Logic Diagram

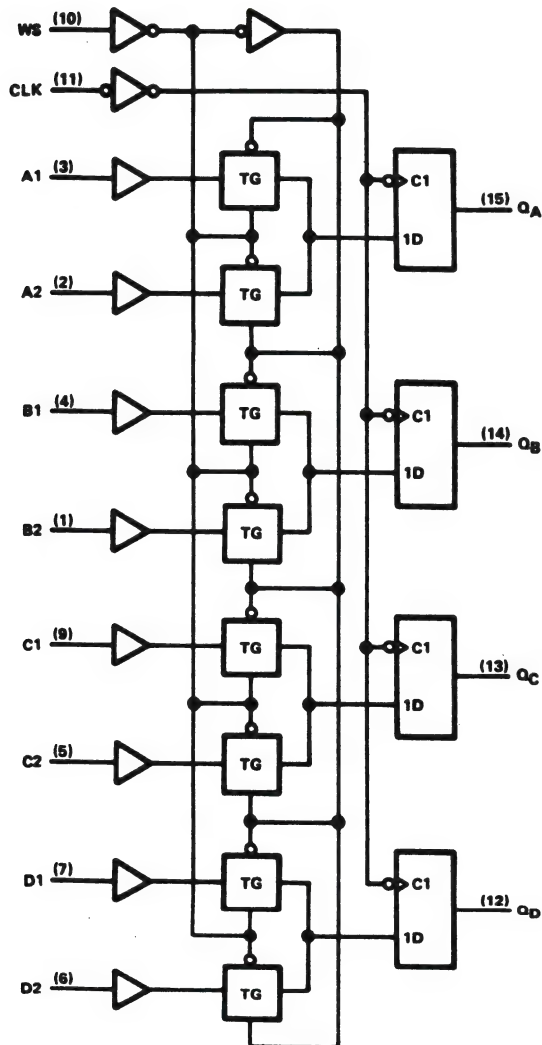


Fig. 1 Logic diagram

Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC Supply voltage		-0.5	+7	V
I_{IK}, I_{OK}	DC input or output diode current	for $V_I < -0.5$ or $V_I > V_{CC} + 0.5V$		20	mA
I_O	DC output source or sink current	for $-0.5V < V_O < V_{CC} + 0.5V$		25	mA
I_{CC}	DC V_{CC} or GND current			50	mA
T_{stg}	Storage temperature range		-65	150	°C
P_D	Power dissipation per package	above +70°C: derate linearly with 8mW/K		500	mW
T_L	Lead temperature	At distance 1/16±1/32 in. from case for 60 sec(CERAMIC) 10 sec(PLASTIC)		300 260	°C

Recommended Operating Conditions

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range V_{CC} : GD54/74HC Types GD54/74HCT Types	2 4.5	6 5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A : GD74 Types GD54 Types	-40 -55	+85 +125	°C
Input Rise and Fall times t_r, t_f : GD54/74HC Types at 2V at 4.5V at 6V GD54/74HCT Types at 4.5 V		1000 500 400 500	ns

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HC298		GD54HC298		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2		1.5 3.15 4.2		V
V _{IL}	LOW level input voltage		2.0 4.5 6.0			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH}	I _{OH} =-20μA	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0	1.9 4.4 5.9		1.9 4.4 5.9		V
		or V _{IL}	I _{OH} =-4mA I _{OH} =-5.2mA	4.5 6.0	3.98 5.48	4.3 5.2	3.84 5.34		3.7 5.2		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH}	I _{OL} =20μA	2.0 4.5 6.0			0.1 0.1 0.1	0.1 0.1 0.1		0.1 0.1 0.1	V
		or V _{IL}	I _{OL} =4mA I _{OL} =5.2mA	4.5 6.0		0.17 0.15	0.26 0.26	0.33 0.33		0.4 0.4	
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	6.0			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	6.0			8		80		160	μA

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HCT298		GD54HCT298		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		4.5 to 5.5	2.0			2.0		2.0		V
V _{IL}	LOW level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH}	I _{OH} =-20μA	4.5	4.4	4.5	4.4		4.4		V
		or V _{IL}	I _{OH} =-4mA	4.5	3.98	4.3	3.84		3.7		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH}	I _{OL} =20μA	4.5			0.1	0.1		0.1	V
		or V _{IL}	I _{OL} =4mA	4.5		0.17	0.26	0.33		0.4	
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	5.5			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	5.5			8		80		160	μA

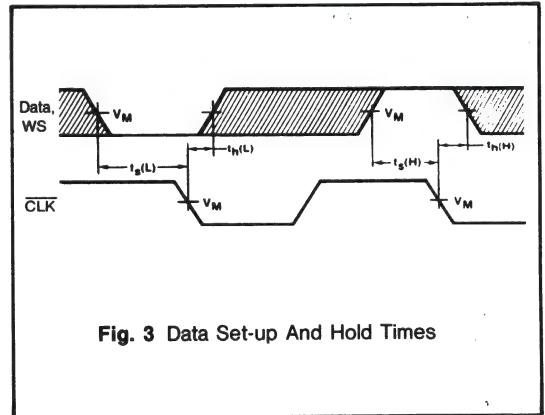
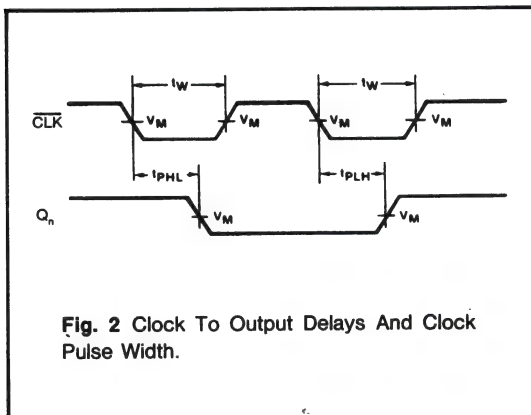
Timing Requirements for HC: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HC298		GD54HC298		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_w	Pulse width	CLK high or low	2.0	75		95		115		ns
			4.5	15		19		23		
			6.0	13		16		20		
t_{su}	Setup time	WS, Data before CLK \downarrow	2.0	80		105		115		ns
			4.5	16		21		25		
			6.0	14		18		21		
t_h	Hold time	WS, Data after CLK \downarrow	2.0	0		0		0		ns
			4.5	0		0		0		
			6.0	0		0		0		

AC Characteristics for HC: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HC298		GD54HC298		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
f_{max}	Maximum Clock Pulse Frequency	2.0	6.5			5.5		4.3		MHz
		4.5	33			27		22		
		6.0	38			31		25		
$t_{PLH}/$ t_{PHL}	Propagation Delay Time CLK to Q_n	2.0		46	120		155		190	ns
		4.5		15	25		31		38	
		6.0		12	21		21		31	
$t_{TLH}/$ t_{THL}	Output Transition Time	2.0		19	75		95		110	ns
		4.5		7	15		19		22	
		6.0		6	13		16		19	

AC Waveforms



Note to AC waveforms

- (1) HC : $V_M=50\%$; $V_I=GND$ to V_{CC} .
HCT : $V_M=1.3V$; $V_I=GND$ to $3V$.

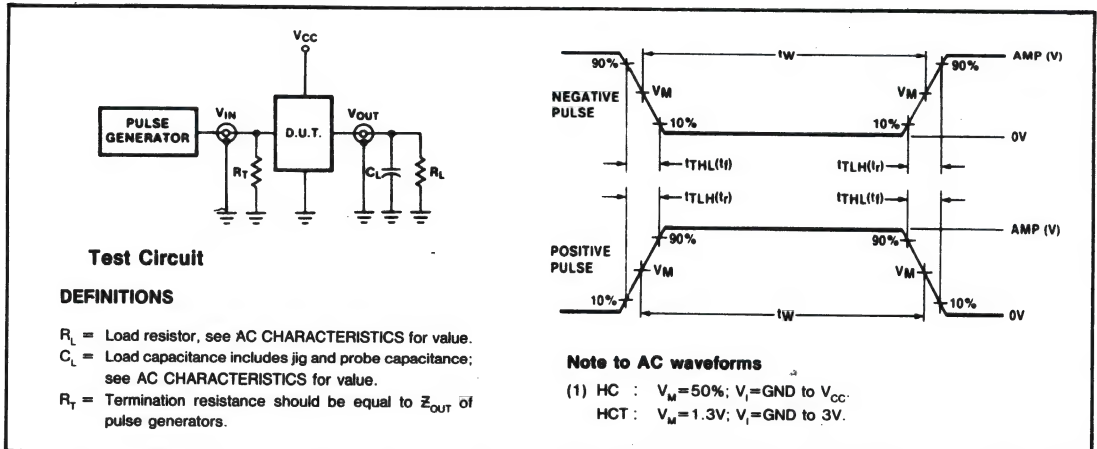
Timing Requirements for HCT: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER		V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HCT298		GD54HCT298		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_w	Pulse width	CLK high or low	4.5	19			23		27		ns
t_{su}	Setup time	WS, Data before CLK \downarrow	4.5	17			21		26		ns
t_h	Hold time	WS, Data after CLK \downarrow	4.5	17			21		26		ns

AC Characteristics for HCT: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER		V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HCT298		GD54HCT298		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
f_{max}	Maximum Clock Pulse Frequency		4.5	30			26		20		MHz
$t_{PLH}/$ t_{PHL}	Propagation Delay Time CLK to Q_n		4.5		19	29		35		42	ns
$t_{TLH}/$ t_{THL}	Output Transition Time		4.5		7	15		19		22	ns

Typical Clear, Shift, and Clear Sequences



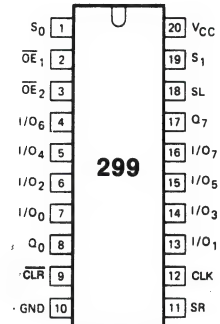
GD54/74HC299, GD54/74HCT299

8-BIT 3-STATE UNIVERSAL SHIFT REGISTER

General Description

These devices are identical in pinout to the 54/74LS299. They feature multiplexed parallel input/output data ports to achieve full 8-bit handling in a 20 pin package. Two mode-select inputs and two output-enable inputs are used to choose the five distinctive modes of operation; hold, shift-right, shift left, load, and clear. Synchronous parallel loading is accomplished by taking both mode select inputs high. This places the 3-state outputs in a high impedance state, which permits data applied to the input/output lines to be clocked into the register. Reading out of the register can be done while the outputs are enabled in any mode. Direct overriding clear is asynchronous and active-low. These devices are characterized for operation over wide temperature ranges to meet industry and military specifications.

Pin Configuration



Suffix-Blank : Plastic Dual In Line Package
 Suffix-J : Ceramic Dual In Line Package
 Suffix-D : Small Outline Package

Features

- Low Power consumption characteristic of CMOS devices
- Output drive capability: 15LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts
for HCT 4.5 to 5.5 volts
- Low input current: 1μA Max.
- Low quiescent current: 80μA Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs

Function Table

INPUTS				RESPONSE
CLR	S ₁	S ₀	CLK	
L	X	X	X	asynchronous reset; Q ₀ -Q ₇ =LOW
H	H	H	↑	parallel load; I/O _n →Q _n
H	L	H	↑	shift right; SR→Q ₀ , Q ₀ →Q ₁ etc.
H	H	L	↑	shift left; SL→Q ₇ , Q ₇ →Q ₆ etc.
H	L	L	X	hold

H = HIGH voltage level
 L = LOW voltage level
 X = don't care
 ↑ = LOW-to-HIGH CLK transition

Logic Diagram

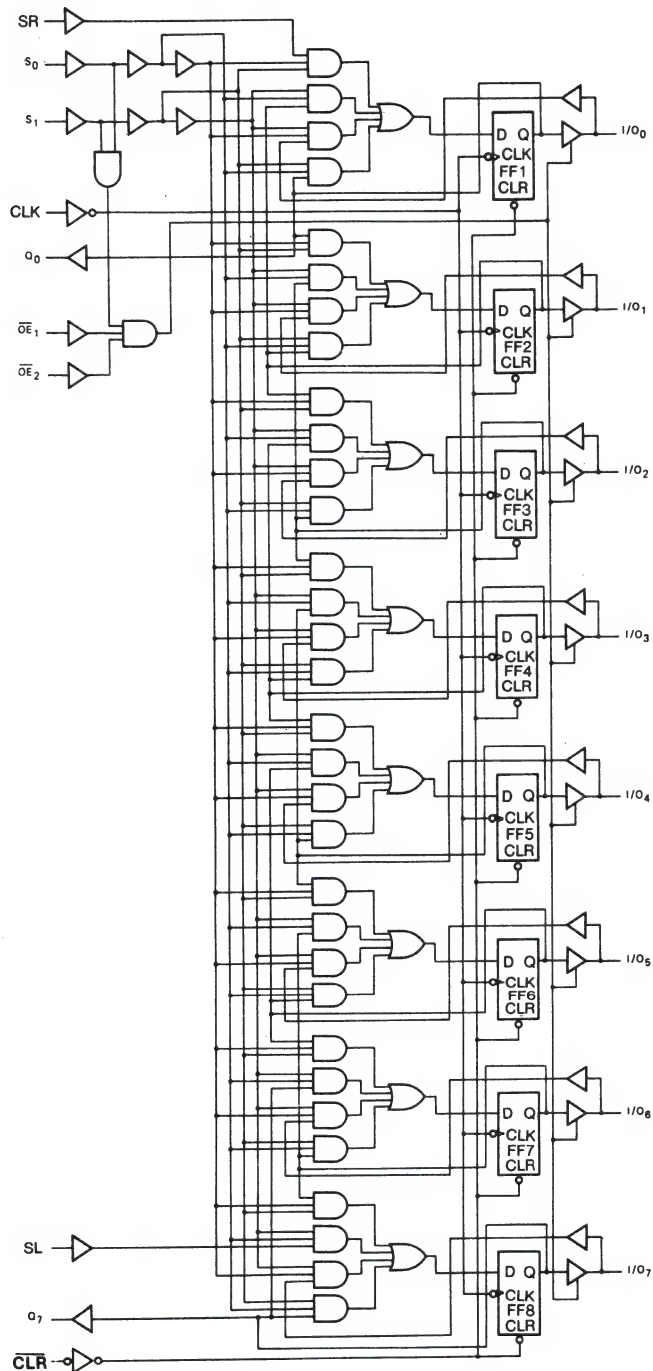


Fig. 1 Logic diagram

Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC Supply voltage		-0.5	+7	V
I_{IK}, I_{OK}	DC input or output diode current	for $V_I < -0.5$ or $V_I > V_{CC} + 0.5V$		20	mA
I_O	DC output source or sink current	for $-0.5V < V_O < V_{CC} + 0.5V$		35	mA
I_{CC}	DC V_{CC} or GND current			70	mA
T_{stg}	Storage temperature range		-65	150	°C
P_D	Power dissipation per package	above +70°C: derate linearly with 8mW/K		500	mW
T_L	Lead temperature	At distance $1/16 \pm 1/32$ in. from case for 60 sec(CERAMIC) 10 sec(PLASTIC)		300 260	°C

Recommended Operating Conditions

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range V_{CC} : GD54/74HC Types GD54/74HCT Types	2 4.5	6 5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A : GD74 Types GD54 Types	-40 -55	+85 +125	°C
Input Rise and Fall times t_r, t_f : GD54/74HC Types at 2V at 4.5V at 6V GD54/74HCT Types at 4.5 V		1000 500 400 500	ns

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HC299		GD54HC299		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2		1.5 3.15 4.2		V
V _{IL}	LOW level input voltage		2.0 4.5 6.0			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH} or V _{IL}	I _{OH} =-20μA I _{OH} =-6mA I _{OH} =-7.8mA	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0	1.9 4.4 5.9		1.9 4.4 5.9		V
V _{OL}	LOW level output voltage	V _{IN} =V _{IH} or V _{IL}	I _{OL} =20μA I _{OL} =6mA I _{OL} =7.8mA	2.0 4.5 6.0		0.1 0.1 0.1	0.1 0.1 0.1		0.1 0.1 0.1		V
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	6.0			0.1		1.0		1.0	μA
I _{OZ}	Three-State leakage current	V _{IN} =V _{IH} or V _{IL} V _O =V _{CC} or GND	6.0		0.01	0.5		5.0		10.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	6.0			8		80		160	μA

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HCT299		GD54HCT299		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		4.5 to 5.0	2.0			2.0		2.0		V
V _{IL}	LOW level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH} or V _{IL}	I _{OH} =-20μA I _{OH} =-6mA	4.5	4.4	4.5	4.4		4.4		V
V _{OL}	LOW level output voltage	V _{IN} =V _{IH} or V _{IL}	I _{OL} =20μA I _{OL} =6mA	4.5		0.1	0.1		0.1		V
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	5.5			0.1		1.0		1.0	μA
I _{OZ}	Three-State leakage current	V _{IN} =V _{IH} or V _{IL} V _O =V _{CC} or GND	5.5		0.01	0.5		5.0		10.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	5.5			8		80		160	μA

Timing Requirements for HC: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER		V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HC299		GD54HC299		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_w	Pulse width	CLK	2.0	100			145		175		ns
			4.5	20			29		35		
			6.0	17			25		30		
		$\overline{\text{CLR}}$ low	2.0	100			125		150		ns
			4.5	20			25		30		
			6.0	17			21		26		
t_{su}	Setup time	S_n to CLK	2.0	150			190		225		ns
			4.5	30			38		45		
			6.0	25			32		38		
		SR, SL to CLK	2.0	75			95		110		ns
			4.5	15			19		22		
			6.0	13			16		19		
t_{rec}	Recovery time	$\overline{\text{CLR}}$ to CLK	2.0	75			95		110		ns
			4.5	15			19		22		
			6.0	13			16		19		
t_h	Hold time	S_n , SR, SL to CLK	2.0	0			0		0		ns
			4.5	0			0		0		
			6.0	0			0		0		

AC Characteristics for HC $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER		V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HC299		GD54HC299		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
f_{max}	Maximum clock Pulse Frequency		2.0	5	13		4		3.3		MHz
			4.5	25	39		20		17		
			6.0	29	46		24		19		
$t_{PLH}/$ t_{PHL}	Propagation Delay Time CLK to Q_0 , or Q_7		2.0		35	90		150		190	ns
			4.5		11	27		38		45	
			6.0		9	25		35		42	
$t_{PLH}/$ t_{PHL}	Propagation Delay Time CLK to I/O_n		2.0		40	95		155		195	ns
			4.5		14	32		42		52	
			6.0		12	29		39		46	
$t_{PZH}/$ t_{PZL}	3-State Output Enable Time \overline{OE}_n to I/O_n		2.0		50	100		170		240	ns
			4.5		15	35		45		52	
			6.0		12	32		42		49	
$t_{PZH}/$ t_{PZL}	3-State Output Enable Time S_n to I/O_n		2.0		55	105		170		230	ns
			4.5		17	37		47		54	
			6.0		14	34		44		51	
$t_{PLZ} /$ t_{PHZ}	3-State Output Disable Time \overline{OE}_n to I/O_n		2.0		60	120		190		230	ns
			4.5		20	39		49		56	
			6.0		17	36		46		53	
$t_{PLZ} /$ t_{PHZ}	3-State Output Disable Time S_n to I/O_n		2.0		65	130		190		230	ns
			4.5		22	42		52		53	
			6.0		19	39		49		55	
t_{PHL}	Propagation Delay Time $\overline{\text{CLR}}$ to Q_0 , or Q_7 .		2.0		40	95		155		195	ns
			4.5		13	32		42		49	
			6.0		11	29		39		43	
t_{PHL}	Propagation Delay Time $\overline{\text{CLR}}$ to I/O_n		2.0		55	105		175		225	ns
			4.5		16	37		47		52	
			6.0		14	34		44		50	
$t_{TLH}/$ t_{THL}	Output Transition Time		2.0		38	75		95		110	ns
			4.5		7	15		19		22	
			6.0		6	13		16		19	

Timing Requirements for HCT: $t_r = t_f = 6\text{ns}$ $C_L = 50\text{ pF}$

SYMBOL	PARAMETER		V _{CC} (V)	T _A = 25°C			GD74HCT299		GD54HCT299		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t _w	Pulse width	CLK	4.5	20			29		35		ns
		$\overline{\text{CLR}}$ low	4.5	20			25		30		ns
t _{su}	Setup time	Sn to CLK	4.5	30			38		45		ns
		SR, SL to CLK	4.5	15			19		22		ns
t _{rec}	Recovery time	$\overline{\text{CLR}}$ to CLK	4.5	15			19		22		ns
t _h	Hold time	Sn, SR, SL to CLK	4.5	0			0		0		ns

AC Characteristics for HCT: $t_r = t_f = 6\text{ns}$ $C_L = 50\text{ pF}$

SYMBOL	PARAMETER		V _{CC} (V)	T _A = 25°C			GD74HCT299		GD54HCT299		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
f _{max}	Maximum Clock Pulse Frequency		4.5	23	37		19		15		MHz
t _{PLH} / t _{PHL}	Propagation Delay Time CLK to Q ₀ , or Q ₇		4.5		16	32		43		50	ns
t _{PLH} / t _{PHL}	Propagation Delay Time CLK to I/O _n		4.5		19	37		47		54	ns
t _{PZH} / t _{PZL}	3-State Output Enable Time $\overline{\text{OE}}_n$ to I/O _n		4.5		20	40		50		57	ns
t _{PZH} / t _{PZL}	3-State Output Enable Time S _n to I/O _n		4.5		22	42		52		59	ns
t _{PLZ} / t _{PHZ}	3-State Output Disable Time $\overline{\text{OE}}_n$ to I/O _n		4.5		25	45		54		62	ns
t _{PLZ} / t _{PHZ}	3-State Output Disable Time S _n to I/O _n		4.5		27	47		57		62	ns
t _{PHL}	Propagation Delay Time $\overline{\text{CLR}}$ to Q ₀ , or Q ₇		4.5		18	37		47		54	ns
t _{PHL}	Propagation Delay Time $\overline{\text{CLR}}$ to I/O _n		4.5		21	42		52		59	ns
t _{TLH} / t _{THL}	Output Transition Time		4.5		7	15		19		22	ns

AC Waveforms

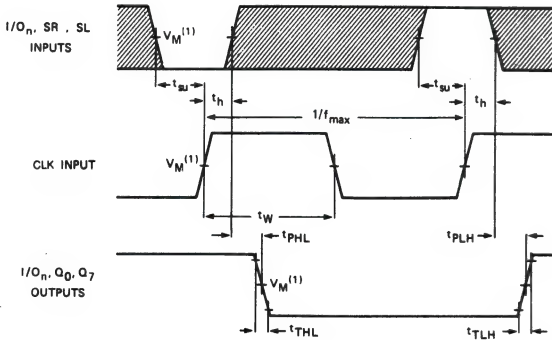


Fig. 2 Waveforms showing the clock (CLK) to output (I/O_n, Q₀, Q₇) propagation delays, the clock pulse width, the I/O_n, SR, and SL to CLK set-up and hold times, the output transition times and the maximum clock frequency.

Note to Fig. 2

The shaded areas indicate when the input is permitted to change for predictable output performance.

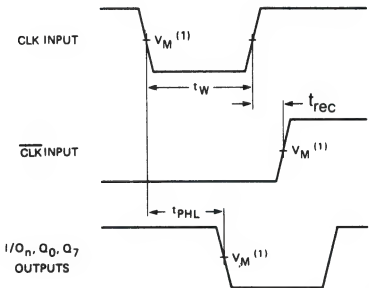


Fig. 3 Waveforms showing the master clear (\overline{CLR}) pulse width (LOW), the master to output (I/O_n, Q₀, Q₇) propagation delays and the CLR to clock (CLK) recovery time.

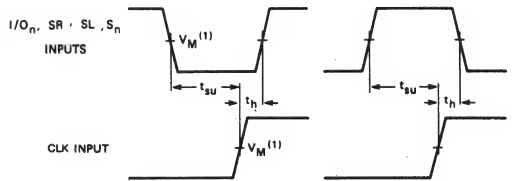


Fig. 4 Waveforms showing the set-up and hold times from the mode control inputs (S₀, S₁) to the clock (CLR).

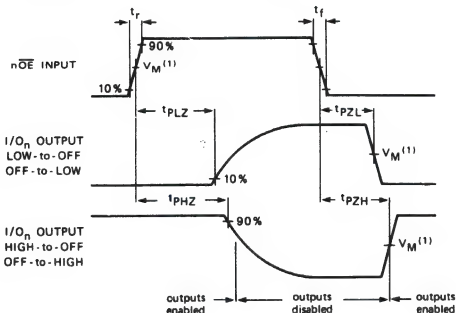


Fig. 5 Waveforms showing the 3-state enable and disable times for \overline{OE}_n inputs.

Note to AC waveforms

- (1) HC : $V_M = 50\%$; $V_I = GND$ to V_{CC} .
- HCT : $V_M = 1.3V$; $V_I = GND$ to $3V$.

GD54/74HC322, GD54/74HCT322

8-BIT 3-STATE SHIFT REGISTER WITH SIGN EXTEND

General Description

These devices are identical in pinout to the 54/74LS322. This circuit features multiplexed parallel input/output data ports to achieve full 8-bit handling in a 20 pin package. Serial data may be entered into the shift register through either of the data inputs as selected by the data select input. A serial output is also provided to facilitate expansion. Synchronous parallel loading can also be accomplished. This places the 3-state input/output ports in the data input mode, data are entered on the rising edge of the clock. The data extend function repeats the sign in the Q_A flip-flop during shifting, direct overring clear input clears the internal registers when low whether the outputs are enabled or off.

Features

- Low Power consumption characteristic of CMOS devices
- Output drive capability: 15LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts
for HCT 4.5 to 5.5 volts
- Low input current: $1\mu A$ Max.
- Low quiescent current: $80\mu A$ Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs

Function Table

OPERATION	INPUTS							INPUTS/OUTPUTS				OUTPUT
	CLR	\bar{G}	S/ \bar{P}	SE	DS	\bar{OE}	CLK	A/ Q_A	B/ Q_B	C/ Q_C	H/ Q_H	
Clear	L	X	X	X	X	L	X	L	L	L	L	L
	L	X	H	X	X	X	X	L	L	L	L	L
Hold	H	H	X	X	X	L	X	Q_{AO}	Q_{BO}	Q_{CO}	Q_{HO}	Q_{HO}
Shift Right	H	L	H	H	L	L	↑	D0	Q_{An}	Q_{Bn}	Q_{Gn}	Q_{Gn}
	H	L	H	H	H	L	↑	D1	Q_{An}	Q_{Bn}	Q_{Gn}	Q_{Gn}
Sign Extend	H	L	H	L	X	L	↑	Q_{An}	Q_{An}	Q_{Bn}	Q_{Gn}	Q_{Gn}
Load	H	L	L	X	X	X	↑	a	b	c	h	h

When the output enable is high, the eight input/output terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected. If both the register enable input and the S/ \bar{P} are low while the clear input is low, the register is cleared while the eight input/output terminals are disabled to the high-impedance state.

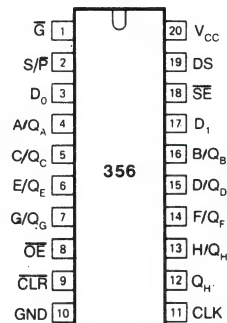
$Q_{AO} \dots Q_{HO}$ = the level of Q_A through Q_H , respectively, before the indicated steady-state conditions were established.

$Q_{An} \dots Q_{Hn}$ = the level of Q_A through Q_H , respectively, before the most recent ↑ transition of the clock.

D_0, D_1 = the level of steady-state inputs D_0 and D_1 , respectively

a...h = the level steady-state inputs at inputs A through H respectively

Pin Configuration



Suffix-Blank : Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package
Suffix-D : Small Outline Package

Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC Supply voltage		-0.5	+7	V
I_{IK}, I_{OK}	DC input or output diode current	for $V_I < -0.5$ or $V_I > V_{CC} + 0.5V$		20	mA
I_O	DC output source or sink current	for $-0.5V < V_O < V_{CC} + 0.5V$		35	mA
I_{CC}	DC V_{CC} or GND current			70	mA
T_{stg}	Storage temperature range		-65	150	°C
P_D	Power dissipation per package	above +70°C: derate linearly with 8mW/K		500	mW
T_L	Lead temperature	At distance 1/16 ± 1/32 in. from case for 60 sec(CERAMIC) 10 sec(PLASTIC)		300 260	°C

Recommended Operating Conditions

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range V_{CC} : GD54/74HC Types GD54/74HCT Types	2 4.5	6 5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A : GD74 Types GD54 Types	-40 -55	+85 +125	°C
Input Rise and Fall times t_r, t_f : GD54/74HC Types at 2V at 4.5V at 6V GD54/74HCT Types at 4.5V		1000 500 400 500	ns

Logic Diagram

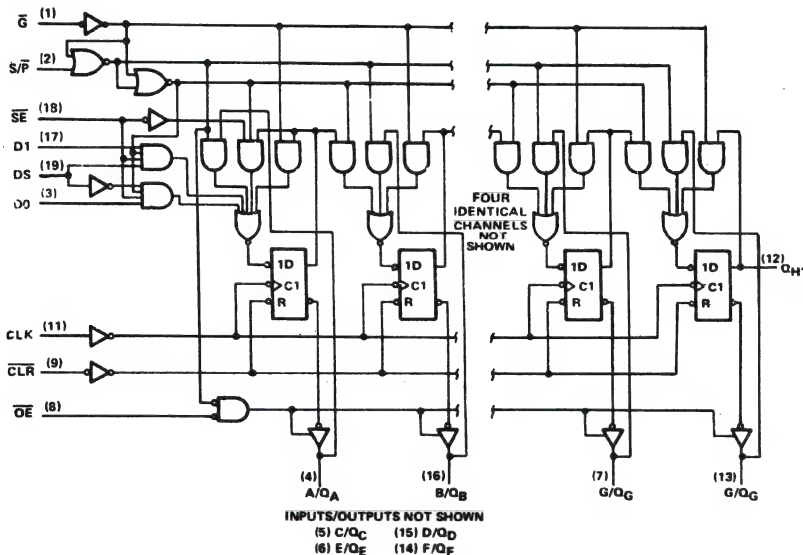


Fig. 1 Logic diagram

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A = 25°C			GD74HC322		GD54HC322		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2		1.5 3.15 4.2		V
V _{IL}	LOW level input voltage		2.0 4.5 6.0			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V
V _{OH}	HIGH level output voltage	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -20μA	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9	V
			I _{OH} = -6mA I _{OH} = -7.8mA	4.5 6.0	3.98 5.48	4.3 5.2		3.84 5.34		3.7 5.2	
		V _{IN} = V _{IH} or V _{IL}	I _{OL} = 20μA	2.0 4.5 6.0			0.1 0.1 0.1	0.1 0.1 0.1		0.1 0.1 0.1	V
			I _{OL} = 6mA I _{OL} = 7.8mA	4.5 6.0		0.17 0.15	0.26 0.26	0.33 0.33		0.4 0.4	
I _{IN}	Input leakage Current	V _{IN} = V _{CC} or GND	6.0			0.1		1.0		1.0	μA
I _{OZ}	Three-State leakage current	V _{IN} = V _{IH} or V _{IL} V _O = V _{CC} or GND	6.0		0.01	0.5		5.0		10.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} = V _{CC} or GND I _{out} = 0μA	6.0			8		80		160	μA

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A = 25°C			GD74HCT322		GD54HCT322		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		4.5 to 5.0	2.0			2.0		2.0		V
V _{IL}	LOW level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V _{OH}	HIGH level output voltage	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -20μA	4.5	4.4	4.5		4.4		4.4	V
			I _{OH} = -6mA	4.5	3.98	4.3		3.84		3.7	
V _{OL}	LOW level output voltage	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 20μA	4.5			0.1	0.1		0.1	V
			I _{OL} = 6mA	4.5		0.17	0.26	0.33		0.4	
I _{IN}	Input leakage Current	V _{IN} = V _{CC} or GND	5.5			0.1		1.0		1.0	μA
I _{OZ}	Three-State leakage current	V _{IN} = V _{IH} or V _{IL} V _O = V _{CC} or GND	5.5		0.01	0.5		5.0		10.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} = V _{CC} or GND I _{out} = 0μA	5.5			8		80		160	μA

Timing Requirements for HC: $t_r = t_f = 6\text{ns}$ $C_L = 50\text{ pF}$

SYMBOL	PARAMETER		V_{CC} (V)	$T_A = 25^\circ\text{C}$			GD74HC322		GD54HC322		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_w	Pulse width	CLK high	2.0	200			250		300		ns
			4.5	40			50		60		
			6.0	34			43		51		
		CLK low	2.0	100			125		150		ns
			4.5	20			25		30		
			6.0	17			21		26		
t_{su}	Setup-time	DS to CLK	2.0	100			125		150		ns
			4.5	20			20		30		
			6.0	17			21		26		
		Data to CLK	2.0	150			190		225		ns
			4.5	30			38		45		
			6.0	26			32		38		
t_{rec}	Recovery time	$\overline{\text{CLR}}$ to CLK	2.0	150			190		225		ns
			4.5	30			38		45		
			6.0	26			32		38		
t_h	Hold time	CLK to DS	2.0	75			95		115		ns
			4.5	15			19		23		
			6.0	13			16		20		
		CLK to Data	2.0	0			0		0		ns
			4.5	0			0		0		
			6.0	0			0		0		

AC Characteristics for HC: $t_r = t_f = 6\text{ns}$ $C_L = 50\text{ pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A = 25^\circ\text{C}$			GD74HC322		GD54HC322		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
f_{max}	Maximum Clock Pulse Frequency	2.0	3.3	6		2.7		2.2		MHz
		4.5	17	35		13		11		
		6.0	20	20		16		13		
$t_{PLH}/$ t_{PHL}	Propagation Delay Time CLK to Q_H	2.0		90	120		190		230	ns
		4.5		28	37		45		52	
		6.0		24	33		41		48	
$t_{PLH}/$ t_{PHL}	Propagation Delay Time $\overline{\text{CLR}}$ to Q_H	2.0		90	120		190		230	ns
		4.5		28	37		45		52	
		6.0		24	33		41		48	
$t_{PLH}/$ t_{PHL}	Propagation Delay Time CLK to Q_A Thru Q_H	2.0		80	110		180		220	ns
		4.5		22	31		39		47	
		6.0		19	27		35		42	
$t_{PLH}/$ t_{PHL}	Propagation Delay Time $\overline{\text{CLR}}$ to Q_A Thru Q_H	2.0		80	110		180		220	ns
		4.5		22	31		39		47	
		6.0		19	27		35		42	
$t_{PZL}/$ t_{PZH}	3-state Output Enable Time $\overline{\text{OE}}$ to Q_A Thru Q_H	2.0		55	95		175		215	ns
		4.5		17	26		35		42	
		6.0		14	23		32		39	
$t_{PLZ}/$ t_{PHZ}	3-state Output Disable Time $\overline{\text{OE}}$ to Q_A Thru Q_H	2.0		55	95		175		215	ns
		4.5		17	26		35		42	
		6.0		14	23		32		39	
$t_{TLH}/$ t_{THL}	Output Transition Time	2.0		38	75		95		110	ns
		4.5		7	15		19		22	
		6.0		6	13		16		19	

Timing Requirements for HCT: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER		V _{CC} (V)	T _A =25°C			GD74HCT322		GD54HCT322		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t _w	Pulse width	CLK high	4.5	40			50		60		ns
		CLK low	4.5	20			25		30		ns
		$\overline{\text{CLR}}$ low	4.5	30			38		45		ns
t _{su}	Setup time	DS to CLK	4.5	20			20		30		ns
		Data to CLK	4.5	30			38		45		ns
t _{rec}	Recovery time	$\overline{\text{CLR}}$ to CLK	4.5	30			38		45		ns
t _h	Hold time	CLK to DS	4.5	15			19		23		ns
		CLK to Data	4.5	0			0		0		ns

AC Characteristics for HCT: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER	V _{CC} (V)	T _A =25°C			GD74HCT322		GD54HCT322		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
f _{max}	Maximum Clock Pulse Frequency	4.5	15	33		12		10		MHz
t _{PLH} / t _{PHL}	Propagation Delay Time CLK to Q _H	4.5		32	41		50		57	ns
t _{PLH} / t _{PHL}	Propagation Delay Time $\overline{\text{CLR}}$ to Q _H	4.5		32	41		50		57	ns
t _{PLH} / t _{PHL}	Propagation Delay Time CLK to Q _A thru Q _H	4.5		26	36		44		52	ns
t _{PLH} / t _{PHL}	Propagation Delay Time $\overline{\text{CLR}}$ to Q _A thru Q _H	4.5		26	36		44		52	ns
t _{PZL} / t _{PZH}	3-state Output Enable Time $\overline{\text{OE}}$ to Q _A thru Q _H	4.5		21	30		39		47	ns
t _{PLZ} / t _{PHZ}	3-state Output Disable Time $\overline{\text{OE}}$ to Q _A thru Q _H	4.5		21	30		39		47	ns
t _{TLH} / t _{THL}	Output Transition Time	4.5		7	15		19		22	ns

AC Waveforms

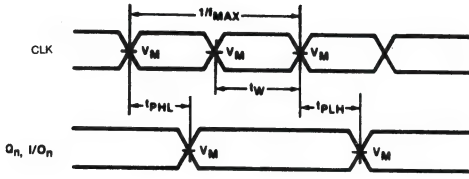


Fig 2. Clock To Output Delays And Clock Pulse Width

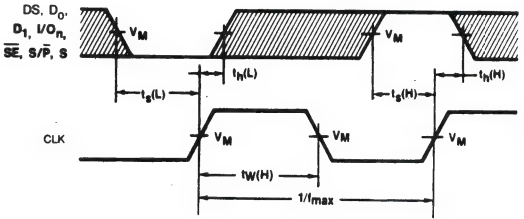


Fig 3. Data Set-up And Hold Times

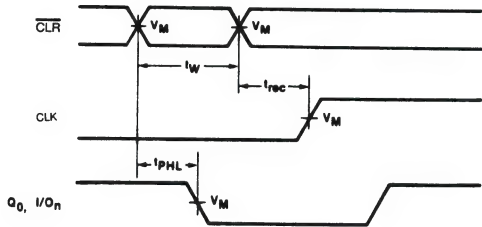


Fig 4. Master clear Pulse Width, Master Clear To Output Delay And Master Clear To Clock Recovery Time

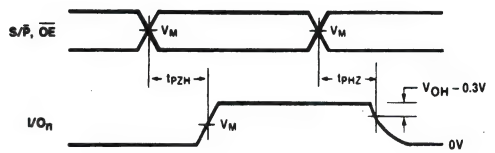


Fig 5. 3-State Output Enable Time to HIGH Level And Output Disable Time From HIGH Level

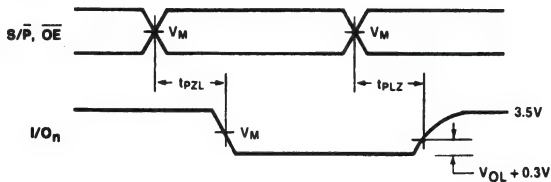


Fig 6. 3-State Output Enable Time To LOW Level And Output Disable Time From LOW Level

NOTE: For all waveforms, $V_M = 1.5V$.

The shaded areas indicate when the input is permitted to change for predictable output performance.

Note to AC waveforms

- (1) HC : $V_M = 50\%$; $V_I = GND$ to V_{CC} .
HCT : $V_M = 1.3V$; $V_I = GND$ to $3V$.

GD54/74HC354, GD54/74HCT354

DUAL 4-TO-1 LINE MULTIPLEXERS WITH LATCHES & 3-STATE OUTPUTS

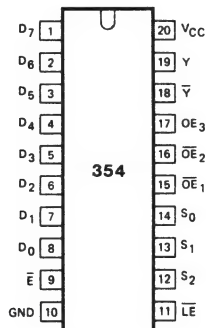
General Description

These devices are identical in pinout to the 54/74LS354. They contain full on-chip binary decoding to select one of eight data sources, determined by the address inputs. The information at the data inputs is stored in the transparent 8-Bit data latch when active-low data latch enable is held low. the address information may be stored in the transparent address latch, which is enabled by the active-low address latch enable. Both true and complementary 3-state outputs are available. The HC/HCT 354 are similar in function to the HC/HCT 356 which have a clocked data latch that is not transparent.

Features

- Low Power consumption characteristic of CMOS devices
- Output drive capability: 15 LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts
for HCT 4.5 to 5.5 volts
- Low input current: 1 μ A Max.
- Low quiescent current: 80 μ A Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs

Pin Configuration



Suffix-Blank : Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package
Suffix-D : Small Outline Package

Function Table

INPUTS								OUTPUTS		DESCRIPTION
ADDRESS *			E	OUTPUT ENABLE			Y	Y̅		
S ₂	S ₁	S ₀		OE ₁	OE ₂	OE ₃				
X	X	X	X	H	X	X	Z	Z	outputs in high impedance OFF – states	
X	X	X	X	X	H	X	Z	Z		
X	X	X	X	X	X	L	Z	Z		
L	L	L	L	L	L	L	D ₀	D̄ ₀	data latch is transparent	
L	L	H	L	L	L	H	D ₁	D̄ ₁		
L	L	L	L	L	L	L	D ₂	D̄ ₂		
L	H	H	L	L	L	H	D ₃	D̄ ₃		
H	L	L	L	L	L	H	D ₄	D̄ ₄		
H	L	H	L	L	L	H	D ₅	D̄ ₅		
H	H	L	L	L	L	H	D ₆	D̄ ₆		
H	H	H	L	L	L	H	D ₇	D̄ ₇		
L	L	L	H	L	L	L	D _{0n}	D̄ _{0n}	data is latched	
L	L	H	H	L	L	H	D _{1n}	D̄ _{1n}		
L	L	L	L	L	L	L	D _{2n}	D̄ _{2n}		
L	H	H	H	L	L	H	D _{3n}	D̄ _{3n}		
H	L	L	H	L	L	H	D _{4n}	D̄ _{4n}		
H	L	H	H	L	L	H	D _{5n}	D̄ _{5n}		
H	H	L	H	L	L	H	D _{6n}	D̄ _{6n}		
H	H	H	H	L	L	H	D _{7n}	D̄ _{7n}		

D₀ to D₇=data at inputs D₀ to D₇

D_{0n} to D_{7n}=data at inputs D₀ to D₇ before the most recent

LOW-to-HIGH transition of E

* This column shows the input address set-up with LE=LOW

Logic Diagram

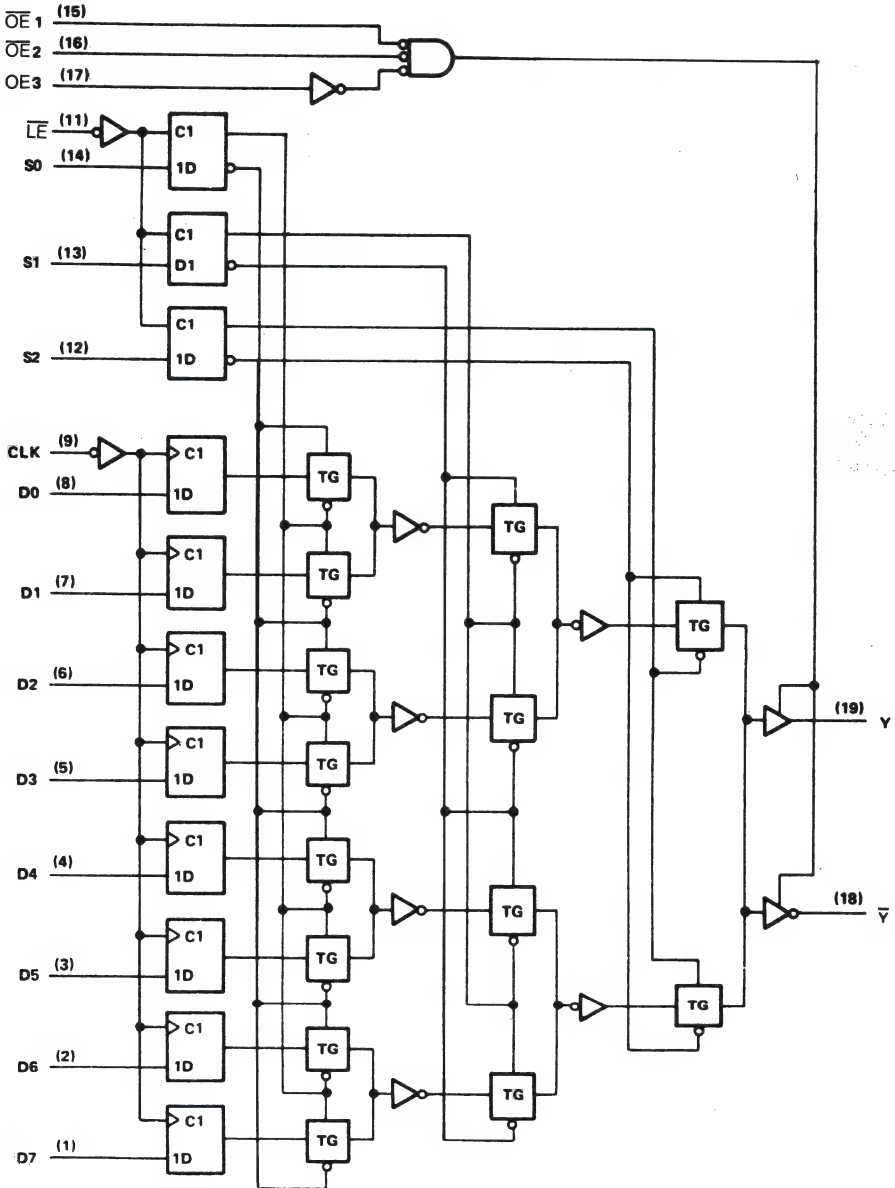


Fig. 1 Logic diagram

Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC Supply voltage		-0.5	+7	V
I_{IK}, I_{OK}	DC input or output diode current	for $V_I < -0.5$ or $V_I > V_{CC} + 0.5V$		20	mA
I_O	DC output source or sink current	for $-0.5V < V_O < V_{CC} + 0.5V$		35	mA
I_{CC}	DC V_{CC} or GND current			70	mA
T_{stg}	Storage temperature range		-65	150	°C
P_D	Power dissipation per package	above +70°C: derate linearly with 8mW/K		500	mW
T_L	Lead temperature	At distance 1/16 ± 1/32 in. from case for 60 sec(CERAMIC) 10 sec(PLASTIC)		300 260	°C

Recommended Operating Conditions

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range V_{CC} : GD54/74HC Types GD54/74HCT Types	2 4.5	6 5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A : GD74 Types GD54 Types	-40 -55	+85 +125	°C
Input Rise and Fall times t_r, t_f : GD54/74HC Types at 2V at 4.5V at 6V GD54/74HCT Types at 4.5 V		1000 500 400 500	ns

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HC354		GD54HC354		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2		1.5 3.15 4.2		V
V _{IL}	LOW level input voltage		2.0 4.5 6.0			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH} or V _{IL}	I _{OH} =-20μA	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0	1.9 4.4 5.9		1.9 4.4 5.9		V
			I _{OH} =-6mA	4.5 6.0	3.98 5.48	4.3 5.2	3.84 5.34		3.7 5.2		
			I _{OH} =-7.8mA								
V _{OL}	LOW level output voltage	V _{IN} =V _{IH} or V _{IL}	I _{OL} =20μA	2.0 4.5 6.0			0.1 0.1 0.1	0.1 0.1 0.1		0.1 0.1 0.1	V
			I _{OL} =6mA	4.5 6.0		0.17 0.15	0.26 0.26	0.33 0.33		0.4 0.4	
			I _{OL} =7.8mA								
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	6.0			0.1		1.0		1.0	μA
I _{OZ}	Three-State leakage current	V _{IN} =V _{IH} or V _{IL} V _O =V _{CC} or GND	6.0		0.01	0.5		5.0		10.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	6.0			8		80		160	μA

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HCT354		GD54HCT354		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		4.5 to 5.0	2.0			2.0		2.0		V
V _{IL}	LOW level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH} or V _{IL}	I _{OH} =-20μA	4.5	4.4	4.5	4.4		4.4		V
			I _{OH} =-6mA	4.5	3.98	4.3	3.84		3.7		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH} or V _{IL}	I _{OL} =20μA	4.5			0.1	0.1		0.1	V
			I _{OL} =6mA	4.5		0.17	0.26	0.33		0.4	
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	5.5			0.1		1.0		1.0	μA
I _{OZ}	Three-State leakage current	V _{IN} =V _{IH} or V _{IL} V _O =V _{CC} or GND	5.5		0.01	0.5		5.0		10.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	5.5			8		80		160	μA

Timing Requirements for HC: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER		V_{CC}	$T_A=25^\circ\text{C}$			GD74HC354		GD54HC354		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{su}	Setup time	data before DS \uparrow	2.0 4.5 6.0	75 15 13			95 19 16		115 23 20		ns
t_h	Hold time	data after DS \uparrow	2.0 4.5 6.0	5 5 5			5 5 5		5 5 5		ns

AC Characteristics for HC: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER	V_{CC}	$T_A=25^\circ\text{C}$			GD74HC354		GD54HC354		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
$t_{PLH}/$ t_{PHL}	Propagation Delay Time D_n to Y	2.0 4.5 6.0		75 25 21						ns
$t_{PLH}/$ t_{PHL}	Propagation Delay Time D_n to \bar{Y}	2.0 4.5 6.0		80 26 22						ns
$t_{PLH}/$ t_{PHL}	Propagation Delay Time \bar{E} to Y	2.0 4.5 6.0		80 26 22						ns
$t_{PLH}/$ t_{PHL}	Propagation Delay Time \bar{E} to \bar{Y}	2.0 4.5 6.0		80 26 22						ns
$t_{PLH}/$ t_{PHL}	Propagation Delay Time S_n to Y	2.0 4.5 6.0		90 30 25						ns
$t_{PLH}/$ t_{PHL}	Propagation Delay Time S_n to \bar{Y}	2.0 4.5 6.0		85 28 24						ns
$t_{PLH}/$ t_{PHL}	Propagation Delay Time $\bar{L}\bar{E}$ to Y	2.0 4.5 6.0		90 30 25						ns
$t_{PLH}/$ t_{PHL}	Propagation Delay Time $\bar{L}\bar{E}$ to \bar{Y}	2.0 4.5 6.0		90 28 24						ns
$t_{PZL}/$ t_{PZH}	3-State Output Enable Time \bar{OE}_1, \bar{OE}_2 to Y	2.0 4.5 6.0		72 22 18						ns
$t_{PZL}/$ t_{PZH}	3-State Output Enable Time \bar{OE}_1, \bar{OE}_2 to \bar{Y}	2.0 4.5 6.0		70 23 19						ns
$t_{PHZ}/$ t_{PLZ}	3-State Output Disable Time \bar{OE}_1, \bar{OE}_2 to Y	2.0 4.5 6.0		40 14 12						ns
$t_{PHZ}/$ t_{PLZ}	3-State Output Disable Time \bar{OE}_1, \bar{OE}_2 to \bar{Y}	2.0 4.5 6.0		40 14 12						ns
$t_{PZL}/$ t_{PZH}	3-State Output Enable Time OE_3 to Y	2.0 4.5 6.0		70 22 18						ns
$t_{PZL}/$ t_{PZH}	3-State Output Enable Time OE_3 to \bar{Y}	2.0 4.5 6.0		70 22 18						ns
$t_{PHZ}/$ t_{PLZ}	3-State Output Disable Time OE_3 to Y	2.0 4.5 6.0		50 16 13						ns
$t_{PHZ}/$ t_{PLZ}	3-State Output Disable Time OE_3 to \bar{Y}	2.0 4.5 6.0		50 17 14						ns
$t_{TLH}/$ t_{THL}	Output Transition Time	2.0 4.5 6.0		38 7 6			75 19 16		110 22 19	ns

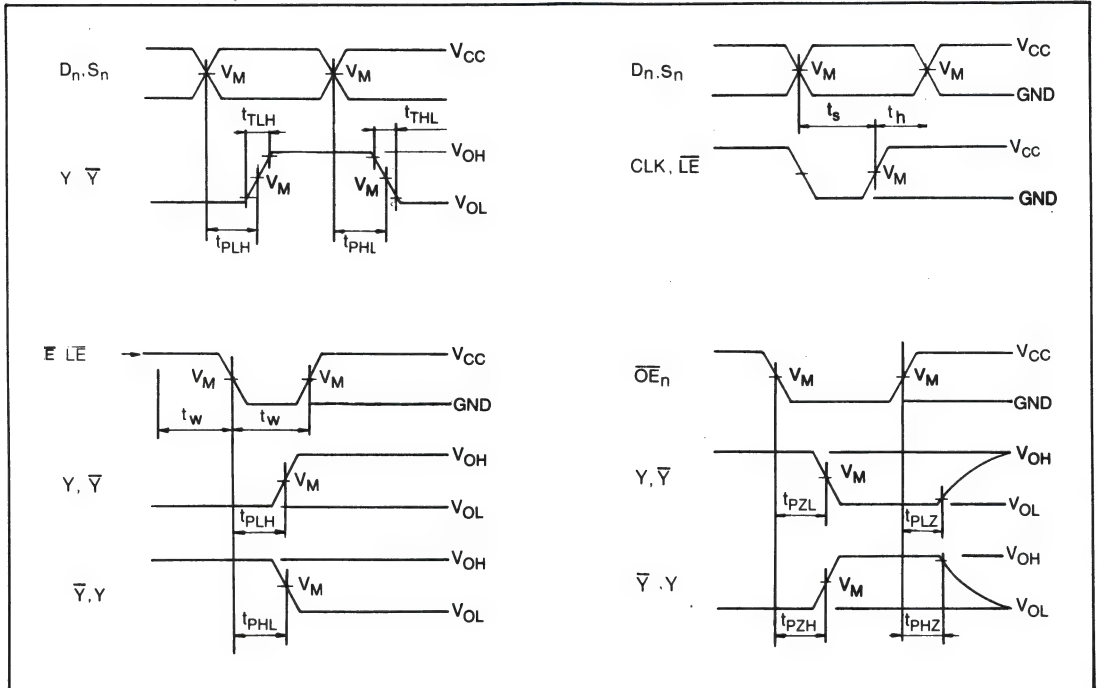
Timing Requirements for HCT: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER		V_{CC}	$T_A=25^\circ\text{C}$			GD74HCT354		GD54HCT354		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{su}	Setup time	data before DS \uparrow	4.5	15			19		23		ns
t_h	Hold time	data after DS \uparrow	4.5	5			5		5		ns

AC Characteristics for HCT: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER	V_{CC}	$T_A=25^\circ\text{C}$			GD74HCT354		GD54HCT354		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
$t_{PLH}/$ t_{PHL}	Propagation Delay Time D _n to Y	4.5		30						ns
$t_{PLH}/$ t_{PHL}	Propagation Delay Time D _n to \bar{Y}	4.5		29						ns
$t_{PLH}/$ t_{PHL}	Propagation Delay Time \bar{E} to Y	4.5		30						ns
$t_{PLH}/$ t_{PHL}	Propagation Delay Time \bar{E} to \bar{Y}	4.5		30						ns
$t_{PLH}/$ t_{PHL}	Propagation Delay Time S _n to Y	4.5		34						ns
$t_{PLH}/$ t_{PHL}	Propagation Delay Time S _n to \bar{Y}	4.5		32						ns
$t_{PLH}/$ t_{PHL}	Propagation Delay Time $\bar{L}\bar{E}$ to Y	4.5		34						ns
$t_{PLH}/$ t_{PHL}	Propagation Delay Time $\bar{L}\bar{E}$ to \bar{Y}	4.5		32						ns
$t_{PZL}/$ t_{PZH}	3-State Output Enable Time \bar{OE}_1, \bar{OE}_2 to Y	4.5		26						ns
$t_{PZL}/$ t_{PZH}	3-State Output Enable Time \bar{OE}_1, \bar{OE}_2 to \bar{Y}	4.5		27						ns
$t_{PHZ}/$ t_{PLZ}	3-State Output Disable Time \bar{OE}_1, \bar{OE}_2 to Y	4.5		18						ns
$t_{PHZ}/$ t_{PLZ}	3-State Output Disable Time \bar{OE}_1, \bar{OE}_2 to \bar{Y}	4.5		18						ns
$t_{PZL}/$ t_{PZH}	3-State Output Enable Time OE_3 to Y	4.5		26						ns
$t_{PZL}/$ t_{PZH}	3-State Output Enable Time OE_3 to \bar{Y}	4.5		26						ns
$t_{PHZ}/$ t_{PLZ}	3-State Output Disable Time OE_3 to Y	4.5		20						ns
$t_{PHZ}/$ t_{PLZ}	3-State Output Disable Time OE_3 to \bar{Y}	4.5		21						ns
$t_{TLH}/$ t_{THL}	Output Transition Time	4.5		7			19		22	ns

AC Waveforms



Note to AC waveforms

- (1) HC : $V_M = 50\%$; $V_I = \text{GND to } V_{CC}$.
HCT : $V_M = 1.3V$; $V_I = \text{GND to } 3V$.

GD54/74HC365, GD54/74HCT365

HEX 3-STATE NONINVERTING BUFFERS

General Description

These devices are identical in pinout to the 54/74LS365. They have high drive current which enable high speed operation even when driving large bus capacitances. The HC/HCT 365 and HC/HCT 367 have noninverting outputs, while the HC/HCT 366 and HC/HCT 368 have inverting outputs.

The HC/HCT 365 and HC/HCT 366 have two 3-state control inputs which are NORed together to control all 6 Gates. The HC/HCT 367 and HC/HCT 368 have two output enables, where one enable controls 4 gates and the other controls the remaining 2 gates. These devices are characterized for operation over wide temperature ranges to meet industry and military specifications.

Features

- Low Power consumption characteristic of CMOS devices
- Output drive capability: 15 LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts
for HCT 4.5 to 5.5 volts
- Low input current: $1\mu\text{A}$ Max.
- Low quiescent current: $80\mu\text{A}$ Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs

Logic Symbol

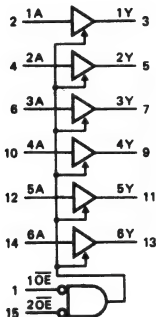
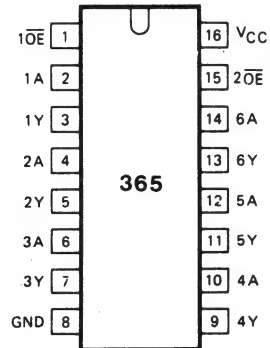


Fig. 1 Logic Symbol

Pin Configuration



Suffix-Blank : Plastic Dual In Line Package
 Suffix-J : Ceramic Dual In Line Package
 Suffix-D : Small Outline Package

Function Table

INPUTS			OUTPUT
1OE	2OE	nA	nY
L	L	L	L
L	L	H	H
X	H	X	Z
H	X	X	Z

H = HIGH voltage level

L = LOW voltage level

X = don't care

Z = high impedance OFF-state

Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC Supply voltage		-0.5	+7	V
I_{IK}, I_{OK}	DC input or output diode current	for $V_I < -0.5$ or $V_I > V_{CC} + 0.5V$		20	mA
I_O	DC output source or sink current	for $-0.5V < V_O < V_{CC} + 0.5V$		35	mA
I_{CC}	DC V_{CC} or GND current			70	mA
T_{stg}	Storage temperature range		-65	150	°C
P_D	Power dissipation per package	above +70°C: derate linearly with 8mW/K		500	mW
T_L	Lead temperature	At distance $1/16 \pm 1/32$ in. from case for 60 sec(CERAMIC) 10 sec(PLASTIC)		300 260	°C

Recommended Operating Conditions

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range V_{CC} : GD54/74HC Types GD54/74HCT Types	2 4.5	6 5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A : GD74 Types GD54 Types	-40 -55	+85 +125	°C
Input Rise and Fall times t_r, t_f : GD54/74HC Types at 2V at 4.5V at 6V GD54/74HCT Types at 4.5 V		1000 500 400 500	ns

Logic Diagram

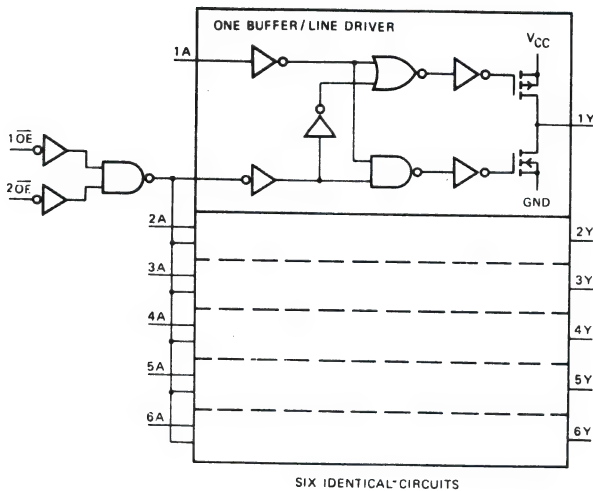


Fig. 2 Logic diagram

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HC365		GD54HC365		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2		1.5 3.15 4.2		V
V _{IL}	LOW level input voltage		2.0 4.5 6.0			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH} or V _{IL}	I _{OH} =-20μA	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0	1.9 4.4 5.9		1.9 4.4 5.9		V
			I _{OH} =-6mA	4.5 6.0	3.98 5.48	4.3 5.2	3.84 5.34		3.7 5.2		
			I _{OH} =-7.8mA	4.5 6.0	3.98 5.48	4.3 5.2	3.84 5.34		3.7 5.2		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH} or V _{IL}	I _{OL} =20μA	2.0 4.5 6.0				0.1 0.1 0.1		0.1 0.1 0.1	V
			I _{OL} =6mA	4.5 6.0		0.17 0.15	0.26 0.26		0.33 0.33	0.4 0.4	
			I _{OL} =7.8mA	4.5 6.0		0.17 0.15	0.26 0.26		0.33 0.33	0.4 0.4	
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	6.0			0.1		1.0		1.0	μA
I _{OZ}	Three-State leakage current	V _{IN} =V _{IH} or V _{IL} V _O =V _{CC} or GND	6.0		0.01	0.5		5.0		10.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	6.0			8		80		160	μA

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HCT365		GD54HCT365		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		4.5 to 5.0	2.0			2.0		2.0		V
V _{IL}	LOW level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH} or V _{IL}	I _{OH} =-20μA	4.5	4.4	4.5	4.4		4.4		V
			I _{OH} =-6mA	4.5	3.98	4.3	3.84		3.7		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH} or V _{IL}	I _{OL} =20μA	4.5			0.1		0.1		V
			I _{OL} =6mA	4.5		0.17	0.26		0.33	0.4	
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	5.5			0.1		1.0		1.0	μA
I _{OZ}	Three-State leakage current	V _{IN} =V _{IH} or V _{IL} V _O =V _{CC} or GND	5.5		0.01	0.5		5.0		10.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	5.5			8		80		160	μA

AC Characteristics for HC, $t_r = t_f = 6\text{ns}$ $C_L = 50\text{ pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A = 25^\circ\text{C}$			GD74HC365		GD54HC365		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} / t_{PHL}	Propagation Delay Time nA to nY	2.0 4.5 6.0		30 10 9	90 19 16		120 24 20		140 29 25	ns
t_{PZH} / t_{PZL}	3-state Output Enable Time \overline{nOE} to nY	2.0 4.5 6.0		40 15 12	140 30 25		180 38 32		210 45 38	ns
t_{PHZ} / t_{PLZ}	3-state Output Disable Time \overline{nOE} to nY	2.0 4.5 6.0		40 15 12	140 30 25		180 38 32		210 45 38	ns
t_{TLH} / t_{THL}	Output Transition Time	2.0 4.5 6.0		15 6 5	60 12 10		75 15 13		90 18 15	ns

AC Characteristics for HCT: $t_r = t_f = 6\text{ns}$ $C_L = 50\text{ pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A = 25^\circ\text{C}$			GD74HCT365		GD54HCT365		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} / t_{PHL}	Propagation Delay Time nA to nY	4.5		12	22		26		30	ns
t_{PZH} / t_{PZL}	3-state Output Enable Time \overline{nOE} to nY	4.5		16	32		40		46	ns
t_{PHZ} / t_{PLZ}	3-state Output Disable Time \overline{nOE} to nY	4.5		16	32		40		46	ns
t_{TLH} / t_{THL}	Output Transition Time	4.5		7	12		15		18	ns

AC Waveforms

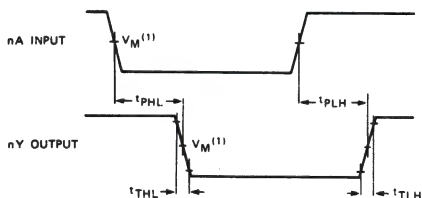


Fig. 3 Waveforms showing the input (nA) to output (nY) propagation delays and the output transition times.

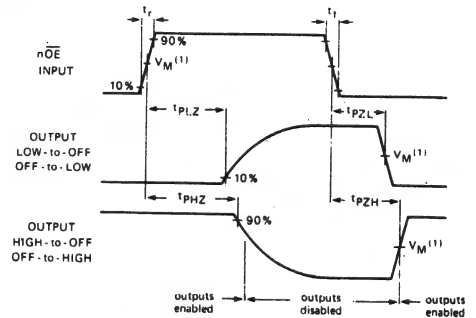


Fig. 4 Waveforms showing the 3-state enable and disable times.

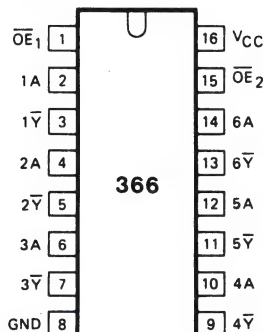
GD54/74HC366, GD54/74HCT366

HEX 3-STATE INVERTING BUFFERS

General Description

These devices are identical in pinout to the 54/74LS366. They have high drive current outputs which enable high speed operation even when driving large bus capacitances. The HC/HCT 365 and HC/HCT 367 have noninverting outputs, while The HC/HCT 366 and HC/HCT 368 have inverting outputs. The HC/HCT 365 and HC/HCT 366 have two 3-state control inputs which are NORed together to control all 6 Gates. The HC/HCT 367 and HC/HCT 368 have two output enables, where one enable controls 4 Gates and the other controls the remaining 2 Gates. These devices are Characterized for operation over wide temperature ranges to meet industry and military specifications.

Pin Configuration



Suffix-Blank : Plastic Dual In Line Package
 Suffix-J : Ceramic Dual In Line Package
 Suffix-D : Small Outline Package

Features

- Low Power consumption characteristic of CMOS devices
- Output drive capability: 15 LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts
for HCT 4.5 to 5.5 volts
- Low input current: 1μA Max.
- Low quiescent current: 80μA Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs

Function Table

INPUTS			OUTPUT
\overline{OE}_1	\overline{OE}_2	nA	nY
L	L	L	H
L	L	H	L
X	H	X	Z
H	X	X	Z

H = HIGH voltage level
 L = LOW voltage level
 X = don't care
 Z = high impedance OFF-state

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A = 25°C			GD74HC366		GD54HC366		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2		1.5 3.15 4.2		V
V _{IL}	LOW level input voltage		2.0 4.5 6.0			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V
V _{OH}	HIGH level output voltage	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -20μA	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0	1.9 4.4 5.9		1.9 4.4 5.9		V
			I _{OH} = -6mA	4.5	3.98	4.3	3.84		3.7		
			I _{OH} = -7.8mA	6.0	5.48	5.2	5.34		5.2		
V _{OL}	LOW level output voltage	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 20μA	2.0 4.5 6.0			0.1 0.1 0.1	0.1 0.1 0.1		0.1 0.1 0.1	V
			I _{OL} = 6mA	4.5		0.17	0.26	0.33		0.4	
			I _{OL} = 7.8mA	6.0		0.15	0.26	0.33		0.4	
I _{IN}	Input leakage Current	V _{IN} = V _{CC} or GND	6.0			0.1		1.0		1.0	μA
I _{OZ}	Three-State leakage current	V _{IN} = V _{IH} or V _{IL} V _O = V _{CC} or GND	6.0		0.01	0.5		5.0		10.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} = V _{CC} or GND I _{out} = 0μA	6.0			8		80		160	μA

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A = 25°C			GD74HCT366		GD54HCT366		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		4.5 to 5.0	2.0			2.0		2.0		V
V _{IL}	LOW level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V _{OH}	HIGH level output voltage	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -20μA	4.5	4.4	4.5	4.4		4.4		V
			I _{OH} = -6mA	4.5	3.98	4.3	3.84		3.7		
V _{OL}	LOW level output voltage	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 20μA	4.5		0.1	0.1		0.1		V
			I _{OL} = 6mA	4.5		0.17	0.26		0.33		
I _{IN}	Input leakage Current	V _{IN} = V _{CC} or GND	5.5			0.1		1.0		1.0	μA
I _{OZ}	Three-State leakage current	V _{IN} = V _{IH} or V _{IL} V _O = V _{CC} or GND	5.5		0.01	0.5		5.0		10.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} = V _{CC} or GND I _{out} = 0μA	5.5			8		80		160	μA

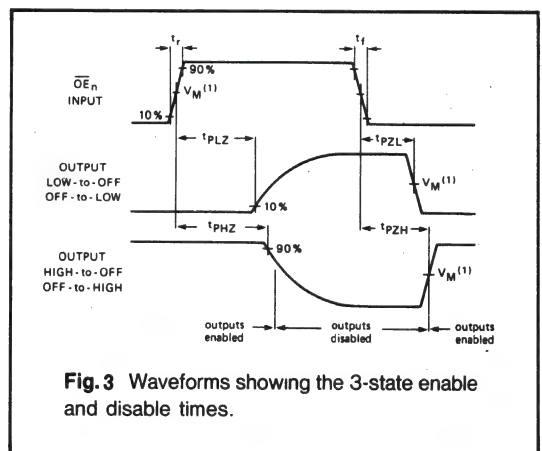
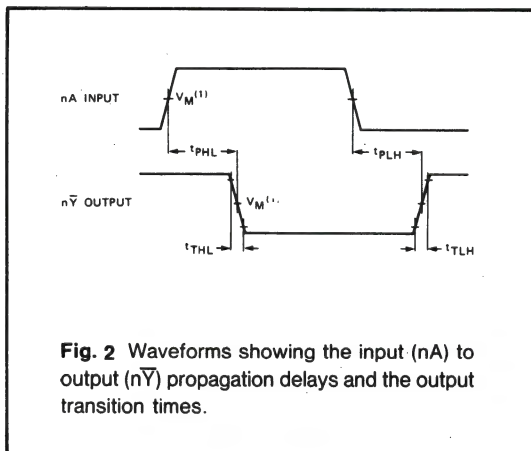
AC Characteristics for HC, $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HC366		GD54HC366		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} / t_{PHL}	Propagation Delay Time nA to $n\bar{Y}$	2.0 4.5 6.0		28 9 8	85 18 16		110 23 20		130 28 25	ns
t_{PZH} / t_{PZL}	3-state Output Enable Time \overline{OE}_n to $n\bar{Y}$	2.0 4.5 6.0		40 15 12	140 30 25		180 38 32		210 45 38	ns
t_{PLZ} / t_{PHZ}	3-state Output Disable Time \overline{OE}_n to $n\bar{Y}$	2.0 4.5 6.0		40 15 12	140 30 25		180 38 32		210 45 38	ns
t_{TLH} / t_{THL}	Output Transition Time	2.0 4.5 6.0		15 6 5	60 12 10		75 15 13		90 18 15	ns

AC Characteristics for HCT, $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HCT366		GD54HCT366		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} / t_{PHL}	Propagation Delay Time nA to $n\bar{Y}$	4.5		12	22		26		30	ns
t_{PZH} / t_{PZL}	3-state Output Enable Time \overline{OE}_n to $n\bar{Y}$	4.5		16	32		40		46	ns
t_{PLZ} / t_{PHZ}	3-state Output Disable Time \overline{OE}_n to $n\bar{Y}$	4.5		16	32		40		46	ns
t_{TLH} / t_{THL}	Output Transition Time	4.5		7	12		15		18	ns

AC Waveforms



GD54/74HC367, GD54/74HCT367

HEX 3-STATE NONINVERTING BUFFERS

General Description

These devices are identical in pinout to the 54/74LS367. They have high drive current outputs which enable high speed operation even when driving large bus capacitances. The HC/HCT 365 and HC/HCT 367 have noninverting outputs, while the HC/HCT 366 and HC/HCT 368 have inverting outputs. The HC/HCT 365 and HC/HCT 366 have two 3-state control inputs which are NORed together to control all 6 gates. The HC/HCT 367 and HC/HCT 368 have two output enables, where one enable controls 4 gates and the other controls the remaining 2 gates. These devices are characterized for operation over wide temperature ranges to meet industry and military specifications.

Features

- Low Power consumption characteristic of CMOS devices
- Output drive capability: 15 LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts
for HCT 4.5 to 5.5 volts
- Low input current: $1\mu\text{A}$ Max.
- Low quiescent current: $80\mu\text{A}$ Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs

Logic Symbol

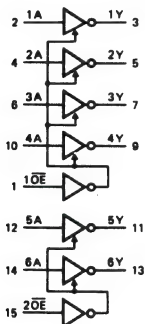
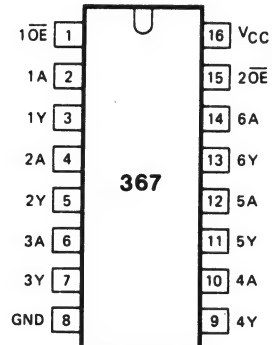


Fig. 1 Logic symbol

Pin Configuration



Suffix-Blank : Plastic Dual In Line Package
 Suffix-J : Ceramic Dual In Line Package
 Suffix-D : Small Outline Package

Function Table

INPUTS		OUTPUTS
nOE	nA	nY
L	L	L
L	H	H
H	X	Z

H = HIGH voltage level
 L = LOW voltage level
 X = don't care
 Z = high impedance OFF-state

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HC367		GD54HC367		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2		1.5 3.15 4.2		V
V _{IL}	LOW level input voltage		2.0 4.5 6.0			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH} or V _{IL}	I _{OH} = -20μA	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0	1.9 4.4 5.9		1.9 4.4 5.9		V
				I _{OH} = -6mA I _{OH} = -7.8mA	4.5 6.0	3.98 5.48	4.3 5.2	3.84 5.34	3.7 5.2		
			I _{OL} =20μA	2.0 4.5 6.0			0.1 0.1 0.1	0.1 0.1 0.1		0.1 0.1 0.1	
				I _{OL} =6mA I _{OL} =7.8mA	4.5 6.0	0.17 0.15	0.26 0.26	0.33 0.33	0.4 0.4		
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	6.0			0.1		1.0		1.0	μA
I _{OZ}	Three-State leakage current	V _{IN} =V _{IH} or V _{IL} V _O =V _{CC} or GND	6.0		0.01	0.5		5.0		10.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	6.0			8		80		160	μA

DC Electrical Characteristics for HCT

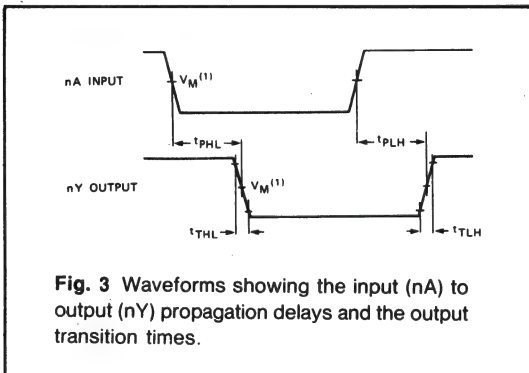
SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HCT367		GD54HCT367		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		4.5 to 5.0	2.0			2.0		2.0		V
V _{IL}	LOW level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH} or V _{IL}	I _{OH} = -20μA	4.5	4.4	4.5	4.4		4.4		V
			I _{OH} = -6mA	4.5	3.98	4.3	3.84		3.7		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH} or V _{IL}	I _{OL} =20μA	4.5		0.1	0.1		0.1		V
			I _{OL} =6mA	4.5		0.17	0.26		0.33	0.4	
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	5.5			0.1		1.0		1.0	μA
I _{OZ}	Three-State leakage current	V _{IN} =V _{IH} or V _{IL} V _O =V _{CC} or GND	5.5		0.01	0.5		5.0		10.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	5.5			8		80		160	μA

AC Characteristics for HC: $t_r = t_f = 6\text{ns}$ $C_L = 50\text{pF}$

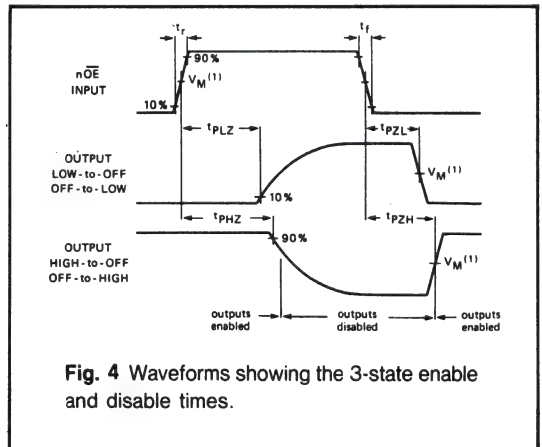
SYMBOL	PARAMETER	V_{CC} (V)	$T_A = 25^\circ\text{C}$			GD74HC367		GD54HC367		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} / t_{PHL}	Propagation Delay Time nA to nY	2.0 4.5 6.0		30 10 9	90 19 16		120 24 20		140 29 25	ns
t_{PZH} / t_{PZL}	3-state Output Enable Time nOE to nY	2.0 4.5 6.0		38 12 11	135 24 22		175 32 30		205 40 38	ns
t_{PLZ} / t_{PHZ}	3-state Output Disable Time nOE to nY	2.0 4.5 6.0		38 12 11	135 24 22		175 32 30		205 40 38	ns
t_{TLH} / t_{THL}	Output Transition Time	2.0 4.5 6.0		15 6 5	60 12 10		75 15 13		90 18 15	ns

AC Characteristics for HCT: $t_r = t_f = 6\text{ns}$ $C_L = 50\text{pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A = 25^\circ\text{C}$			GD74HCT367		GD54HCT367		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation Delay Time nA to nY	4.5		12	22		26		30	ns
t_{PZH} t_{PZL}	3-state Output Enable Time nOE to nY	4.5		13	26		34		42	ns
t_{PLZ} t_{PHZ}	3-state Output Disable Time nOE to nY	4.5		13	26		34		42	ns
t_{TLH} t_{THL}	Output Transition Time	4.5		7	12		15		18	ns

AC Waveforms**Note to AC waveforms**

- (1) HC : $V_M = 50\%$; $V_I = \text{GND to } V_{CC}$
HCT : $V_M = 1.3\text{V}$; $V_I = \text{GND to } 3\text{V}$.



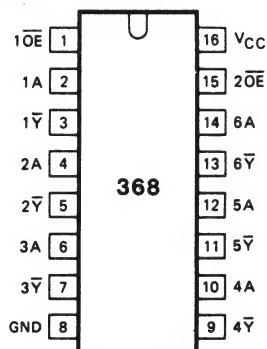
GD54/74HC368, GD54/74HCT368

HEX 3-STATE INVERTING BUFFERS

General Description

These devices are identical in pinout to the 54/74LS368. They have high drive current outputs which enable high speed operation even when driving large buscapacitances. The HC/HCT 365 and HC/HCT 367 have noninverting outputs, while the HC/HCT 366 and HC/HCT 368 have inverting outputs. The HC/HCT 365 and HC/HCT 366 have two 3-state control inputs which are NORed together to control all 6 gates. The HC/HCT 367 and HC/HCT 368 have two output enables, where one enable controls 4 gates and the other controls the remaining 2-gates. These devices are characterized for operation over wide temperature ranges to meet industry and military specifications.

Pin Configuration



Suffix-Blank : Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package
Suffix-D : Small Outline Package

Features

- Low Power consumption characteristic of CMOS devices
- Output drive capability: 15 LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts
for HCT 4.5 to 5.5 volts
- Low input current: $1\mu A$ Max.
- Low quiescent current: $80\mu A$ Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs

Function Table

INPUTS		OUTPUTS
$n\overline{OE}$	nA	$n\overline{Y}$
L	L	H
L	H	L
H	X	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC Supply voltage		-0.5	+7	V
I_{IK}, I_{OK}	DC input or output diode current	for $V_I < -0.5$ or $V_I > V_{CC} + 0.5V$		20	mA
I_O	DC output source or sink current	for $-0.5V < V_O < V_{CC} + 0.5V$		35	mA
I_{CC}	DC V_{CC} or GND current			70	mA
T_{stg}	Storage temperature range		-65	150	°C
P_D	Power dissipation per package	above +70°C: derate linearly with 8mW/K		500	mW
T_L	Lead temperature	At distance 1/16±1/32 in. from case for 60 sec(CERAMIC) 10 sec(PLASTIC)		300 260	°C

Recommended Operating Conditions

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range V_{CC} : GD54/74HC Types GD54/74HCT Types	2 4.5	6 5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A : GD74 Types GD54 Types	-40 -55	+85 +125	°C
Input Rise and Fall times t_r, t_f : GD54/74HC Types at 2V at 4.5V at 6V GD54/74HCT Types at 4.5 V		1000 500 400 500	ns

Logic Symbol

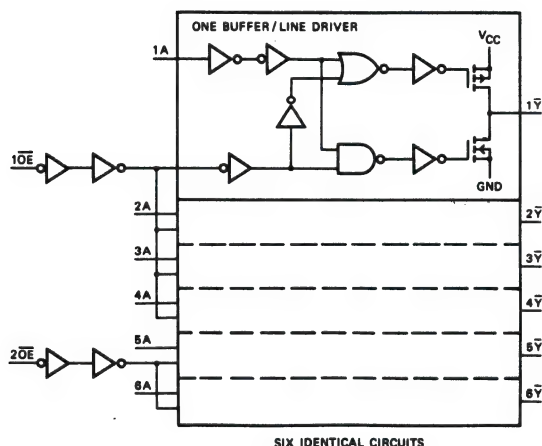


Fig. 1 Logic diagram

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION		V _{CC} (V)	T _A =25°C			GD74HC368		GD54HC368		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage			2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2		1.5 3.15 4.2		V
V _{IL}	LOW level input voltage			2.0 4.5 6.0			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH} or V _{IL}	I _{OH} =−20μA	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V
			I _{OH} =−6mA	4.5 6.0	3.98 5.48	4.3 5.2		3.84 5.34		3.7 5.2		
			I _{OH} =−7.8mA									
V _{OL}	LOW level output voltage	V _{IN} =V _{IH} or V _{IL}	I _{OL} =20μA	2.0 4.5 6.0			0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V
			I _{OL} =6mA	4.5 6.0		0.17 0.15	0.26 0.26		0.33 0.33		0.4 0.4	
			I _{OL} =7.8mA									
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND		6.0			0.1		1.0		1.0	μA
I _{OZ}	Three-State leakage current	V _{IN} =V _{IH} or V _{IL}	V _O =V _{CC} or GND	6.0		0.01	0.5		5.0		10.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA		6.0			8		80		160	μA

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION		V _{CC} (V)	T _A = 25 °C			GD74HCT368		GD54HCT368		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage			4.5 to 5.0	2.0			2.0		2.0		V
V _{IL}	LOW level input voltage			4.5 to 5.5			0.8		0.8		0.8	V
V _{OH}	HIGH level output voltage	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -20μA	4.5	4.4	4.5		4.4		4.4		V
			I _{OH} = -6mA	4.5	3.98	4.3		3.84		3.7		
V _{OL}	LOW level output voltage	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 20μA	4.5			0.1		0.1		0.1	V
			I _{OL} = 6mA	4.5		0.17	0.26		0.33		0.4	
I _{IN}	Input leakage Current	V _{IN} = V _{CC} or GND		5.5			0.1		1.0		1.0	μA
I _{OZ}	Three-State leakage current	V _{IN} = V _{IH} or V _{IL}	V _O = V _{CC} or GND	5.5		0.01	0.5		5.0		10.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} = V _{CC} or GND I _{out} = 0 μA		5.5			8		80		160	μA

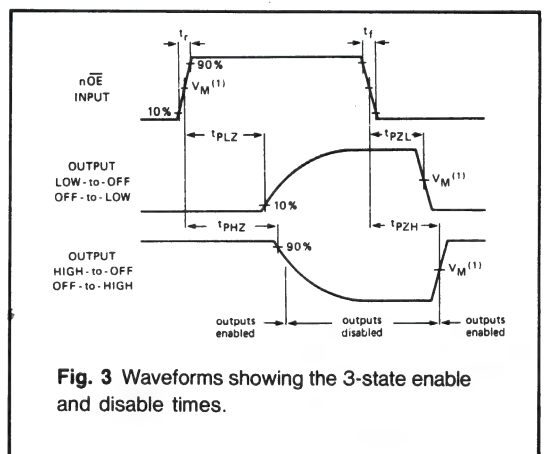
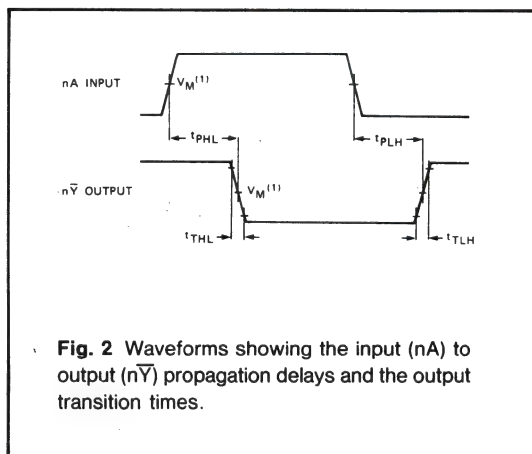
AC Characteristics for HC: $t_r = t_f = 6\text{ns}$ $C_L = 50\text{ pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A = 25^\circ\text{C}$			GD74HC368		GD54HC368		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
$t_{PLH} /$ t_{PHL}	Propagation Delay Time nA to nY	2.0 4.5 6.0		28 9 8	85 18 16		110 23 20		130 28 25	ns
$t_{PZH} /$ t_{PZL}	3-state Output Enable Time nOE to nY	2.0 4.5 6.0		38 12 11	135 24 22		175 32 30		205 40 38	ns
$t_{PLZ} /$ t_{PHZ}	3-state Output Disable Time nOE to nY	2.0 4.5 6.0		38 12 11	135 24 22		175 32 30		205 40 38	ns
$t_{TLH} /$ t_{THL}	Output Transition Time	2.0 4.5 6.0		15 6 5	60 12 10		75 15 13		90 18 15	ns

AC Characteristics for HCT: $t_r = t_f = 6\text{ns}$ $C_L = 50\text{ pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A = 25^\circ\text{C}$			GD74HCT368		GD54HCT368		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
$t_{PLH} /$ t_{PHL}	Propagation Delay Time nA to nY	4.5		12	22		26		30	ns
$t_{PZH} /$ t_{PZL}	3-state Output Enable Time nOE to nY	4.5		13	26		34		42	ns
$t_{PLZ} /$ t_{PHZ}	3-state Output Disable Time nOE to nY	4.5		13	26		34		42	ns
$t_{TLH} /$ t_{THL}	Output Transition Time	4.5		7	12		15		18	ns

AC Waveforms



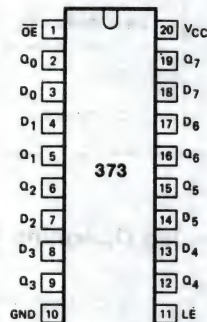
GD54/74HC373, GD54/74HCT373

OCTAL 3-STATE NONINVERTING D-TYPE TRANSPARENT LATCHES

General Description

These devices are identical in pinout to the 54/74LS374. They contain eight D-type master/slave flip-flops with a common clock and clear. Data meeting the setup and hold time requirements are transferred to the 3-state outputs on the rising edge of the clock pulse. The output enable input does not affect the states of the flip-flops, but when output enable is high, the outputs are forced to the device is not selected. The HC/HCT 373 are identical in function to the HC/HCT 573 which have the input pins on the opposite side of the package from the output pins. They are similar in function to the HC/HCT 533 which have inverting outputs. These devices are characterized for operation over wide temperature ranges to meet industry and military specifications.

Pin Configuration



Suffix-Blank : Plastic Dual In Line Package
 Suffix-J : Ceramic Dual In Line Package
 Suffix-D : Small Outline Package

Features

- Low Power consumption characteristic of CMOS devices
- Output drive capability: 15 LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts
for HCT 4.5 to 5.5 volts
- Low input current: $1\mu\text{A}$ Max.
- Low quiescent current: $80\mu\text{A}$ Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs

Function Table

OPERATING MODES	INPUTS			INTERNAL LATCHES	OUTPUTS Q_0 to Q_7
	$\overline{\text{OE}}$	LE	D_n		
enable and read register (transparent mode)	L	H	L	L	L
	L	H	H	H	H
latch and read register	L	L	L	L	L
	L	L	h	H	H
latch register and disable outputs	H	L	L	L	Z
	H	L	h	H	Z

H = HIGH voltage level

h = HIGH voltage level one set-up time prior to the HIGH-to-LOW LE transition

L = LOW voltage level

L = LOW voltage level one set-up time prior to the HIGH-to-LOW LE transition

Z = high impedance OFF-state

Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC Supply voltage		-0.5	+7	V
I_{IK}, I_{OK}	DC input or output diode current	for $V_I < -0.5$ or $V_I > V_{CC} + 0.5V$		20	mA
I_O	DC output source or sink current	for $-0.5V < V_O < V_{CC} + 0.5V$		35	mA
I_{CC}	DC V_{CC} or GND current			70	mA
T_{stg}	Storage temperature range		-65	150	°C
P_D	Power dissipation per package	above +70°C: derate linearly with 8mW/K		500	mW
T_L	Lead temperature	At distance 1/16 ± 1/32 in. from case for 60 sec(CERAMIC) 10 sec(PLASTIC)		300 260	°C

Recommended Operating Conditions

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range V_{CC} : GD54/74HC Types GD54/74HCT Types	2 4.5	6 5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A : GD74 Types GD54 Types	-40 -55	+85 +125	°C
Input Rise and Fall times t_r, t_f : GD54/74HC Types at 2V at 4.5V at 6V GD54/74HCT Types at 4.5 V		1000 500 400 500	ns

Logic Diagram

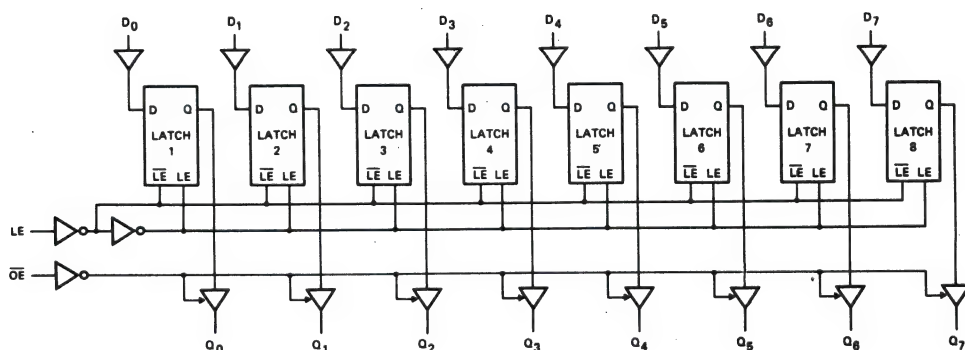


Fig. 1 Logic diagram.

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A = 25°C			GD74HC373		GD54HC373		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2		1.5 3.15 4.2		V
V _{IL}	LOW level input voltage		2.0 4.5 6.0			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V
V _{OH}	HIGH level output voltage	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -20μA	2.0	1.9	2.0	1.9		1.9		V
				4.5	4.4	4.5	4.4		4.4		
			I _{OH} = -6mA I _{OH} = -7.8mA	6.0	5.9	6.0	5.9		5.9		
				4.5	3.98	4.3	3.84		3.7		
V _{OL}	LOW level output voltage	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 20μA	2.0			0.1		0.1		V
				4.5			0.1		0.1		
			I _{OL} = 6mA I _{OL} = 7.8mA	6.0			0.1		0.1		
				4.5	0.17	0.26	0.33		0.4		
I _{IN}	Input leakage Current	V _{IN} = V _{CC} or GND	6.0			0.1		1.0		1.0	μA
I _{OZ}	Three-State leakage current	V _{IN} = V _{IH} or V _{IL} V _O = V _{CC} or GND	6.0		0.01	0.5		5.0		10.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} = V _{CC} or GND I _{out} = 0μA	6.0			8		80		160	μA

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A = 25°C			GD74HCT373		GD54HCT373		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		4.5 to 5.0	2.0			2.0		2.0		V
V _{IL}	LOW level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V _{OH}	HIGH level output voltage	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -20μA	4.5	4.4	4.5	4.4		4.4		V
				4.5	3.98	4.3	3.84		3.7		
			I _{OH} = -6mA	4.5							
				4.5							
V _{OL}	LOW level output voltage	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 20μA	4.5			0.1		0.1		V
				4.5							
			I _{OL} = 6mA	4.5		0.17	0.26		0.33		
				4.5						0.4	
I _{IN}	Input leakage Current	V _{IN} = V _{CC} or GND	5.5			0.1		1.0		1.0	μA
I _{OZ}	Three-State leakage current	V _{IN} = V _{IH} or V _{IL} V _O = V _{CC} or GND	5.5		0.01	0.5		5.0		10.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} = V _{CC} or GND I _{out} = 0μA	5.5			8		80		160	μA

Timing Requirement for HC: $t_r = t_f = 6\text{ns}$ $C_L = 50\text{ pF}$

SYMBOL	PARAMETER		V_{CC} (V)	$T_A = 25^\circ\text{C}$			GD74HC373		GD54HC373		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_w	Pulse width	LE high	2.0	80	30		100		120		ns
			4.5	16	10		20		25		
			6.0	14	8		18		22		
t_{su}	Setup time	Data before LE ↓	2.0	60	30		100		120		ns
			4.5	12	10		20		25		
			6.0	10	8		18		22		
t_h	Hold time	Data after LE ↓	2.0	3	0		3		3		ns
			4.5	3	0		3		3		
			6.0	3	0		3		3		

AC Characteristics for HC: $t_r = t_f = 6\text{ns}$ $C_L = 50\text{ pF}$

SYMBOL	PARAMETER		V_{CC} (V)	$T_A = 25^\circ\text{C}$			GD74HC373		GD54HC373		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
$t_{PLH}/$ t_{PHL}	Propagation Delay Time Dn to Qn		2.0		40	140		180		210	ns
			4.5		14	28		36		40	
			6.0		12	26		33		38	
$t_{PLH}/$ t_{PHL}	Propagation Delay Time LE to Qn		2.0		42	150		190		220	ns
			4.5		16	32		42		50	
			6.0		14	30		38		45	
$t_{PZH}/$ t_{PZL}	3-state Output Enable Time \overline{OE} to Qn		2.0		45	150		190		220	ns
			4.5		15	30		38		45	
			6.0		14	26		33		38	
$t_{PLZ}/$ t_{PHZ}	3-state Output Disable Time \overline{OE} to Qn		2.0		45	150		190		220	ns
			4.5		15	30		38		45	
			6.0		14	26		33		38	
$t_{TLH}/$ t_{THL}	Output Transition Time		2.0		15	60		75		90	ns
			4.5		6	12		15		18	
			6.0		5	10		13		15	

Timing Requirements for HCT: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER		V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HCT373		GD54HCT373		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_w	Pulse width	LE high	4.5	16	10		20		25		ns
t_{su}	Setup time	Data after LE \downarrow	4.5	12	10		20		25		ns
t_h	Hold time	Data before LE \downarrow	4.5	3	0		3		3		ns

AC Characteristics for HCT: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HCT373		GD54HCT373		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
$t_{PLH}/$ t_{PHL}	Propagation Delay Time D_n to Q_n	4.5		16	30		38		44	ns
$t_{PLH}/$ t_{PHL}	Propagation Delay Time LE to Q_n	4.5		19	35		42		48	ns
$t_{PZH}/$ t_{PZL}	3-state Output Enable time \overline{OE} to Q_n	4.5		15	30		38		45	ns
$t_{PLZ}/$ t_{PHZ}	3-state Output Disable Time \overline{OE} to Q_n	4.5		15	30		38		45	ns
$t_{TLH}/$ t_{THL}	Output Transition Time	4.5		6	12		15		18	ns

AC Waveforms

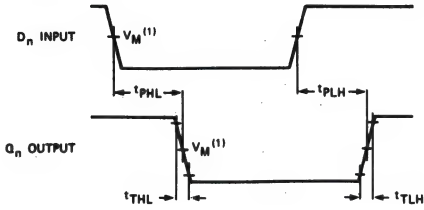


Fig. 2 Waveforms showing the data input (D_n) to output (Q_n) propagation delays and the output transition times.

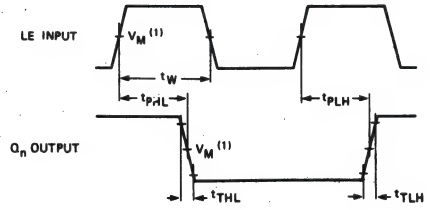


Fig. 3 Waveforms showing the latch enable input (LE) pulse width, the latch enable input to output (Q_n) propagation delays and the output transition times.

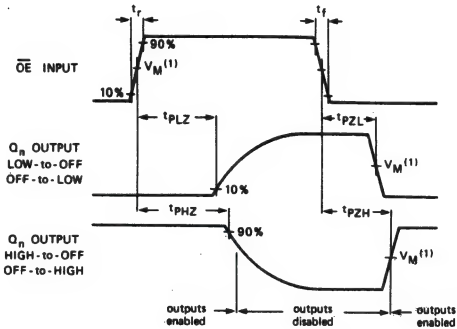


Fig. 4 Waveforms showing the 3-state enable and disable time.

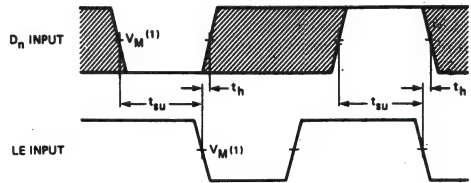


Fig. 5 Waveforms showing the data set-up and hold times for D_n input to LE input.

Note to Fig. 5

The shaded areas indicate when the input is permitted to change for predictable output performance.

Note to AC waveforms

(1) HC : $V_M=50\%$; $V_I=GND$ to V_{CC} .
HCT: $V_M=1.3V$; $V_I=GND$ to $3V$.

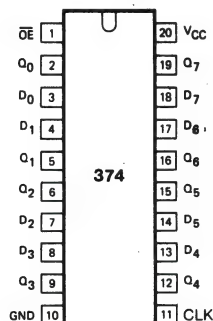
GD54/74HC374, GD54/74HCT374

OCTAL 3-STATE NONINVERTING D-TYPE FLIP-FLOPS

General Description

These devices are identical in pinout to the 54/74LS374. They contain eight D-type master/slave flip-flops with a common clock and clear. Data meeting the setup and hold time requirements are transferred to the 3-state outputs on the rising edge of the clock pulse. The output enable input does not affect the states of the flip-flops, but when output enable is high, the outputs are forced to the high impedance state. Data may thus be stored even when the device is not selected. The HC/HCT 374 are identical in function to the HC/HCT 574 which have the input pins on the opposite side of the package from the output pins. They are similar in function to the HC/HCT 534 which have inverting outputs. These devices are characterized for operation over wide temperature ranges to meet industry and military specifications.

Pin Configuration



Suffix-Blank : Plastic Dual In Line Package
 Suffix-J : Ceramic Dual In Line Package
 Suffix-D : Small Outline Package

Features

- Low Power consumption characteristic of CMOS devices
- Output drive capability: 15 LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts
for HCT 4.5 to 5.5 volts
- Low input current: 1μA Max.
- Low quiescent current: 80μA Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs

Function Table

OPERATING MODES	INPUTS			INTERNAL FLIP-FLOPS	OUTPUTS Q ₀ to Q ₇
	OE	CLK	D _n		
load and read register	L	↑	L	L	L
	L	↑	h	H	H
load register and disable outputs	H	↑	L	L	Z
	H	↑	h	H	Z

H = HIGH voltage level

h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CLK transition

L = LOW voltage level

l = LOW voltage level one set-up time prior to the LOW-to-HIGH CLK transition

Z = high impedance OFF-state

↑ = LOW-to-HIGH clock transition

Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC Supply voltage		-0.5	+7	V
I_{IK}, I_{OK}	DC input or output diode current	for $V_I < -0.5$ or $V_I > V_{CC} + 0.5V$		20	mA
I_O	DC output source or sink current	for $-0.5V < V_O < V_{CC} + 0.5V$		35	mA
I_{CC}	DC V_{CC} or GND current			70	mA
T_{stg}	Storage temperature range		-65	150	°C
P_D	Power dissipation per package	above +70°C: derate linearly with 8mW/K		500	mW
T_L	Lead temperature	At distance 1/16±1/32 in. from case for 60 sec(CERAMIC) 10 sec(PLASTIC)		300 260	°C

Recommended Operating Conditions

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range V_{CC} : GD54/74HC Types GD54/74HCT Types	2 4.5	6 5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A : GD74 Types GD54 Types	-40 -55	+85 +125	°C
Input Rise and Fall times t_r, t_f : GD54/74HC Types at 2V at 4.5V at 6V GD54/74HCT Types at 4.5 V		1000 500 400 500	ns

Logic Diagram

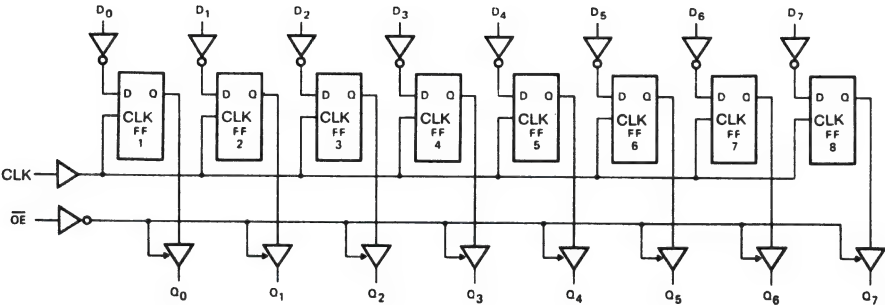


Fig. 1 Logic diagram

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HC374		GD54HC374		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2		1.5 3.15 4.2		V
V _{IL}	LOW level input voltage		2.0 4.5 6.0			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH} or V _{IL}	I _{OH} =-20μA	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0	1.9 4.4 5.9		1.9 4.4 5.9		V
			I _{OH} =-6mA	4.5 6.0	3.98 5.48	4.3 5.2	3.84 5.34		3.7 5.2		
			I _{OH} =-7.8mA	6.0	5.48	5.2	5.34		5.2		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH} or V _{IL}	I _{OL} =20μA	2.0 4.5 6.0			0.1 0.1 0.1	0.1 0.1 0.1		0.1 0.1 0.1	V
			I _{OL} =6mA	4.5 6.0		0.17 0.15		0.33 0.33		0.4 0.4	
			I _{OL} =7.8mA	6.0		0.15		0.33		0.4	
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	6.0			0.1		1.0		1.0	μA
I _{OZ}	Three-State leakage current	V _{IN} =V _{IH} or V _{IL} V _O =V _{CC} or GND	6.0		0.01	0.5		5.0		10.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	6.0			8		80		160	μA

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HCT374		GD54HCT374		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		4.5 to 5.0	2.0			2.0		2.0		V
V _{IL}	LOW level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH} or V _{IL}	I _{OH} =-20μA	4.5	4.4	4.5	4.4		4.4		V
			I _{OH} =-6mA	4.5	3.98	4.3	3.84		3.7		
			I _{OH} =-7.8mA	6.0	5.48	5.2	5.34		5.2		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH} or V _{IL}	I _{OL} =20μA	4.5			0.1	0.1		0.1	V
			I _{OL} =6mA	4.5		0.17		0.33		0.4	
			I _{OL} =7.8mA	6.0		0.15		0.33		0.4	
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	5.5			0.1		1.0		1.0	μA
I _{OZ}	Three-State leakage current	V _{IN} =V _{IH} or V _{IL} V _O =V _{CC} or GND	5.5		0.01	0.5		5.0		10.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	5.5			8		80		160	μA

Timing Requirements for HC: $t_r = t_f = 6\text{ns}$ $C_L = 50\text{ pF}$

SYMBOL	PARAMETER		V_{CC} (V)	$T_A = 25^\circ\text{C}$			GD74HC374		GD54HC374		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_w	Pulse width	CLK high or low	2.0	80	30		100		120		ns
			4.5	16	10		20		25		
			6.0	14	8		18		22		
t_{su}	Setup time	Data before CLK \uparrow	2.0	60	30		100		120		ns
			4.5	12	10		20		25		
			6.0	10	8		18		22		
t_h	Hold time	Data after CLK \uparrow	2.0	3	0		3		3		ns
			4.5	3	0		3		3		
			6.0	3	0		3		3		

AC Characteristics for HC: $t_r = t_f = 6\text{ns}$ $C_L = 50\text{ pF}$

SYMBOL	PARAMETER		V_{CC} (V)	$T_A = 25^\circ\text{C}$			GD74HC374		GD54HC374		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
f_{max}	Maximum Clock Pulse frequency		2.0	6	20		5		4		MHz
			4.5	30	65		25		20		
			6.0	35	75		30		25		
$t_{PLH}/$ t_{PHL}	Propagation Delay Time CLK to Q_n		2.0		40	140		180		210	ns
			4.5		14	28		36		40	
			6.0		12	26		33		38	
$t_{PZH}/$ t_{PZL}	3-State Output Enable Time \overline{OE} to Q_n		2.0		38	140		180		210	ns
			4.5		13	28		36		40	
			6.0		12	26		33		38	
$t_{PLZ}/$ t_{PHZ}	3-State Output Disable Time \overline{OE} to Q_n		2.0		38	140		180		210	ns
			4.5		13	28		36		40	
			6.0		12	26		33		38	
$t_{TLH}/$ t_{THL}	Output Transition Time		2.0		15	60		75		90	ns
			4.5		6	12		15		18	
			6.0		5	10		13		15	

Timing Requirements for HCT: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER		V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HCT374		GD54HCT374		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_w	Pulse width	CLK high or low	4.5	16	10		20		25		ns
t_{su}	Setup time	Data before CLK↑	4.5	12	10		20		25		ns
t_h	Hold time	Data after CLK↑	4.5	3	0		3		3		ns

AC Characteristics for HCT: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HCT374		GD54HCT374		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
f_{max}	Maximum Clock Pulse Frequency	4.5	27	54		22		18		MHz
$t_{PLH}/$ t_{PHL}	Propagation Delay Time CLK to Q_n	4.5		16	30		38		45	ns
$t_{PZH}/$ t_{PZL}	3-state Output Enable Time. \overline{OE} to Q_n	4.5		15	30		38		45	ns
$t_{PLZ}/$ t_{PHZ}	3-state Output disable time \overline{OE} to Q_n	4.5		15	30		38		45	ns
$t_{TLH}/$ t_{THL}	Output Transition Time	4.5		6	12		15		18	ns

AC Waveforms

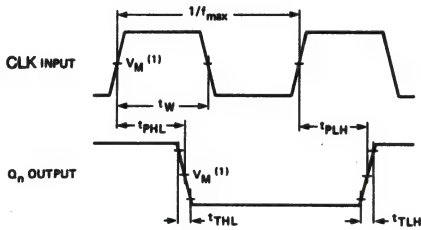


Fig. 2 Waveforms showing the clock (CLK) to output (Q_n) propagation delays, the clock pulse width, output transition times and the maximum clock pulse frequency.

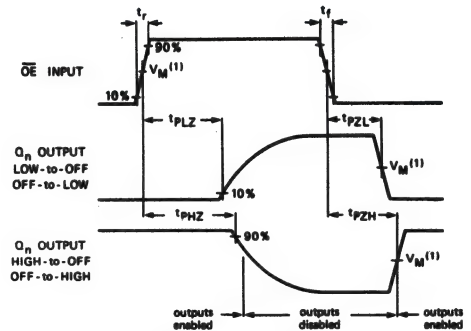


Fig. 3 Waveforms showing the 3-state enable and disable times.

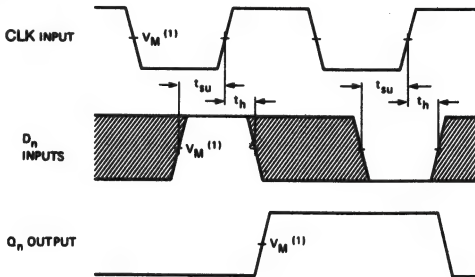


Fig. 4 Waveforms showing the data set-up and hold times for D_n input.

Note to Fig. 4

The shaded areas indicate when the input is permitted to change for predictable output performance.

Note to AC waveforms

(1) HC : $V_M = 50\%$; $V_I = GND$ to V_{CC} .

HCT : $V_M = 1.3V$; $V_I = GND$ to $3V$.

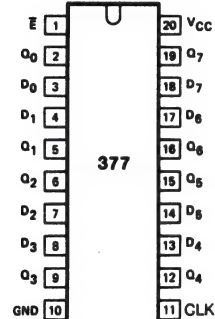
GD54/74HC377, GD54/74HCT377

OCTAL D-TYPE FLIP-FLOPS WITH COMMON CLOCK & ENABLE

General Description

These devices are identical in pinout to the 54/74LS377. They contain eight master/slave D-type flip-flops with a common clock and enable. Information at the data inputs meeting the setup and hold time requirements is transferred to the outputs on the rising edge of the clock pulse if the enable input is low. When the clock input is at either the high or low level, the data input signal has no effect at the output. The circuits are designed to prevent false clocking by transitions at the enable input. The HC/HCT 377 are similar to the HC/HCT 273, but feature a common enable instead of a common clear. These devices are characterized for operation over wide temperature ranges to meet industry and military specifications.

Pin Configuration



Suffix-Blank : Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package
Suffix-D : Small Outline Package

Features

- Low Power consumption characteristic of CMOS devices
- Output drive capability: 10 LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts
for HCT 4.5 to 5.5 volts
- Low input current: 1 μ A Max.
- Low quiescent current: 80 μ A Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs

Function Table

OPERATING MODES	INPUTS			OUTPUTS
	CLK	\bar{E}	D_n	Q_n
load "1"	\uparrow	L	h	H
load "0"	\uparrow	L	L	L
hold (do nothing)	\uparrow	h	X	no change
	X	H	X	no change

H = HIGH voltage level

h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CLK transition

L = LOW voltage level

L = LOW voltage level one set-up time prior to the LOW-to-HIGH CLK transition

\uparrow = LOW-to-HIGH transition

X = don't care

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD54HC377		GD74HC377		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2		1.5 3.15 4.2		V
V _{IL}	LOW level input voltage		2.0 4.5 6.0			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH}	I _{OH} =-20μA	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0	1.9 4.4 5.9		1.9 4.4 5.9		V
			I _{OH} =-4mA	4.5 6.0	3.98 5.48	4.3 5.2	3.84 5.34		3.7 5.2		
		or V _{IL}	I _{OH} =-5.2mA	4.5 6.0	3.98 5.48	4.3 5.2	3.84 5.34		3.7 5.2		
			I _{OH} =-5.2mA	4.5 6.0	3.98 5.48	4.3 5.2	3.84 5.34		3.7 5.2		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH}	I _{OL} =20μA	2.0 4.5 6.0			0.1 0.1 0.1	0.1 0.1 0.1		0.1 0.1 0.1	V
			I _{OL} =4mA	4.5 6.0		0.17 0.15	0.26 0.26	0.33 0.33		0.4 0.4	
		or V _{IL}	I _{OL} =4mA	4.5 6.0		0.17 0.15	0.26 0.26	0.33 0.33		0.4 0.4	
			I _{OL} =5.2mA	4.5 6.0		0.17 0.15	0.26 0.26	0.33 0.33		0.4 0.4	
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	6.0			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	6.0			2		80		160	μA

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HCT377		GD54HCT377		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		4.5 to 5.5	2.0			2.0		2.0		V
V _{IL}	LOW level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH}	I _{OH} =-20μA	4.5	4.4	4.5	4.4		4.4		V
		or V _{IL}	I _{OH} =-4mA	4.5	3.98	4.3	3.84		3.7		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH}	I _{OL} =20μA	4.5			0.1	0.1		0.1	V
		or V _{IL}	I _{OL} =4mA	4.5		0.17	0.26	0.33		0.4	
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	5.5			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	5.5			8		80		160	μA

Timing Requirements for HC: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER		V _{CC} (V)	T _A =25°C			GD74HC377		GD54HC377		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t _w	Pulse width	CLK high	2.0	80	30		100		120		ns
			4.5	16	10		20		25		
			6.0	14	8		18		22		
t _{su}	Setup time	Data before CLK↑	2.0	60	30		100		120		ns
			4.5	12	10		20		25		
			6.0	10	8		18		22		
t _h	Hold time	Data after CLK↑	2.0	3	0		3		3		ns
			4.5	3	0		3		3		
			6.0	3	0		3		3		

AC Characteristics for HC: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER		V _{CC} (V)	T _A =25°C			GD74HC377		GD54HC377		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
f _{max}	Maximum Clock Pulse Frequency		2.0	6	20		5		4		MHz
			4.5	30	65		25		20		
			6.0	35	75		30		25		
t _{PLH} / t _{PHL}	Propagation Delay Time CLK to Qn		2.0		38	110		140		160	ns
			4.5		14	24		30		34	
			6.0		12	20		25		30	
t _{TLH} / t _{THL}	Output Transition Time		2.0		25	70		85		100	ns
			4.5		8	15		18		22	
			6.0		7	13		16		19	

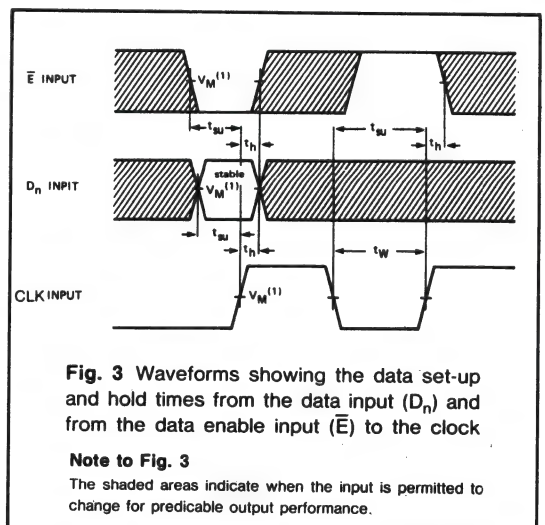
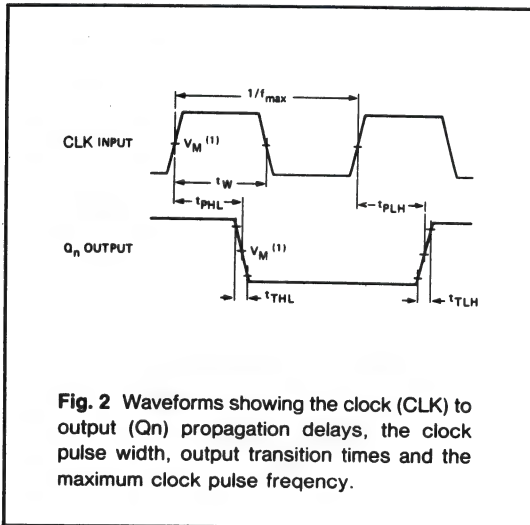
Timing Requirements for HCT: $t_r = t_f = 6\text{ns}$ $C_L = 50\text{ pF}$

SYMBOL	PARAMETER		V _{CC} (V)	T _A = 25°C			GD74HCT377		GD54HCT377		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_w	Pulse Width	CLK High or Low	4.5	16	10		20		25		ns
t_{su}	Setup time	Data before CLK↑	4.5	12	10		20		25		ns
t_h	Hold time	Data after CLK↑	4.5	3	0		3		3		ns

AC Characteristics for HCT: $t_r = t_f = 6\text{ns}$ $C_L = 50\text{ pF}$

SYMBOL	PARAMETER		V _{CC} (V)	T _A = 25°C			GD74HCT377		GD54HCT377		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
f_{max}	Maximum Clock Pulse Frequency		4.5	27	54		22		18		MHz
$t_{PLH}/$ t_{PHL}	Propagation Delay Time CLK to Q _n		4.5		16	26		32		36	ns
$t_{TLH}/$ t_{THL}	Output Transition Time		4.5		8	15		18		22	ns

AC Waveforms



GD54/74HC386, GD54/74HCT386

QUAD 2-INPUT EXCLUSIVE OR GATES

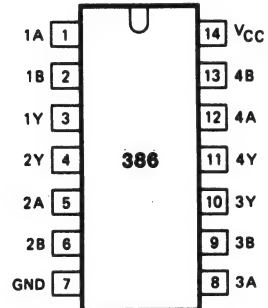
General Description

These devices are identical in pinout to the 54/74LS386. They contain four independent 2-input Exclusive OR gates. The HC/HCT 386 are electrically identical to the HC/HCT 86, However, different in pinouts with each other. These devices are characterized for operation over wide temperature ranges to meet industry and military specifications.

Features

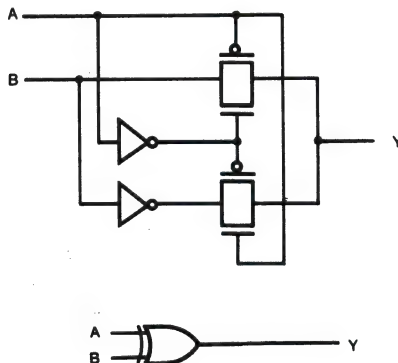
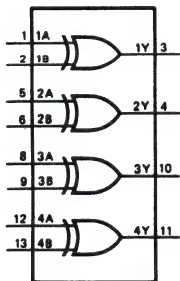
- Low Power consumption characteristic of CMOS devices
- Output drive capability: 10 LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts
for HCT 4.5 to 5.5 volts
- Low input current: $1\mu\text{A}$ Max.
- Low quiescent current: $20\mu\text{A}$ Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs

Pin Configuration



Suffix-Blank : Plastic Dual In Line Package
 Suffix-J : Ceramic Dual In Line Package
 Suffix-D : Small Outline Package

Logic Symbol and Diagram



Function Table

INPUTS		OUTPUT
nA	nB	nY
L	L	L
L	H	H
H	L	H
H	H	L

H = HIGH voltage level
 L = LOW voltage level

Fig. 1 Logic symbol

Fig. 2 Logic diagram (one gate)

Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC Supply voltage		-0.5	+7	V
I_{IK}, I_{OK}	DC input or output diode current	for $V_I < -0.5$ or $V_I > V_{CC} + 0.5V$		20	mA
I_O	DC output source or sink current	for $-0.5V < V_O < V_{CC} + 0.5V$		25	mA
I_{CC}	DC V_{CC} or GND current			50	mA
T_{stg}	Storage temperature range		-65	150	°C
P_D	Power dissipation per package	above +70°C: derate linearly with 8mW/K		500	mW
T_L	Lead temperature	At distance 1/16 ± 1/32 in. from case for 60 sec(CERAMIC) 10 sec(PLASTIC)		300 260	°C

Recommended Operating Conditions

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range V_{CC} : GD54/74HC Types GD54/74HCT Types	2 4.5	6 5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A : GD74 Types GD54 Types	-40 -55	+85 +125	°C
Input Rise and Fall times t_r, t_f : GD54/74HC Types at 2V at 4.5V at 6V GD54/74HCT Types at 4.5V		1000 500 400 500	ns

Circuit Diagram

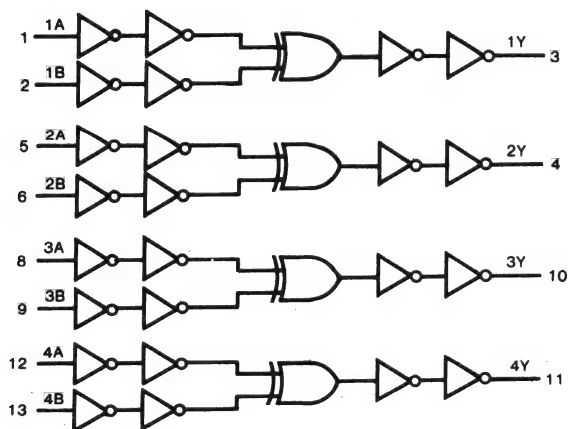


Fig. 3 Circuit diagram

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HC386		GD54HC386		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2		1.5 3.15 4.2		V
V _{IL}	LOW level input voltage		2.0 4.5 6.0			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH}	I _{OH} =-20μA	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0	1.9 4.4 5.9		1.9 4.4 5.9		V
		or V _{IL}	I _{OH} =-4mA I _{OH} =-5.2mA	4.5 6.0	3.98 5.48	4.3 5.2	3.84 5.34		3.7 5.2		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH}	I _{OL} =20μA	2.0 4.5 6.0			0.1 0.1 0.1	0.1 0.1 0.1		0.1 0.1 0.1	V
		or V _{IL}	I _{OL} =4mA I _{OL} =5.2mA	4.5 6.0		0.17 0.15	0.26 0.26	0.33 0.33		0.4 0.4	
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	6.0			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	6.0			2		20		40	μA

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HCT386		GD54HCT386		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		4.5 to 5.5	2.0			2.0		2.0		V
V _{IL}	LOW level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH}	I _{OH} =-20μA	4.5	4.4	4.5	4.4		4.4		V
		or V _{IL}	I _{OH} =-4mA	4.5	3.98	4.3	3.84		3.7		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH}	I _{OL} =20μA	4.5			0.1	0.1		0.1	V
		or V _{IL}	I _{OL} =4mA	4.5		0.17	0.26	0.33		0.4	
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	5.5			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	5.5			2		20		40	μA

AC Characteristics for HC: $t_r = t_f = 6\text{ns}$ $C_L = 50\text{pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A = 25^\circ\text{C}$			GD74HC386		GD54HC386		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
$t_{PLH}/$ t_{PHL}	Propagation Delay Time nA, nB to nY	2.0 4.5 6.0		36 11 9	65 21 19		85 26 24		100 29 27	ns
$t_{TLH}/$ t_{THL}	Output Transition Time	2.0 4.5 6.0		19 7 6	75 15 13		95 19 16		110 22 19	ns

AC Characteristics for HCT: $t_r = t_f = 6\text{ns}$ $C_L = 50\text{pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A = 25^\circ\text{C}$			GD74HCT386		GD54HCT386		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
$t_{PLH}/$ t_{PHL}	Propagation Delay Time nA, nB to nY	4.5		14	28		36		44	ns
$t_{TLH}/$ t_{THL}	Output Transition Time	4.5		7	15		19		22	ns

AC Waveform

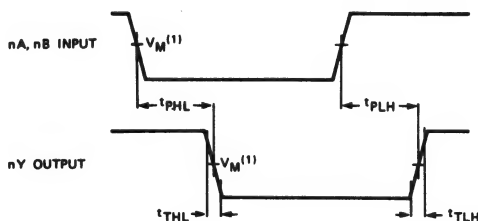


Fig. 4 Waveforms showing the input (nA, nB) to output (nY) propagation delays and the output transition times.

Note to AC waveform

(1) HC : $V_M = 50\%$, $V_I = \text{GND to } V_{CC}$
HCT: $V_M = 1.3V$, $V_I = \text{GND to } 3V$.

GD54/74HC390, GD54/74HCT390

DUAL 4-BIT DECADE COUNTERS

General Description

These devices are identical in pinout to the 54/74LS390. They incorporate two independent 4-Bit decade counters, each composed of a divide-by-2 and a divide-by-5 counter. The divide-by-2 and divide-by-5 counters can be cascaded to form dual decade, dual bi-quinary, or various combinations up to a single divide-by-100 counter. Each counter is incremented on the falling edge of the clock, and each has an independent clear input. When the clear is set high all four bits of each counter are set to a low level. This enables count truncation and allows the implementation of divide-by-N counter configurations.

Features

- Low Power consumption characteristic of CMOS devices
- Output drive capability: 10 LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts
for HCT 4.5 to 5.5 volts
- Low input current: 1 μ A Max.
- Low quiescent current: 80 μ A Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs

Function Table

BCD COUNT SEQUENCE FOR 1/2 THE "390"

COUNT	OUTPUTS			
	Q ₀	Q ₁	Q ₂	Q ₃
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H

Note

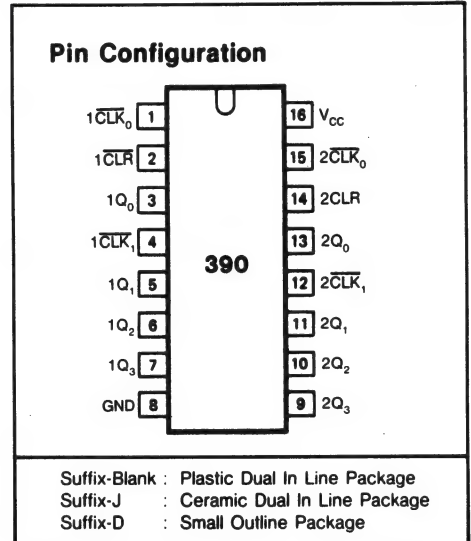
Output Q₀ connected to nCLK₁ with counter input on nCLK₀.

BI-QUINARY COUNT SEQUENCE FOR 1/2 THE "390"

COUNT	OUTPUTS			
	Q ₀	Q ₁	Q ₂	Q ₃
0	L	L	L	L
1	L	H	L	L
2	L	L	H	L
3	L	H	H	L
4	L	L	L	H
5	H	L	L	L
6	H	H	L	L
7	H	L	H	L
8	H	H	H	L
9	H	L	L	H

Note

Output Q₃ connected to nCLK₀ with counter input on nCLK₁.



Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC Supply voltage		-0.5	+7	V
I_{IK}, I_{OK}	DC input or output diode current	for $V_I < -0.5$ or $V_I > V_{CC} + 0.5V$		20	mA
I_O	DC output source or sink current	for $-0.5V < V_O < V_{CC} + 0.5V$		25	mA
I_{CC}	DC V_{CC} or GND current			50	mA
T_{stg}	Storage temperature range		-65	150	°C
P_D	Power dissipation per package	above +70°C: derate linearly with 8mW/K		500	mW
T_L	Lead temperature	At distance 1/16 ± 1/32 in. from case for 60 sec(CERAMIC) 10 sec(PLASTIC)		300 260	°C

Recommended Operating Conditions

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range V_{CC} : GD54/74HC Types GD54/74HCT Types	2 4.5	6 5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A : GD74 Types GD54 Types	-40 -55	+85 +125	°C
Input Rise and Fall times t_r, t_f : GD54/74HC Types at 2V at 4.5V at 6V GD54/74HCT Types at 4.5V		1000 500 400 500	ns

Logic Diagram

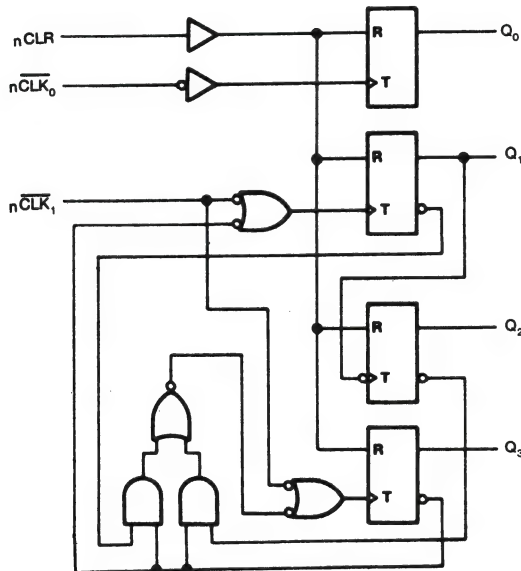


Fig. 1 Logic diagram

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HC390		GD54HC390		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2		1.5 3.15 4.2		V
V _{IL}	LOW level input voltage		2.0 4.5 6.0			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH}	I _{OH} =-20μA	2.0	1.9	2.0			1.9		V
				4.5	4.4	4.5			4.4		
		or V _{IL}	I _{OH} =-4mA I _{OH} =-5.2mA	6.0	5.9	6.0			5.9		
				4.5	3.98	4.3			3.7		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH}	I _{OL} =20μA	2.0			0.1	0.1		0.1	V
				4.5			0.1	0.1		0.1	
		or V _{IL}	I _{OL} =4mA I _{OL} =5.2mA	6.0							
				4.5		0.17	0.26	0.33		0.4	
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	6.0			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	6.0			8		80		160	μA

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HCT390		GD54HCT390		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		4.5 to 5.5	2.0			2.0		2.0		V
V _{IL}	LOW level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH}	I _{OH} =-20μA	4.5	4.4	4.5			4.4		V
				4.5	3.98	4.3			3.7		
		or V _{IL}	I _{OH} =-4mA	4.5			3.84				
				4.5							
V _{OL}	LOW level output voltage	V _{IN} =V _{IH}	I _{OL} =20μA	4.5			0.1	0.1		0.1	V
				4.5							
		or V _{IL}	I _{OL} =4mA	4.5		0.17	0.26	0.33		0.4	
				4.5							
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	5.5			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	5.5			8		80		160	μA

Timing Requirements for HC: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER		V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HC390		GD54HC390		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_w	Pulse width	\overline{nCLK}_n , nCLR	2.0	80			100		120		ns
			4.5	16			20		24		
			6.0	14			18		20		
t_{rec}	Recovery time	\overline{nCLK}_n to nCLR	2.0	25			25		25		ns
			6.0	5			5		5		
			6.0	5			5		5		

AC Characteristics for HC: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER V_{CC}	(V)	$T_A=25^\circ\text{C}$			GD74HC390		GD54HC390		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
f_{max}	Maximum Clock Pulse Frequency	2.0	6	20		5		4.2		MHz
		4.5	31	60		25		21		
		6.0	36	71		28		25		
$t_{PLH}/$ t_{PHL}	Propagation Delay Time \overline{nCLK}_0 to Q_0	2.0		45	130		160		190	ns
		4.5		15	24		30		35	
		6.0		12	20		26		31	
$t_{PLH}/$ t_{PHL}	Propagation Delay Time \overline{nCLK}_1 to Q_1	2.0		45	130		160		190	ns
		4.5		15	24		30		35	
		6.0		12	20		26		31	
$t_{PLH}/$ t_{PHL}	Propagation Delay Time \overline{nCLK}_1 to Q_2	2.0		75	145		195		255	ns
		4.5		25	35		45		53	
		6.0		20	30		40		45	
$t_{PLH}/$ t_{PHL}	Propagation Delay Time \overline{nCLK}_1 to Q_3	2.0		50	130		160		190	ns
		4.5		16	30		35		40	
		6.0		13	25		31		36	
$t_{PLH}/$ t_{PHL}	Propagation Delay Time nCLR to Q_n	2.0		45	165		205		250	ns
		4.5		15	30		40		40	
		6.0		12	25		35		42	
$t_{TLH}/$ t_{THL}	Output Transition Time	2.0		28	25		95		110	ns
		4.5		7	15		19		22	
		6.0		6	13		16		19	

Timing Requirements for HCT: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER		V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HC390		GD54HC390		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_w	Pulse width	$n\overline{\text{CLK}}_n, n\text{CLR}$	4.5	18			23		27		ns
t_{rec}	Recovery time	$n\overline{\text{CLK}}_n$ to $n\text{CLR}$	4.5	5			5		5		ns

AC Characteristics for HCT: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HCT390		GD54HCT390		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
f_{max}	Maximum Clock Pulse Frequency	4.5	27	55		22		18		MHz
$t_{\text{PLH}}/$ t_{PHL}	Propagation Delay Time $n\overline{\text{CLK}}_0$ to Q_0	4.5		20	30		35		40	ns
$t_{\text{PLH}}/$ t_{PHL}	Propagation Delay Time $n\overline{\text{CLK}}_1$ to Q_1	4.5		20	30		35		40	ns
$t_{\text{PLH}}/$ t_{PHL}	Propagation Delay Time $n\overline{\text{CLK}}_1$ to Q_2	4.5		30	40		45		50	ns
$t_{\text{PLH}}/$ t_{PHL}	Propagation Delay Time $n\overline{\text{CLK}}_1$ to Q_3	4.5		21	29		44		49	ns
$t_{\text{PLH}}/$ t_{PHL}	Propagation Delay Time $n\text{CLR}$ to Q_n	4.5		20	30		35		40	ns
$t_{\text{TLH}}/$ t_{THL}	Output Transition Time	4.5		7	15		19		22	ns

AC Waveforms

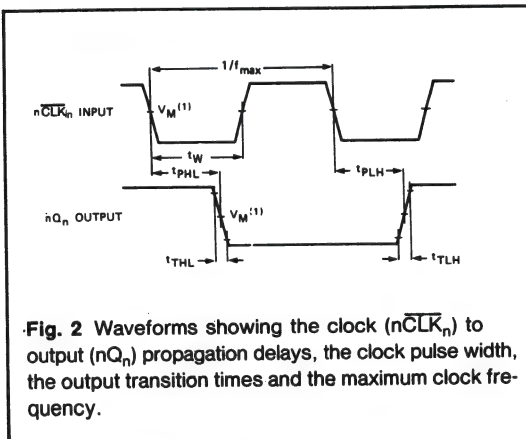


Fig. 2 Waveforms showing the clock ($n\overline{\text{CLK}}_n$) to output (nQ_n) propagation delays, the clock pulse width, the output transition times and the maximum clock frequency.

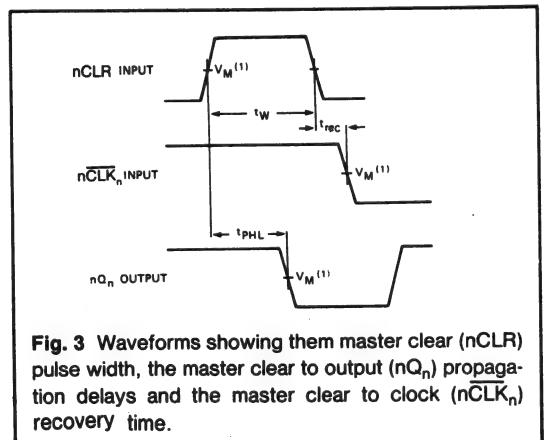


Fig. 3 Waveforms showing the master clear ($n\text{CLR}$) pulse width, the master clear to output (nQ_n) propagation delays and the master clear to clock ($n\overline{\text{CLK}}_n$) recovery time.

Note to AC waveforms

- (1) HC : $V_M=50\%$; $V_L=\text{GND}$ to V_{CC} .
HCT : $V_M=1.3V$; $V_L=\text{GND}$ to $3V$.

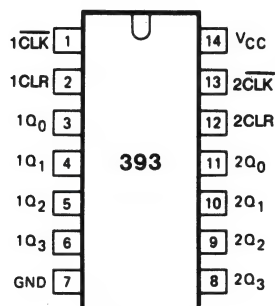
GD54/74HC393, GD54/74HCT393

DUAL 4-BIT BINARY COUNTERS

General Description

These devices are identical in pinout to the 54/74LS393. They consist of two independent 4-Bit binary ripple counters with parallel outputs from each counter stage. A divide-by-256 counter can be obtained by cascading the two binary counters. Each of the two 4-bit counters is incremented on the falling edge of the clock input, and each has an independent clear input. When clear is set high all four bits of each counter are set to a low level. This enables count truncation and allows the implementation of divide-by-N counter configurations. These devices are characterized for operation over wide temperature ranges to meet industry and military specifications.

Pin Configuration



Suffix-Blank : Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package
Suffix-D : Small Outline Package

Features

- Low Power consumption characteristic of CMOS devices
- Output drive capability: 10 LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts
for HCT 4.5 to 5.5 volts
- Low input current: 1 μ A Max.
- Low quiescent current: 80 μ A Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs

Function Table

COUNT	OUTPUTS			
	Q ₀	Q ₁	Q ₂	Q ₃
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
10	L	H	L	H
11	H	H	L	H
12	L	L	H	H
13	H	L	H	H
14	L	H	H	H
15	H	H	H	H

Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC Supply voltage		-0.5	+7	V
I_{IK}, I_{OK}	DC input or output diode current	for $V_I < -0.5$ or $V_I > V_{CC} + 0.5V$		20	mA
I_O	DC output source or sink current	for $-0.5V < V_O < V_{CC} + 0.5V$		35	mA
I_{CC}	DC V_{CC} or GND current			70	mA
T_{stg}	Storage temperature range		-65	150	°C
P_D	Power dissipation per package	above +70°C: derate linearly with 8mW/K		500	mW
T_L	Lead temperature	At distance 1/16 ± 1/32 in. from case for 60 sec(CERAMIC) 10 sec(PLASTIC)		300 260	°C

Recommended Operating Conditions

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range V_{CC} : GD54/74HC Types GD54/74HCT Types	2 4.5	6 5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A : GD74 Types GD54 Types	-40 -55	+85 +125	°C
Input Rise and Fall times t_r, t_f : GD54/74HC Types at 2V at 4.5V at 6V GD54/74HCT Types at 4.5V		1000 500 400 500	ns

Logic Diagram

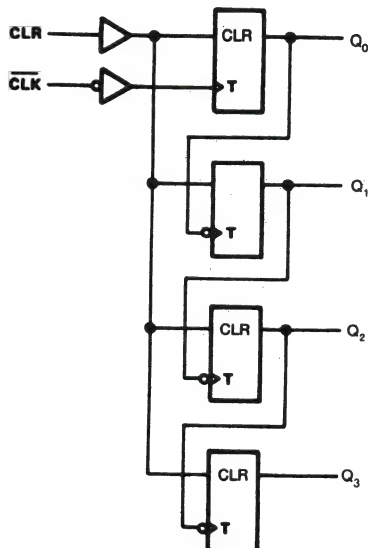


Fig. 1 Logic diagram

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HC393		GD54HC393		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2		1.5 3.15 4.2		V
V _{IL}	LOW level input voltage		2.0 4.5 6.0			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH}	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V
		or V _{IL}									
V _{OL}	LOW level output voltage	V _{IN} =V _{IH}	2.0 4.5 6.0			0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V
		or V _{IL}									
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	6.0			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	6.0			8		80		160	μA

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HCT393		GD54HCT393		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		4.5 to 5.5	2.0			2.0		2.0		V
V _{IL}	LOW level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH}	4.5	4.4	4.5		4.4		4.4		V
		or V _{IL}	4.5	3.98	4.3		3.84		3.7		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH}	4.5			0.1		0.1		0.1	V
		or V _{IL}	4.5		0.17	0.26		0.33		0.4	
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	5.5			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	5.5			8		80		160	μA

Timing Requirements for HC: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER		V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HC393		GD54HC393		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_w	Pulse width	$\overline{\text{CLK}}$ high or low	2.0	80			100		120		ns
			4.5	16			20		24		
			6.0	14			18		20		
		CLR high	2.0	80			100		120		ns
			4.5	16			20		24		
			6.0	14			18		20		
t_{rec}	Recovery time	CLR to $\overline{\text{CLK}}$	2.0	5			5		5		ns
			4.5	5			5		5		
			6.0	5			5		5		

AC Characteristics for HC: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER		V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HC393		GD54HC393		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
f_{max}	Maximum Clock Pulse Frequency		2.0	6	20		5		4.2		MHz
			4.5	31	60		25		21		
			6.0	36	71		28		25		
$t_{\text{PLH}}/$ t_{PHL}	Propagation Delay Time $\overline{\text{CLK}}$ to Q_0		2.0		41	125		150		180	ns
			4.5		14	24		30		37	
			6.0		12	20		25		31	
$t_{\text{PLH}}/$ t_{PHL}	Propagation Delay Time $\overline{\text{CLK}}$ to Q_3		2.0		83	260		315		390	ns
			4.5		29	50		64		79	
			6.0		24	44		52		67	
t_{PHL}	Propagation Delay Time CLR to Q_n		2.0		39	140		175		210	ns
			4.5		14	28		35		42	
			6.0		11	14		30		36	
$t_{\text{TLH}}/$ t_{THL}	Output Transition Time		2.0		28	75		95		110	ns
			4.5		7	15		19		22	
			6.0		6	13		16		19	

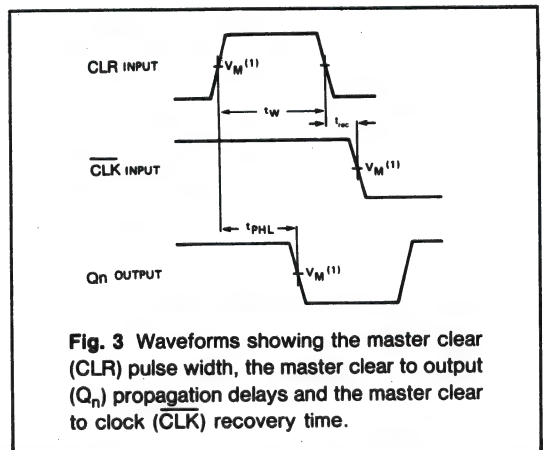
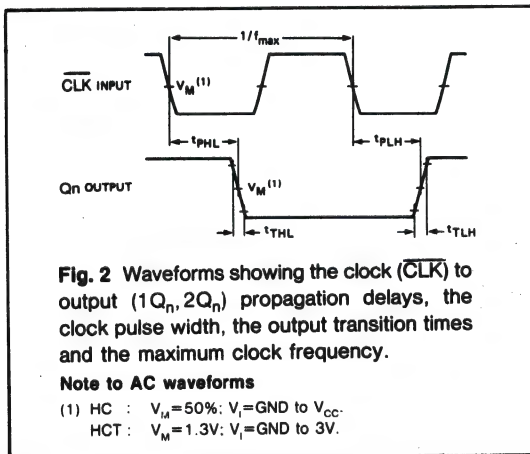
Timing Requirements for HCT: $t_r = t_f = 6\text{ns}$ $C_L = 50\text{ pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A = 25^\circ\text{C}$			GD74HCT393		GD54HCT393		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_w	Pulse width	CLK high or low	4.5	19		24		29		ns
		CLR high	4.5	16		20		24		ns
t_{rec}	Recovery time	CLR to $\overline{\text{CLK}}$	4.5	5		5		5		ns

AC Characteristics for HCT: $t_r = t_f = 6\text{ns}$ $C_L = 50\text{ pF}$

SYMBOL	PARAMETER	V_{CC}	$T_A = 25^\circ\text{C}$			GD74HCT393		GD54HCT393		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
f_{max}	Maximum Clock Pulse Frequency	4.5	27			22		18		MHz
$t_{PLH}/$ t_{PHL}	Propagation Delay Time $\overline{\text{CLK}}$ to Q_0	4.5		20	30		36		43	ns
$t_{PLH}/$ t_{PHL}	Propagation Delay Time $\overline{\text{CLK}}$ to Q_3	4.5		38	58		70		89	ns
t_{PHL}	Propagation Delay Time CLR to Q_n	4.5		18	32		39		47	ns
$t_{TLH}/$ t_{THL}	Output Transition Time	4.5		7	15		19		22	ns

AC Waveforms



GD54/74HC423, GD54/74HCT423

DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATORS

General Description

The devices are identical in pinout to the 54/74LS423. They consist of two retriggerable monostable multivibrators. Each multivibrator features an active-low asynchronous clear and both negative-and positive-edge triggered inputs, either of which can be used as an enable. Also included is a clear input that when taken low resets the one shot. The HC/HCT 423 cannot be triggered from clear. The output pulse width can be controlled with stability by the simple equation:

$$PW = (R_{EXT}) (C_{EXT})$$

Where PW is in seconds, R_{EXT} is in ohms, an C_{EXT} is in farads. Refer to HC/HCT123 and 221 for triggering from clear pin.

Features

- Low Power consumption characteristic of CMOS devices
- Output drive capability: 10 LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts
for HCT 4.5 to 5.5 volts
- Low input current: $1\mu A$ Max.
- Low quiescent current: $80\mu A$ Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs

Functional Symbol

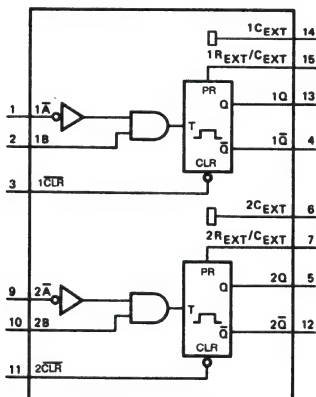
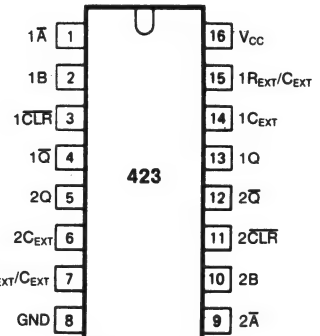


Fig. 1 Functional symbol

Pin Configuration



Suffix-Blank : Plastic Dual In Line Package
 Suffix-J : Ceramic Dual In Line Package
 Suffix-D : Small Outline Package

Function Table

INPUTS			OUTPUTS	
\overline{nCLR}	\overline{nA}	nB	nQ	\overline{nQ}
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	\uparrow		
H	\downarrow	H		

= one HIGH level output pulse
 = one LOW level output pulse

Timing Component

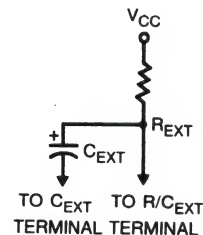
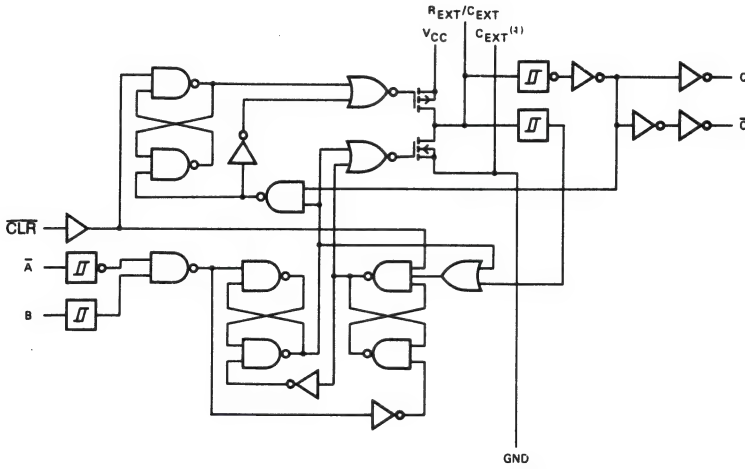


Fig. 2 Timing Component

Logic Diagram



It is recommended to ground pins 6 ($2C_{EXT}$) and 14 ($1C_{EXT}$) externally to pin 8 (GND)

Fig. 3 Logic diagram

Theory of Operation

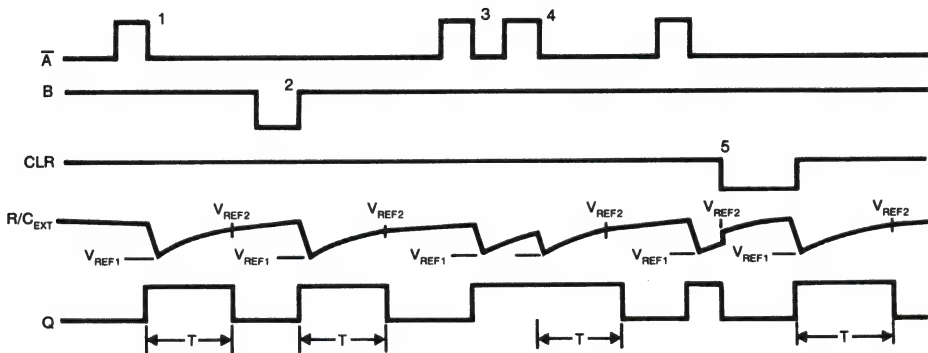


Fig. 4 (1) POSITIVE EDGE TRIGGER
(2) NEGATIVE EDGE TRIGGER
(3) POSITIVE EDGE TRIGGER
(4) POSITIVE EDGE RE-TRIGGER (PULSE LENGTHENING)
(5) RESET PULSE SHORTENING

Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC Supply voltage		-0.5	+7	V
I_{IK}, I_{OK}	DC input or output diode current	for $V_I < -0.5$ or $V_I > V_{CC} + 0.5V$		20	mA
I_O	DC output source or sink current	for $-0.5V < V_O < V_{CC} + 0.5V$		25	mA
I_{CC}	DC V_{CC} or GND current			50	mA
T_{stg}	Storage temperature range		-65	150	°C
P_D	Power dissipation per package	above +70°C: derate linearly with 8mW/K		500	mW
T_L	Lead temperature	At distance 1/16 ± 1/32 in. from case for 60 sec(CERAMIC) 10 sec(PLASTIC)		300 260	°C

Recommended Operating Conditions

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range V_{CC} : GD54/74HC Types GD54/74HCT Types	2 4.5	6 5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A : GD74 Types GD54 Types	-40 -55	+85 +125	°C
Input Rise and Fall times t_r, t_f : GD54/74HC Types at 2V at 4.5V at 6V GD54/74HCT Types at 4.5V		1000 500 400 500	ns

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A = 25°C			GD74HCT423		GD54HCT423		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2		1.5 3.15 4.2		V
V _{IL}	LOW level input voltage		2.0 4.5 6.0			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V
V _{OH}	HIGH level output voltage	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -20μA I _{OH} = -4mA I _{OH} = -5.6mA	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0	1.9 4.4 5.9		1.9 4.4 5.9		V
				4.5 6.0	3.98 5.48	4.3 5.2	3.84 5.34		3.7 5.2		
V _{OL}	LOW level output voltage	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 20μA I _{OL} = 6mA I _{OL} = 7.8mA	2.0 4.5 6.0			0.1 0.1 0.1	0.1 0.1 0.1		0.1 0.1 0.1	V
				4.5 6.0		0.17 0.15	0.26 0.26	0.33 0.33		0.4 0.4	
I _{IN}	Input leakage Current	V _{IN} = V _{CC} or GND	6.0			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} = V _{CC} or GND I _{out} = 0μA	6.0			8		80		160	μA

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A = 25°C			GD74HCT423		GD54HCT423		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		4.5 to 5.0	2.0			2.0		2.0		V
V _{IL}	LOW level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V _{OH}	HIGH level output voltage	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -20μA	4.5	4.4	4.5	4.4		4.4		V
			I _{OH} = -4mA	4.5	3.98	4.3	3.84		3.7		
V _{OL}	LOW level output voltage	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 20μA	4.5		0.1	0.1		0.1		V
			I _{OL} = 4mA	4.5		0.17	0.26		0.33		
I _{IN}	Input leakage Current	V _{IN} = V _{CC} or GND	5.5			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} = V _{CC} or GND I _{out} = 0μA	5.5			8		80		160	μA

Timing Requirements for HC: $t_r = t_f = 6\text{ns}$ $C_L = 50\text{ pF}$

SYMBOL	PARAMETER		V_{CC} (V)	$T_A = 25^\circ\text{C}$			GD74HC423		GD54HC423		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_w	Pulse width	Trigger $n\bar{A} = \text{low}$, $nB = \text{high}$ Clear $n\bar{CLR} = \text{low}$	2.0 4.5 6.0	100 20 17			125 25 21		150 30 26		ns
		Output $nQ = \text{high}$, $n\bar{Q} = \text{low}$ $C_{EXT} = 100\text{nF}$, $R_{EXT} = 10\text{K}\Omega$	5.0		450						μs
		Output $nQ = \text{high}$, $n\bar{Q} = \text{low}$ $C_{EXT} = \text{OpF}$, $R_{EXT} = 5\text{K}\Omega$	5.0		75						ns
t_{rt}	Retrigger time	nA , nB $C_{EXT} = \text{OpF}$, $R_{EXT} = 5\text{K}\Omega$	5.0		44						ns
R_{ext}	External timing resistor. Note 2		2.0 5.0	10 2		1,000 1000					$\text{K}\Omega$
C_{ext}	External timing capacitor. Note 3		5.0	No limits							pF

AC Characteristics for HC: $t_r = t_f = 6\text{ns}$ $C_L = 50\text{ pF}$

SYMBOL	PARAMETER		V_{CC} (V)	$T_A = 25^\circ\text{C}$			GD74HC423		GD54HC423		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
$t_{PHL}/$ t_{PLH}	Propagation Delay Time $n\bar{A}$, nB to nQ , $n\bar{Q}$		2.0 4.5 6.0		80 30 24	225 51 43		290 64 54		360 77 65	ns
$t_{PHL}/$ t_{PLH}	Propagation Delay Time $n\bar{CLR}$, nQ , $n\bar{Q}$		2.0 4.5 6.0		66 24 19	200 43 37		260 54 46		310 65 55	ns
$t_{TLH}/$ t_{THL}	Output Transition Time		2.0 4.5 6.0		19 7 6	75 15 13		95 19 15		110 22 19	ns

Timing Requirements for HCT: $t_r = t_f = 6\text{ns}$ $C_L = 50\text{ pF}$

SYMBOL	PARAMETER		V_{CC} (V)	$T_A = 25^\circ\text{C}$			GD74HCT423		GD54HCT423		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_w	Pulse width	Trigger $n\bar{A} = \text{low}$, $nB = \text{high}$ Clear $n\bar{CLR} = \text{low}$	4.5	20			25		30		ns
		Output $nQ = \text{high}$, $n\bar{Q} = \text{low}$ $C_{EXT} = 100\text{nF}$, $R_{EXT} = 10\text{K}\Omega$	5.0		450						μs
		Output $nQ = \text{high}$, $n\bar{Q} = \text{low}$ $C_{EXT} = 0\text{pF}$, $R_{EXT} = 5\text{K}\Omega$	5.0		75						ns
t_{rt}	Retrigger time	$n\bar{A}$, nB $C_{EXT} = 0\text{pF}$, $R_{EXT} = 5\text{K}\Omega$	5.0		41						ns
R_{ext}	External timing resistor. Note 2		2.0 5.0	10 2		1.000 1000					$\text{K}\Omega$
C_{ext}	External timing capacitor. Note 3		5.0	No limits							pF

AC Characteristics for HCT: $t_r = t_f = 6\text{ns}$ $C_L = 50\text{ pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A = 25^\circ\text{C}$			GD74HCT423		GD54HCT423		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
$t_{PHL}/$ t_{PLH}	Propagation Delay Time $n\bar{A}$, nB to nQ , $n\bar{Q}$	4.5		30	51		64		77	ns
$t_{PHL}/$ t_{PLH}	Propagation Delay Time $n\bar{CLR}$ to nQ , $n\bar{Q}$	4.5		26	46		58		64	ns
$t_{TLH}/$ t_{THL}	Output Transition Time	4.5		7	15		19		22	ns

AC Waveforms

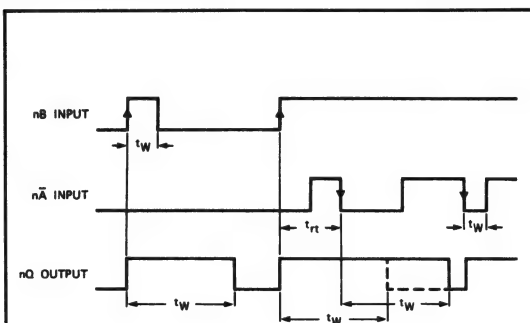


Fig. 5 Output pulse control using retrigger pulse; $\overline{nCLR} = \text{HIGH}$.

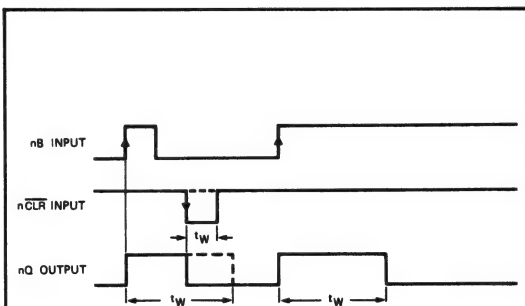


Fig. 6 Output pulse control using reset input \overline{nCLR} ; $nA = \text{LOW}$.

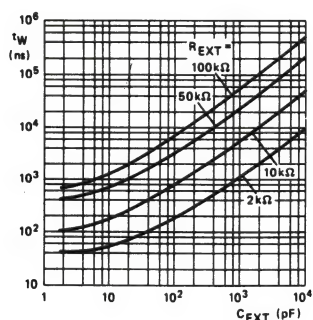


Fig. 7 Typical output pulse width as a function of the external capacitor values at $V_{CC} = 5.0\text{V}$ and $T_{amb} = 25^\circ\text{C}$.

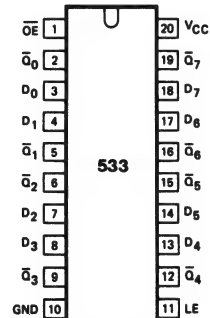
GD54/74HC533, GD54/74HCT533

OCTAL 3-STATE INVERTING D-TYPE TRANSPARENT LATCHES

General Description

These devices are identical in pinout to the 54/74LS533. They contain eight D-type latches, one latch enable, and one output control. These latches appear transparent to data, i.e., the outputs change asynchronously, when latch enable is high. When latch enable goes low, data meeting the setup time becomes latched. The output enable input does not affect the state of the latches when it is low. But when it is high, all outputs go to the high impedance state regardless of what signals are present at the other inputs and the state of the storage elements. The HC/HCT 533 are identical in function to the HC/HCT 563 which have the input pins on the opposite side of the package from the output pins. They are similar in function to the HC/HCT 373 which have noninverting outputs. These devices are characterized for operation over wide temperature ranges to meet industry and military specifications.

Pin Configuration



Suffix-Blank : Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package
Suffix-D : Small Outline Package

Features

- Low Power consumption characteristic of CMOS devices
- Output drive capability: 15LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts
for HCT 4.5 to 5.5 volts
- Low input current: 1 μ A Max.
- Low quiescent current: 80 μ A Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs

Function Table

OPERATING MODES	INPUTS			INTERNAL LATCHES	OUTPUTS \bar{Q}_0 to \bar{Q}_7
	\bar{OE}	LE	D_n		
enable and read (transparent mode)	L	H	L	L	H
	L	H	H	H	L
latch and read register	L	L	L	L	H
	L	L	H	H	L
latch register and disable outputs	H	X	X	X	Z
	H	X	X	X	Z

H = HIGH voltage level

h = HIGH voltage level one set-up time prior to the LOW-to-HIGH
LE transition or the HIGH-to-LOW \bar{OE} transition

L = LOW voltage level

l = LOW voltage level one set-up time prior to the LOW-to-HIGH
LE transition or the HIGH-to-LOW \bar{OE} transition

X = don't care

Z = high impedance OFF-state

Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC Supply voltage		-0.5	+7	V
I_{IK}, I_{OK}	DC input or output diode current	for $V_I < -0.5$ or $V_I > V_{CC} + 0.5V$		20	mA
I_O	DC output source or sink current	for $-0.5V < V_O < V_{CC} + 0.5V$		35	mA
I_{CC}	DC V_{CC} or GND current			70	mA
T_{stg}	Storage temperature range		-65	150	°C
P_D	Power dissipation per package	above +70°C: derate linearly with 8mW/K		500	mW
T_L	Lead temperature	At distance $1/16 \pm 1/32$ in. from case for 60 sec(CERAMIC) 10 sec(PLASTIC)		300 260	°C

Recommended Operating Conditions

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range V_{CC} : GD54/74HC Types GD54/74HCT Types	2 4.5	6 5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A : GD74 Types GD54 Types	-40 -55	+85 +125	°C
Input Rise and Fall times t_r, t_f : GD54/74HC Types at 2V at 4.5V at 6V GD54/74HCT Types at 4.5V		1000 500 400 500	ns

Logic Diagram

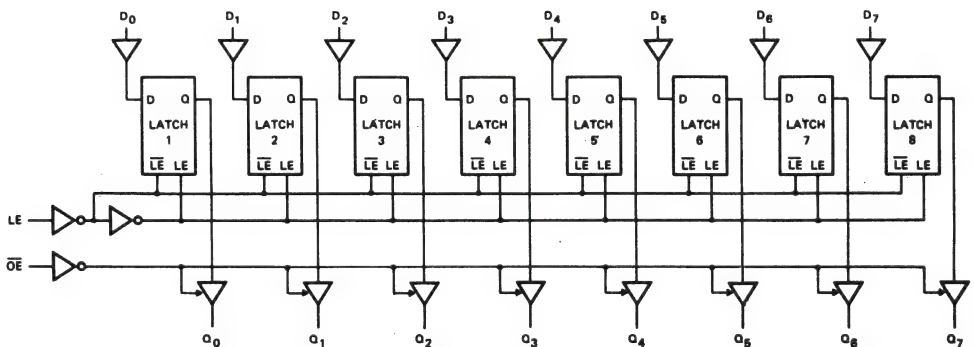


Fig. 1 Logic diagram.

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HC533		GD54HC533		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2		1.5 3.15 4.2		V
V _{IL}	LOW level input voltage		2.0 4.5 6.0			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH} or V _{IL}	I _{OH} =-20μA I _{OH} =-6mA I _{OH} =-7.8mA	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0	1.9 4.4 5.9		1.9 4.4 5.9		V
				4.5 6.0	3.98 5.48	4.3 5.2	3.84 5.34		3.7 5.2		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH} or V _{IL}	I _{OL} =20μA I _{OL} =6mA I _{OL} =7.8mA	2.0 4.5 6.0			0.1 0.1 0.1		0.1 0.1 0.1		V
				4.5 6.0		0.17 0.15	0.26 0.26		0.33 0.33		
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	6.0			0.1		1.0		1.0	μA
I _{OZ}	Three-State leakage current	V _{IN} =V _{IH} or V _{IL} V _O =V _{CC} or GND	6.0		0.01	0.5		5.0		10.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	6.0			8		80		160	μA

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HCT533		GD54HCT533		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		4.5 to 5.0	2.0			2.0		2.0		V
V _{IL}	LOW level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH} or V _{IL}	I _{OH} =-20μA	4.5	4.4	4.5	4.4		4.4		V
			I _{OH} =-6mA	4.5	3.98	4.3	3.84		3.7		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH} or V _{IL}	I _{OL} =20μA	4.5			0.1		0.1		V
			I _{OL} =6mA	4.5		0.17	0.26		0.33		
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	5.5			0.1		1.0		1.0	μA
I _{OZ}	Three-State leakage current	V _{IN} =V _{IH} or V _{IL} V _O =V _{CC} or GND	5.5		0.01	0.5		5.0		10.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	5.5			8		80		160	μA

Timing Requirements for HC: $t_r = t_f = 6\text{ns}$ $C_L = 50\text{ pF}$

SYMBOL	PARAMETER		V_{CC} (V)	$T_A = 25^\circ\text{C}$			GD74HC533		GD54HC533		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_w	Pulse width	LE high	2.0	80	30		100		120		ns
			4.5	16	10		20		25		
			6.0	14	8		18		22		
t_{su}	Setup time	Data after LE ↓	2.0	60	30		100		120		ns
			4.5	12	10		20		25		
			6.0	10	8		18		22		
t_h	Hold time	Data before LE ↓	2.0	3	0		3		3		ns
			4.5	3	0		3		3		
			6.0	3	0		3		3		

AC Characteristics for HC: $t_r = t_f = 6\text{ns}$ $C_L = 50\text{ pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A = 25^\circ\text{C}$			GD74HC533		GD54HC533		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
$t_{PLH}/$ t_{PHL}	Propagation Delay Time D_n to \overline{Q}_n	2.0		40	140		180		210	ns
		4.5		14	28		36		40	
		6.0		12	26		33		38	
$t_{PLH}/$ t_{PHL}	Propagation Delay Time LE to \overline{Q}_n	2.0		42	150		190		220	ns
		4.5		16	32		42		50	
		6.0		14	30		38		45	
$t_{PZH}/$ t_{PZL}	3-state Output Enable Time \overline{OE} to \overline{Q}_n	2.0		45	150		190		220	ns
		4.5		15	30		38		45	
		6.0		14	26		33		38	
$t_{PLZ}/$ t_{PHZ}	3-state Output Disable Time \overline{OE} to \overline{Q}_n	2.0		45	150		190		220	ns
		4.5		15	30		38		45	
		6.0		14	26		33		38	
$t_{TLH}/$ t_{THL}	Output Transition Time	2.0		15	60		75		90	ns
		4.5		6	12		15		18	
		6.0		5	10		13		15	

Timing Requirements for HCT: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER		V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HCT533		GD54HCT533		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_w	Pulse width	LE high	4.5	16	10		20		25		ns
t_{su}	Setup time	Data before LE ↓	4.5	12	10		20		25		ns
t_h	Hold time	Data after LE ↓	4.5	3	0		3		3		ns

AC Characteristics for HCT: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HCT533		GD54HCT533		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
$t_{PLH}/$ t_{PHL}	Propagation Delay Time D_n to \overline{Q}_n	4.5		16	30		38		44	ns
$t_{PLH}/$ t_{PHL}	Propagation Delay Time LE to \overline{Q}_n	4.5		19	35		42		48	ns
$t_{PZH}/$ t_{PZL}	3-state Output Enable Time \overline{OE} to \overline{Q}_n	4.5		15	30		38		45	ns
$t_{PLZ}/$ t_{PHZ}	3-state Output Disable Time \overline{OE} to \overline{Q}_n	4.5		15	30		38		45	ns
$t_{TLH}/$ t_{THL}	Output Transition Time	4.5		6	12		15		18	ns

AC Waveforms

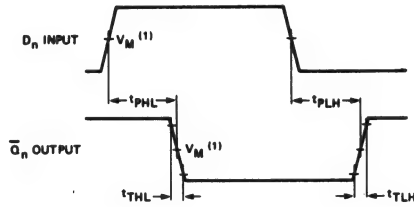


Fig. 2 Waveforms showing the data input (D_n) to output (Q_n) propagation delays and the output transition times.

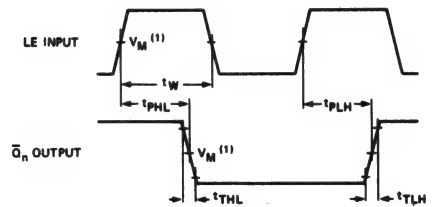


Fig. 3 Waveforms showing the latch enable input (LE) pulse width, the latch enable input to output (Q_n) propagation delays and the output transition times.

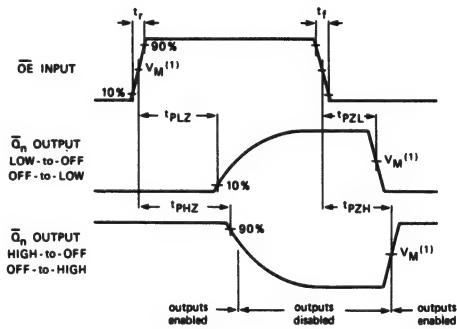


Fig. 4 Waveforms showing the 3-state enable and disable time.

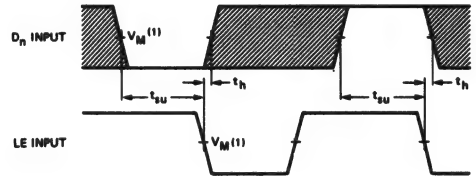


Fig. 5 Waveforms showing the data set-up and hold times for D_n input to LE input.

Note to Fig. 5

The shaded areas indicate when the input is permitted to change for predicable output performance.

Note to AC waveforms

- (1) HC : $V_M = 50\%$; $V_I = \text{GND to } V_{CC}$.
HCT: $V_M = 1.3\text{V}$; $V_I = \text{GND to } 3\text{V}$.

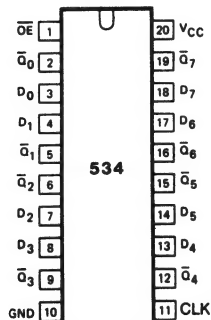
GD54/74HC534, GD54/74HCT534

OCTAL 3-STATE INVERTING D-TYPE FLIP-FLOPS

General Description

These devices are identical in pinout to the 54/74LS534. They contain eight D-type master/slave flip-flops with a common clock and clear. Data meeting the setup and hold time requirements are transferred to the 3-state outputs on the rising edge of the clock pulse. The output enable input does not affect the states of the flip-flops, but when output enable is high, the outputs are forced to the high impedance state. Data may thus be stored even when the device is not selected. The HC/HCT 534 are identical in function to the HC/HCT 564 which have the input pins on the opposite side of the package from the output pins. They are similar in function to the HC/HCT 374 which have noninverting outputs. These devices are characterized for operation over wide temperature ranges to meet industry and military specifications.

Pin Configuration



Suffix-Blank : Plastic Dual In Line Package
 Suffix-J : Ceramic Dual In Line Package
 Suffix-D : Small Outline Package

Features

- Low Power consumption characteristic of CMOS devices
- Output drive capability: 10 LS TTL Loads Min
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts
for HCT 4.5 to 5.5 volts
- Low input current: 1μA Max.
- Low quiescent current: 80μA Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs

Function Table

OPERATING MODES	INPUTS			INTERNAL FLIP-FLOPS	OUTPUT Q ₀ to Q ₇
	OE	CLK	D _n		
load and read register	L	↑	L	L	H
	L	↑	h	H	L
load register and disable outputs	H	↑	L	L	Z
	H	↑	h	H	Z

H = HIGH voltage level
 h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CLK transition
 L = LOW voltage level
 l = LOW voltage level one set-up time prior to the LOW-to-HIGH CLK transition
 Z = high impedance OFF-state
 ↑ = LOW-to-HIGH clock transition

Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC Supply voltage		-0.5	+7	V
I_{IK}, I_{OK}	DC input or output diode current	for $V_i < -0.5$ or $V_i > V_{CC} + 0.5V$		20	mA
I_O	DC output source or sink current	for $-0.5V < V_O < V_{CC} + 0.5V$		35	mA
I_{CC}	DC V_{CC} or GND current			70	mA
T_{stg}	Storage temperature range		-65	150	°C
P_D	Power dissipation per package	above +70°C: derate linearly with 8mW/K		500	mW
T_L	Lead temperature	At distance $1/16 \pm 1/32$ in. from case for 60 sec(CERAMIC) 10 sec(PLASTIC)		300 260	°C

Recommended Operating Conditions

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range V_{CC} : GD54/74HC Types GD54/74HCT Types	2 4.5	6 5.5	V
DC Input or Output Voltage V_i, V_O	0	V_{CC}	V
Operating Temperature T_A : GD74 Types GD54 Types	-40 -55	+85 +125	°C
Input Rise and Fall times t_r, t_f : GD54/74HC Types at 2V at 4.5V at 6V GD54/74HCT Types at 4.5V		1000 500 400 500	ns

Logic Diagram

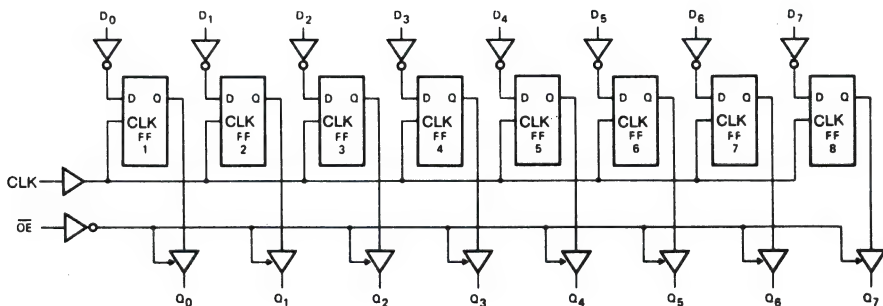


Fig. 1 Logic diagram.

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HC534		GD54HC534		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2		1.5 3.15 4.2		V
V _{IL}	LOW level input voltage		2.0 4.5 6.0			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH} or V _{IL}	I _{OH} =-20μA	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0	1.9 4.4 5.9		1.9 4.4 5.9		V
			I _{OH} =-6mA	4.5 6.0	3.98 5.48	4.3 5.2	3.84 5.34		3.7 5.2		
			I _{OH} =-7.8mA	6.0							
V _{OL}	LOW level output voltage	V _{IN} =V _{IH} or V _{IL}	I _{OL} =20μA	2.0 4.5 6.0			0.1 0.1 0.1	0.1 0.1 0.1		0.1 0.1 0.1	V
			I _{OL} =6mA	4.5 6.0		0.17 0.15	0.26 0.26	0.33 0.33		0.4 0.4	
			I _{OL} =7.8mA	6.0							
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	6.0			0.1		1.0		1.0	μA
I _{OZ}	Three-State leakage current	V _{IN} =V _{IH} or V _{IL} V _O =V _{CC} or GND	6.0		0.01	0.5		5.0		10.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	6.0			8		80		160	μA

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HCT534		GD54HCT534		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		4.5 to 5.0	2.0			2.0		2.0		V
V _{IL}	LOW level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH} or V _{IL}	I _{OH} =-20μA	4.5	4.4	4.5	4.4		4.4		V
			I _{OH} =-6mA	4.5	3.98	4.3	3.84		3.7		
			I _{OH} =-7.8mA	6.0							
V _{OL}	LOW level output voltage	V _{IN} =V _{IH} or V _{IL}	I _{OL} =20μA	4.5			0.1	0.1		0.1	V
			I _{OL} =6mA	4.5		0.17	0.26	0.33		0.4	
			I _{OL} =7.8mA	6.0							
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	5.5			0.1		1.0		1.0	μA
I _{OZ}	Three-State leakage current	V _{IN} =V _{IH} or V _{IL} V _O =V _{CC} or GND	5.5		0.01	0.5		5.0		10.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	5.5			8		80		160	μA

Timing Requirements for HC : $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER		V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HC534		GD54HC534		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_w	Pulse width	CLK high or low	2.0	80	30		100		120		ns
			4.5	16	10		20		25		
			6.0	14	8		18		22		
t_{su}	Setup time	Data before CLK \uparrow	2.0	60	30		100		120		ns
			4.5	12	10		20		25		
			6.0	10	8		18		22		
t_h	Hold time	Data after CLK \uparrow	2.0	3	0		3		3		ns
			4.5	3	0		3		3		
			6.0	3	0		3		3		

AC Characteristics for HC: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER		V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HC534		GD54HC534		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
f_{max}	Maximum Clock Pulse Frequency		2.0	6	20		5		4		MHz
			4.5	30	65		25		20		
			6.0	35	75		30		25		
$t_{PLH}/$ t_{PHL}	Propagation Delay Time CLK to \overline{Q}_n		2.0		40	140		180		210	ns
			4.5		14	28		36		40	
			6.0		12	26		33		38	
$t_{PZH}/$ t_{PZL}	3-state Output Enable Time \overline{OE} to \overline{Q}_n		2.0		38	140		180		210	ns
			4.5		13	28		36		40	
			6.0		12	26		33		38	
$t_{PLZ}/$ t_{PHZ}	3-state Output disable time \overline{OE} to \overline{Q}_n		2.0		38	140		180		210	ns
			4.5		13	28		30		40	
			6.0		12	26		33		38	
$t_{TLH}/$ t_{THL}	Output Transition Time		2.0		15	60		75		90	ns
			4.5		6	12		15		18	
			6.0		5	10		13		15	

Timing Requirements for HCT: $t_r = t_f = 6\text{ns}$ $C_L = 50\text{pF}$

SYMBOL	PARAMETER		V_{CC} (V)	$T_A = 25^\circ\text{C}$			GD74HCT534		GD54HCT534		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_w	Pulse width	CLK high or low	4.5	16	10		20		25		ns
t_{su}	Setup time	Data before CLK↑	4.5	12	10		20		25		ns
t_h	Hold time	Data after CLK↑	4.5	3	0		3		3		ns

AC Characteristics for HCT: $t_r = t_f = 6\text{ns}$ $C_L = 50\text{ pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A = 25^\circ\text{C}$			GD74HCT534		GD54HCT534		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
f_{max}	Maximum Clock Pulse Frequency	4.5	27	54		22		18		MHz
$t_{PLH}/$ t_{PHL}	Propagation Delay Time CLK to \overline{Q}_n	4.5		16	30		38		44	ns
$t_{PZH}/$ t_{PZL}	3-state Output Enable Time \overline{OE} to \overline{Q}_n	4.5		15	30		38		45	ns
$t_{PLZ}/$ t_{PHZ}	3-state Output Disable Time \overline{OE} to \overline{Q}_n	4.5		15	30		38		45	ns
$t_{TLH}/$ t_{THL}	Output Transition Time	4.5		6	12		15		18	ns

AC Waveforms

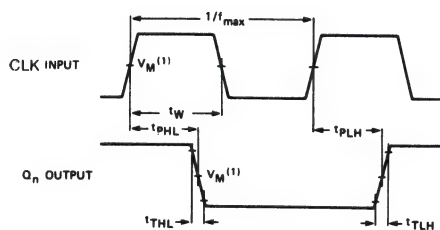


Fig. 2 Waveforms showing the clock (CLK) to output (Q_n) propagation delays, the clock pulse width, output transition times and the maximum clock pulse frequency.

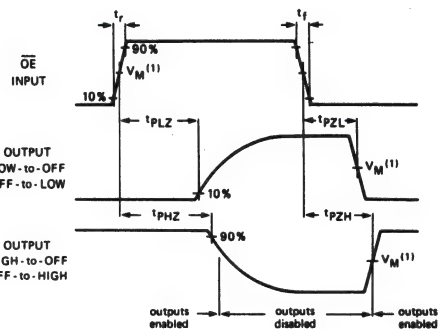


Fig. 3 Waveforms showing the 3-state enable and disable times.

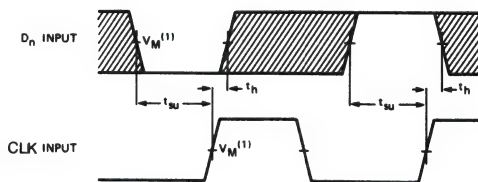


Fig. 4 Waveforms showing the data set-up and hold times for D_n input.

Note to Fig. 4

The shaded areas indicate when the input is permitted to change for predictable output performance.

Note to AC waveforms

(1) HC : $V_M = 50\%$; $V_I = \text{GND to } V_{CC}$.
HCT : $V_M = 1.3V$; $V_I = \text{GND to } 3V$.

GD54/74HC540, GD54/74HCT540

OCTAL INVERTING 3-STATE BUFFERS

General Description

These devices are identical in pinout to the 54/74LS540. These eight inverting buffers feature two NORed active-low output enables, inverting 3-state outputs, and inputs and outputs on opposite sides of the package. These octal inverting buffers/line drivers/line receivers are designed to be used with 3-state memory address drivers, clock drivers, and other bus-oriented systems. The HC/HCT 540 are similar in function to the HC/HCT 541 which have noninverting outputs. These devices are characterized for operation over wide temperature ranges to meet industry and military specifications.

Features

- Low Power consumption characteristic of CMOS devices
- Output drive capability: 15 LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts
for HCT 4.5 to 5.5 volts
- Low input current: 1 μ A Max.
- Low quiescent current: 80 μ A Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs

Logic Diagram

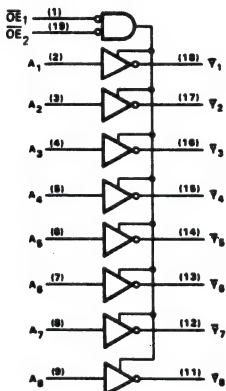
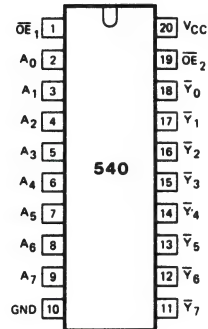


Fig. 1 Logic diagram

Pin Configuration



Suffix-Blank : Plastic Dual In Line Package
 Suffix-J : Ceramic Dual In Line Package
 Suffix-D : Small Outline Package

Function Table

INPUTS			OUTPUT
\overline{OE}_1	\overline{OE}_2	A_n	\overline{Y}_n
L	L	L	H
L	L	H	L
X	H	X	Z
H	X	X	Z

H= HIGH voltage level
 L= LOW voltage level
 X= don't care
 Z= high impedance OFF state

Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC Supply voltage		-0.5	+7	V
I_{IK}, I_{OK}	DC input or output diode current	for $V_I < -0.5$ or $V_I > V_{CC} + 0.5V$		20	mA
I_O	DC output source or sink current	for $-0.5V < V_O < V_{CC} + 0.5V$		35	mA
I_{CC}	DC V_{CC} or GND current			70	mA
T_{stg}	Storage temperature range		-65	150	°C
P_D	Power dissipation per package	above +70°C: derate linearly with 8mW/K		500	mW
T_L	Lead temperature	At distance $1/16 \pm 1/32$ in. from case for 60 sec(CERAMIC) 10 sec(PLASTIC)		300 260	°C

Recommended Operating Conditions

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range V_{CC} : GD54/74HC Types GD54/74HCT Types	2 4.5	6 5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A : GD74 Types GD54 Types	-40 -55	+85 +125	°C
Input Rise and Fall times t_r, t_f : GD54/74HC Types at 2V at 4.5V at 6V GD54/74HCT Types at 4.5V		1000 500 400 500	ns

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HC540		GD54HC540		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2		1.5 3.15 4.2		V
V _{IL}	LOW level input voltage		2.0 4.5 6.0			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH} or V _{IL}	I _{OH} =-20μA 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V
			I _{OH} =-6mA I _{OH} =-7.8mA 6.0	3.98 5.48	4.3 5.2		3.84 5.34		3.7 5.2		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH} or V _{IL}	I _{OL} =20μA 4.5 6.0			0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V
			I _{OL} =6mA I _{OL} =7.8mA 6.0		0.17 0.15	0.26 0.26		0.33 0.33		0.4 0.4	
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	6.0			0.1		1.0		1.0	μA
I _{OZ}	Three-State leakage current	V _{IN} =V _{IH} or V _{IL} V _O =V _{CC} or GND	6.0		0.01	0.5		5.0		10.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	6.0			8		80		160	μA

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HCT540		GD54HCT540		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		4.5 to 5.0	2.0			2.0		2.0		V
V _{IL}	LOW level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH} or V _{IL}	I _{OH} =-20μA 4.5	4.4	4.5		4.4		4.4		V
			I _{OH} =-6mA 4.5	3.98	4.3		3.84		3.7		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH} or V _{IL}	I _{OL} =20μA 4.5			0.1		0.1		0.1	V
			I _{OL} =6mA 4.5		0.17	0.26		0.33		0.4	
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	5.5			0.1		1.0		1.0	μA
I _{OZ}	Three-State leakage current	V _{IN} =V _{IH} or V _{IL} V _O =V _{CC} or GND	5.5		0.01	0.5		5.0		10.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	5.5			8		80		160	μA

AC Characteristics for HC: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HC540		GD54HC540		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} / t_{PHL}	Propagation Delay Time A_n to \overline{Y}_n	2.0		30	100		120		140	ns
		4.5		9	18		24		28	
		6.0		8	16		20		25	
t_{PZH} t_{PZL}	3-state output Enable Time \overline{OE}_n to \overline{Y}_n	2.0		45	140		180		210	ns
		4.5		18	32		40		45	
		6.0		16	28		36		40	
t_{PLZ} / t_{PHZ}	3-state Output Disable Time \overline{OE}_n to \overline{Y}_n	2.0		45	140		180		210	ns
		4.5		18	32		40		48	
		6.0		16	28		36		42	
t_{TLH} / t_{THL}	Output Transition Time	2.0		15	60		75		90	ns
		4.5		6	12		15		18	
		6.0		5	10		13		15	

AC Characteristics for HCT: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HCT540		GD54HCT540		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} / t_{PHL}	Propagation Delay Time A_n to \overline{Y}_n	4.5		12	22		26		30	ns
t_{PZH} t_{PZL}	3-state output Enable Time \overline{OE}_n to \overline{Y}_n	4.5		19	34		42		48	ns
t_{PLZ} / t_{PHZ}	3-state Output Disable Time \overline{OE}_n to \overline{Y}_n	4.5		19	34		42		48	ns
t_{TLH} / t_{THL}	Output Transition Time	4.5		7	12		15		18	ns

AC Waveforms

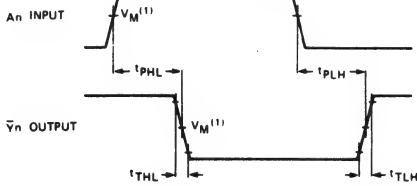


Fig. 2 Waveforms showing the input (A_n) to output (\bar{Y}_n) propagation delays and the output transition times.

Note to AC waveforms

- (1) HC : $V_M=50\%$; $V_I=GND$ to V_{CC} .
HCT : $V_M=1.3V$; $V_I=GND$ to $3V$.

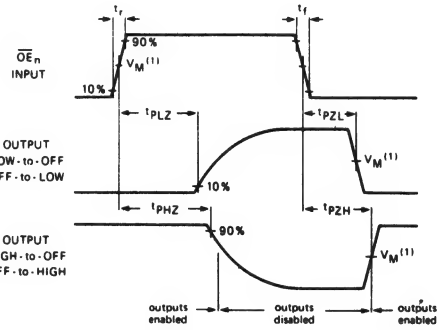


Fig. 3 Waveforms showing the 3-state enable and disable times.

GD54/74HC541, GD54/74HCT541

OCTAL NONINVERTING 3-STATE BUFFERS

General Description

These devices are identical in pinout to the 54/74LS541. These eight noninverting buffers feature two NORed active-low output enables, noninverting 3-state outputs, and inputs and outputs on opposite sides of the package. These octal noninverting buffers/line drivers/line receivers are designed to be used with 3-state memory address drivers, clock drivers, and other bus-oriented systems. The HC/HCT 541 are similar in function to the HC/HCT 540 which have inverting outputs. These devices are characterized for operation over wide temperature ranges to meet industry and military specifications.

Features

- Low Power consumption characteristic of CMOS devices
- Output drive capability: 15 LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts
for HCT 4.5 to 5.5 volts
- Low input current: 1 μ A Max.
- Low quiescent current: 80 μ A Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs

Logic Diagram

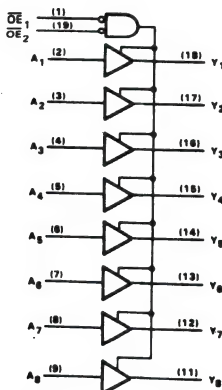
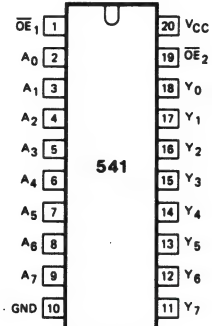


Fig. 1 Logic diagram

Pin Configuration



Suffix-Blank : Plastic Dual In Line Package
 Suffix-J : Ceramic Dual In Line Package
 Suffix-D : Small Outline Package

Function Table

INPUTS			OUTPUT
\overline{OE}_1	\overline{OE}_2	A_n	Y_n
L	L	L	L
L	L	H	H
X	H	X	Z
H	X	X	Z

H= HIGH voltage level
 L= LOW voltage level
 X= don't care
 Z= high impedance OFF state

Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC Supply voltage		-0.5	+7	V
I_{IK}, I_{OK}	DC input or output diode current	for $V_I < -0.5$ or $V_I > V_{CC} + 0.5V$		20	mA
I_O	DC output source or sink current	for $-0.5V < V_O < V_{CC} + 0.5V$		35	mA
I_{CC}	DC V_{CC} or GND current			70	mA
T_{stg}	Storage temperature range		-65	150	°C
P_D	Power dissipation per package	above +70°C: derate linearly with 8mW/K		500	mW
T_L	Lead temperature	At distance $1/16 \pm 1/32$ in. from case for 60 sec(CERAMIC) 10 sec(PLASTIC)		300 260	°C

Recommended Operating Conditions

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range V_{CC} : GD54/74HC Types GD54/74HCT Types	2 4.5	6 5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A : GD74 Types GD54 Types	-40 -55	+85 +125	°C
Input Rise and Fall times t_r, t_f : GD54/74HC Types at 2V at 4.5V at 6V GD54/74HCT Types at 4.5V		1000 500 400 500	ns

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HC541		GD54HC541		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2		1.5 3.15 4.2		V
V _{IL}	LOW level input voltage		2.0 4.5 6.0			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH}	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V
		or V _{IL}									
V _{OL}	LOW level output voltage	V _{IN} =V _{IH}	2.0 4.5 6.0			0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V
		or V _{IL}									
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	6.0			0.1		1.0		1.0	μA
I _{OZ}	Three-State leakage current	V _{IN} =V _{IH} or V _{IL} V _O =V _{CC} or GND	6.0		0.01	0.5		5.0		10.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	6.0			8		80		160	μA

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HCT541		GD54HCT541		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		4.5 to 5.0	2.0			2.0		2.0		V
V _{IL}	LOW level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH}	4.5	4.4	4.5		4.4		4.4		V
		or V _{IL}									
V _{OL}	LOW level output voltage	V _{IN} =V _{IH}	4.5			0.1		0.1		0.1	V
		or V _{IL}									
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	5.5			0.1		1.0		1.0	μA
I _{OZ}	Three-State leakage current	V _{IN} =V _{IH} or V _{IL} V _O =V _{CC} or GND	5.5		0.01	0.5		5.0		10.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	5.5			8		80		160	μA

AC Characteristics for HC: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HC541		GD54HC541		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} / t_{PHL}	Propagation Delay Time An to \bar{Y}_n	2.0		30	100		120		140	ns
		4.5		9	18		24		28	
		6.0		8	16		20		25	
t_{PZH} / t_{PZL}	3-state Output Enable Time $\bar{O}E_n$ to \bar{Y}_n	2.0		45	140		180		210	ns
		4.5		18	32		40		45	
		6.0		16	28		36		40	
t_{PLZ} / t_{PHZ}	3-state Output Disable Time $\bar{O}E_n$ to \bar{Y}_n	2.0		45	140		180		210	ns
		4.5		18	32		40		48	
		6.0		16	28		36		42	
t_{TLH} / t_{THL}	Output Transition Time	2.0		15	60		75		90	ns
		4.5		6	12		15		18	
		6.0		5	10		13		15	

AC Characteristics for HCT: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD54HCT541		GD54HCT541		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} / t_{PHL}	Propagation Delay Time An to \bar{Y}_n	4.5		12	22		26		30	ns
t_{PZH} / t_{PZL}	3-state Output Enable Time $\bar{O}E_n$ to \bar{Y}_n	4.5		19	34		42		48	ns
t_{PLZ} / t_{PHZ}	3-state Output Disable Time $\bar{O}E_n$ to \bar{Y}_n	4.5		19	34		42		48	ns
t_{TLH} / t_{THL}	Output Transition Time	4.5		7	12		15		18	ns

AC Waveforms

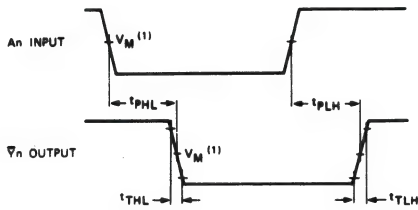


Fig. 2 Waveforms showing the input (An) to output (Yn) propagation delays and the output transition times.

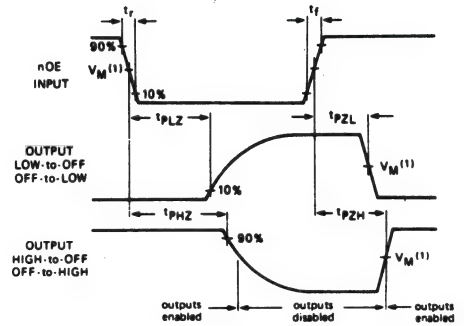


Fig. 3 Waveforms showing the 3-state enable and disable times.

Note to AC waveforms

- (1) HC : $V_M = 50\%$; $V_I = \text{GND to } V_{CC}$.
HCT : $V_M = 1.3V$; $V_I = \text{GND to } 3V$.

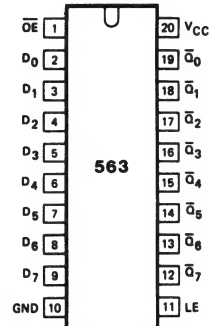
GD54/74HC563, GD54/74HCT563

OCTAL 3-STATE INVERTING D-TYPE TRANSPARENT LATCHES

General Description

These devices are identical in pinout to the 54/74LS563. They contain eight D-type latches, one latch enable, and one output control. These latches appear transparent to data, i.e., The outputs change asynchronously, when latch enable is high. when it is high, all outputs go to the high impedance time becomes latched. The output enable input does not affect the state of the latches when it is low. But when it is high, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements. The HC/HCT 563 are similar in function to the HC/HCT 573 which have noninverting outputs. These devices are characterized for operation over wide temperature ranges to meet industry and military specifications.

Pin Configuration



Suffix-Blank : Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package
Suffix-D : Small Outline Package

Features

- Low Power consumption characteristic of CMOS devices
- Output drive capability: 15 LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts
for HCT 4.5 to 5.5 volts
- Low input current: 1 μ A Max.
- Low quiescent current: 80 μ A Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs

Function Table

OPERATING MODES	INPUTS			INTERNAL LATCHES	OUTPUTS \bar{Q}_0 to \bar{Q}_7
	\bar{OE}	LE	D_n		
enable and read register	L	H	L	L	H
	L	H	H	H	L
latch and read register	L	L	L	L	H
	L	L	H	H	L
latch register and disable outputs	H	L	L	L	Z
	H	L	H	H	Z

H = HIGH voltage level

h = HIGH voltage level one set-up time prior to the LOW-to-HIGH LE transition

L = LOW voltage level

l = LOW voltage level one set-up time prior to the LOW-to-HIGH LE transition

Z = high impedance OFF-state

Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC Supply voltage		-0.5	+7	V
I_{IK}, I_{OK}	DC input or output diode current	for $V_I < -0.5$ or $V_I > V_{CC} + 0.5V$		20	mA
I_O	DC output source or sink current	for $-0.5V < V_O < V_{CC} + 0.5V$		35	mA
I_{CC}	DC V_{CC} or GND current			70	mA
T_{stg}	Storage temperature range		-65	150	°C
P_D	Power dissipation per package	above +70°C: derate linearly with 8mW/K		500	mW
T_L	Lead temperature	At distance 1/16 ± 1/32 in. from case for 60 sec(CERAMIC) 10 sec(PLASTIC)		300 260	°C

Recommended Operating Conditions

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range V_{CC} : GD54/74HC Types GD54/74HCT Types	2 4.5	6 5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A : GD74 Types GD54 Types	-40 -55	+85 +125	°C
Input Rise and Fall times t_r, t_f : GD54/74HC Types at 2V at 4.5V at 6V GD54/74HCT Types at 4.5 V		1000 500 400 500	ns

Logic Diagram

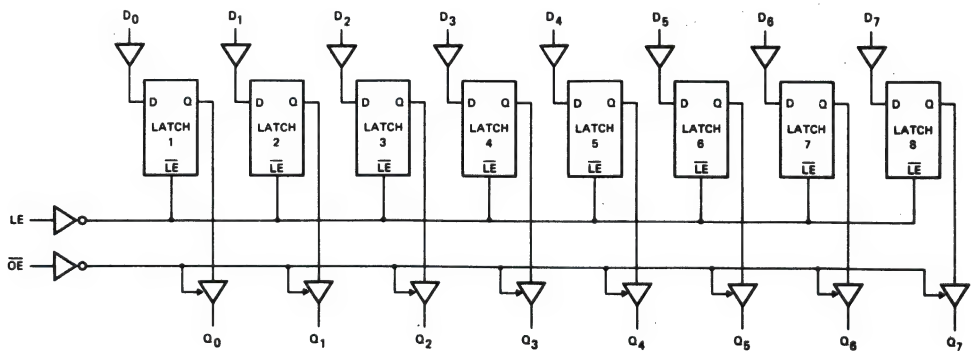


Fig. 1 Logic diagram.

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A = 25°C			GD74HC563		GD54HC563		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2		1.5 3.15 4.2		V
V _{IL}	LOW level input voltage		2.0 4.5 6.0			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V
V _{OH}	HIGH level output voltage	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -20μA	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0	1.9 4.4 5.9		1.9 4.4 5.9		V
			I _{OH} = -6mA	4.5 6.0	3.98 5.48	4.3 5.2	3.84 5.34		3.7 5.2		
			I _{OH} = -7.8mA								
V _{OL}	LOW level output voltage	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 20μA	2.0 4.5 6.0			0.1 0.1 0.1	0.1 0.1 0.1		0.1 0.1 0.1	V
			I _{OL} = 6mA	4.5 6.0		0.17 0.15	0.26 0.26	0.33 0.33		0.4 0.4	
			I _{OL} = 7.8mA								
I _{IN}	Input leakage Current	V _{IN} = V _{CC} or GND	6.0			0.1		1.0		1.0	μA
I _{OZ}	Three-State leakage current	V _{IN} = V _{IH} or V _{IL} V _O = V _{CC} or GND	6.0		0.01	0.5		5.0		10.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} = V _{CC} or GND I _{out} = 0μA	6.0			8		80		160	μA

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A = 25°C			GD74HCT563		GD54HCT563		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		4.5 to 5.0	2.0			2.0		2.0		V
V _{IL}	LOW level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V _{OH}	HIGH level output voltage	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -20μA	4.5	4.4	4.5	4.4		4.4		V
			I _{OH} = -6mA	4.5	3.98	4.3	3.84		3.7		
V _{OL}	LOW level output voltage	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 20μA	4.5			0.1	0.1		0.1	V
			I _{OL} = 6mA	4.5		0.17	0.26	0.33		0.4	
I _{IN}	Input leakage Current	V _{IN} = V _{CC} or GND	5.5			0.1		1.0		1.0	μA
I _{OZ}	Three-State leakage current	V _{IN} = V _{IH} or V _{IL} V _O = V _{CC} or GND	5.5		0.01	0.5		5.0		10.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} = V _{CC} or GND I _{out} = 0μA	5.5			8		80		160	μA

Timing Requirements for HC: $t_r = t_f = 6\text{ns}$ $C_L = 50\text{ pF}$

SYMBOL	PARAMETER		V_{CC} (V)	$T_A = 25^\circ\text{C}$			GD74HC563		GD54HC563		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_w	Pulse width	LE high	2.0	80	30		100		120		ns
			4.5	16	10		20		25		
			6.0	14	8		18		22		
t_{su}	Setup time	Data before LE ↓	2.0	60	30		100		120		ns
			4.5	12	10		20		25		
			6.0	10	8		18		22		
t_h	Hold time	Data after LE ↓	2.0	3	0		3		3		ns
			4.5	3	0		3		3		
			6.0	3	0		3		3		

AC Characteristics for HC: $t_r = t_f = 6\text{ns}$ $C_L = 50\text{ pF}$

SYMBOL	PARAMETER		V_{CC} (V)	$T_A = 25^\circ\text{C}$			GD74HC563		GD54HC563		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
$t_{PLH}/$ t_{PHL}	Propagation Delay Time D_n to \overline{Q}_n		2.0		40	140		180		210	ns
			4.5		14	28		36		40	
			6.0		12	26		33		38	
$t_{PLH}/$ t_{PHL}	Propagation Delay Time LE to \overline{Q}_n		2.0		42	150		190		220	ns
			4.5		16	32		42		50	
			6.0		14	30		38		45	
$t_{PZH}/$ t_{PZL}	3-state Output Enable Time \overline{OE} to \overline{Q}_n		2.0		45	150		190		220	ns
			4.5		15	30		38		45	
			6.0		14	26		33		38	
$t_{PLZ}/$ t_{PHZ}	3-state Output Disable Time \overline{OE} to \overline{Q}_n		2.0		45	150		190		220	ns
			4.5		15	30		38		45	
			6.0		14	26		33		38	
$t_{TLH}/$ t_{THL}	Output Transition Time		2.0		15	60		75		90	ns
			4.5		6	12		15		18	
			6.0		5	10		13		15	

Timing Requirements for HCT, $t_r=t_f=6\text{ns}$ $C_L=50\text{pF}$

SYMBOL	PARAMETER		V_{CC}	$T_A=25^\circ\text{C}$			GD74HCT563		GD54HCT563		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_w	Pulse width	LE high	4.5	16	10		20		25		ns
t_{su}	Setup time	Data after LE \downarrow	4.5	12	10		20		25		ns
t_h	Hold time	Data before LE \downarrow	4.5	3	0		3		3		ns

AC Characteristics for HCT: $t_r=t_f=6\text{ns}$ $C_L=50\text{pF}$

SYMBOL	PARAMETER	V_{CC}	$T_A=25^\circ\text{C}$			GD74HCT563		GD54HCT563		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
$t_{PLH}/$ t_{PHL}	Propagation Delay Time D_n to \overline{Q}_n	4.5		16	30		38		44	ns
$t_{PLH}/$ t_{PHL}	Propagation Delay Time LE to \overline{Q}_n	4.5		19	35		42		48	ns
$t_{PZH}/$ t_{PZL}	3-state Output Enable Time \overline{OE} to \overline{Q}_n	4.5		15	30		38		45	ns
$t_{PLZ}/$ t_{PHZ}	3-state Output Disable Time \overline{OE} to \overline{Q}_n	4.5		15	30		38		45	ns
$t_{TLH}/$ t_{THL}	Output Transition Time	4.5		6	12		15		18	ns

AC Waveforms

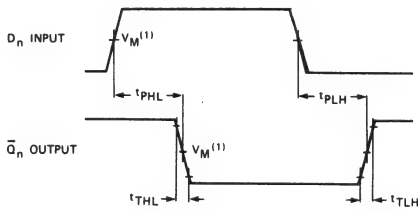


Fig. 2 Waveforms showing the data input (D_n) to output (\bar{Q}_n) propagation delays and the output transition times.

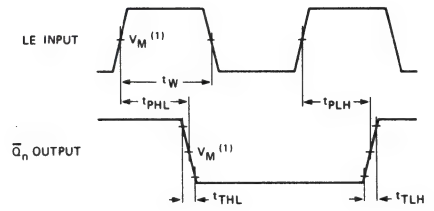


Fig. 3 Waveforms showing the latch enable input (LE) pulse width, the latch enable input to output (\bar{Q}_n) propagation delays and the output transition times.

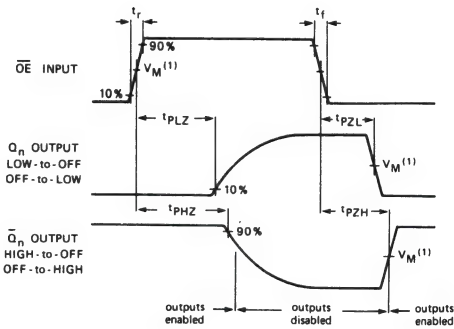


Fig. 4 Waveforms showing the 3-state enable and disable time.

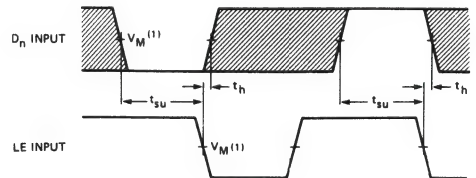


Fig. 5 Waveforms showing the data set-up and hold times for D_n input to LE input.

Note to AC waveforms

- (1) HC : $V_M = 50\%$; $V_I = \text{GND to } V_{CC}$.
HCT: $V_M = 1.3V$; $V_I = \text{GND to } 3V$.

Note to Fig. 5

The shaded areas indicate when the input is permitted to change for predictable output performance.

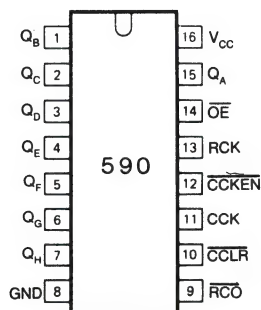
GD54/74HC590, GD54/74HCT590

8-BIT BINARY COUNTER WITH 3-STATE OUTPUT REGISTER

General Description

These devices are identical in pinout to the 54/74LS590. They contain an 8-bit binary counter which feeds an 8-bit register having 3-state output. The storage register has parallel outputs. Separate clocks are provided for both the binary counter and storage register. For cascading, a ripple carry output is provided. Expansion is easily accomplished for two stages by connecting the ripple carry output of the first stage to the counter clock enable of the second stage. Cascading for larger count chains can be accomplished by connecting the ripple carry output of each stage to the count clock of the following stage. Both the counter and register are positive-edge triggered. These devices are characterized for operation over wide temperature ranges to meet industry and military specifications.

Pin Configuration



Suffix-Blank : Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package
Suffix-D : Small Outline Package

Features

- Low Power consumption characteristic of CMOS devices
- Output drive capability: 15 LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts
for HCT 4.5 to 5.5 volts
- Low input current: $1\mu A$ Max.
- Low quiescent current: $80\mu A$ Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs

Logic Diagram

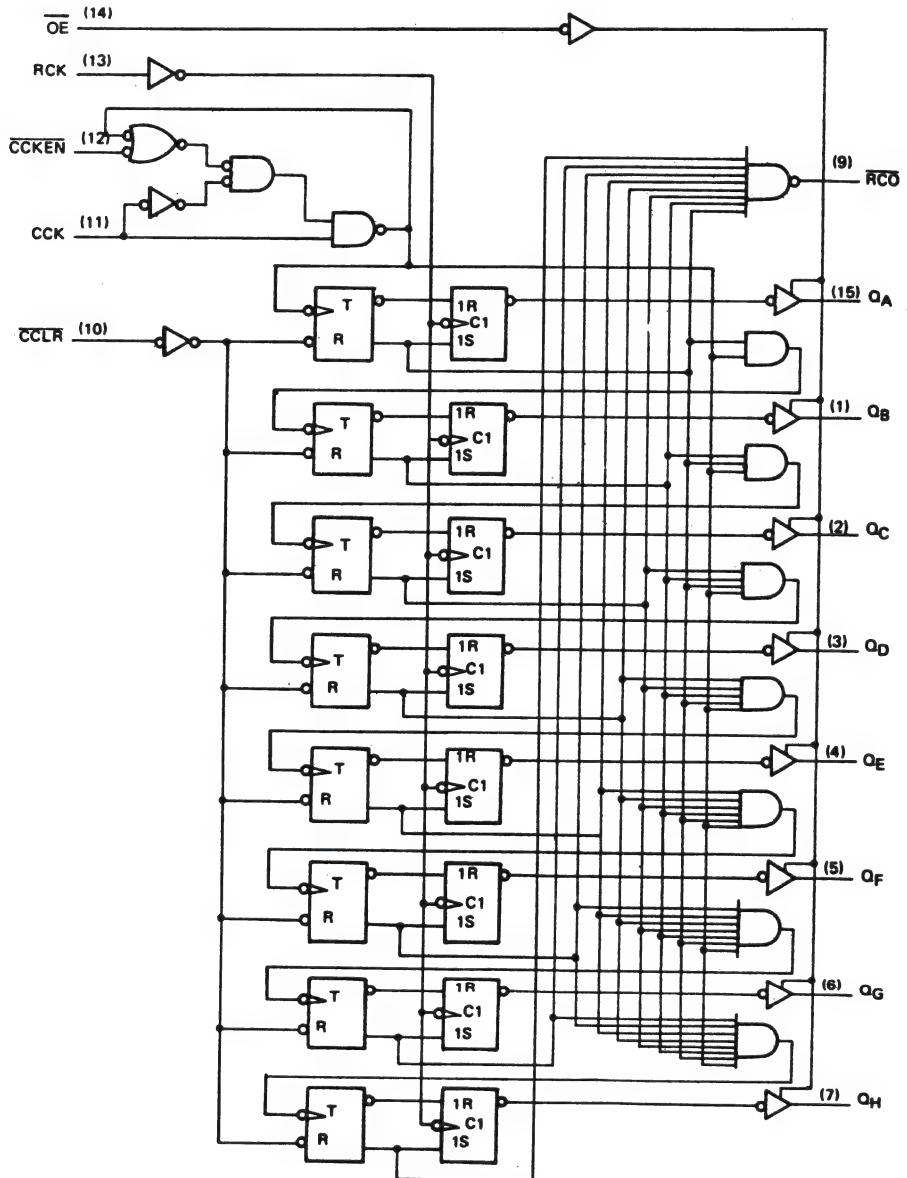


Fig. 1 Logic diagram

Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC Supply voltage		-0.5	+7	V
I_{IK}, I_{OK}	DC input or output diode current	for $V_I < -0.5$ or $V_I > V_{CC} + 0.5V$		20	mA
I_O	DC output source or sink current	for $-0.5V < V_O < V_{CC} + 0.5V$		35	mA
I_{CC}	DC V_{CC} or GND current			70	mA
T_{stg}	Storage temperature range		-65	150	°C
P_D	Power dissipation per package	above +70°C: derate linearly with 8mW/K		500	mW
T_L	Lead temperature	At distance 1/16 ± 1/32 in. from case for 60 sec(CERAMIC) 10 sec(PLASTIC)		300 260	°C

Recommended Operating Conditions

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range V_{CC} : GD54/74HC Types GD54/74HCT Types	2 4.5	6 5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A : GD74 Types GD54 Types	-40 -55	+85 +125	°C
Input Rise and Fall times t_r, t_f : GD54/74HC Types at 2V at 4.5V at 6V GD54/74HCT Types at 4.5V		1000 500 400 500	ns

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HC590		GD54HC590		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2		1.5 3.15 4.2		V
V _{IL}	LOW level input voltage		2.0 4.5 6.0			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH} or V _{IL}	I _{OH} = -20μA	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0	1.9 4.4 5.9		1.9 4.4 5.9		V
			I _{OH} = -6mA	4.5 6.0	3.98 5.48	4.3 5.2	3.84 5.34		3.7 5.2		
			I _{OH} = -7.8mA	6.0	5.48	5.2	5.34		5.2		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH} or V _{IL}	I _{OL} =20μA	2.0 4.5 6.0		0.1 0.1 0.1	0.1 0.1 0.1		0.1 0.1 0.1		V
			I _{OL} =6mA	4.5 6.0		0.17 0.15	0.26 0.26		0.33 0.33		
			I _{OL} =7.8mA	6.0		0.15	0.26		0.33		
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	6.0			0.1		1.0		1.0	μA
I _{OZ}	Three-State leakage current	V _{IN} =V _{IH} or V _{IL} V _O =V _{CC} or GND	6.0		0.01	0.5		5.0		10.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	6.0			8		80		160	μA

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HCT590		GD54HCT590		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		4.5 to 5.0	2.0			2.0		2.0		V
V _{IL}	LOW level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH} or V _{IL}	I _{OH} = -20μA	4.5	4.4	4.5	4.4		4.4		V
			I _{OH} = -6mA	4.5	3.98	4.3	3.84		3.7		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH} or V _{IL}	I _{OL} =20μA	4.5		0.1		0.1		0.1	V
			I _{OL} =6mA	4.5		0.17		0.33		0.4	
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	5.5			0.1		1.0		1.0	μA
I _{OZ}	Three-State leakage current	V _{IN} =V _{IH} or V _{IL} V _O =V _{CC} or GND	5.5		0.01	0.5		5.0		10.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	5.5			8		80		160	μA

Timing Requirements for HC: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER		V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HC590		GD54HC590		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_w	Pulse Width	CLK (High or low)	2.0	80	30		100		120		ns
			4.5	16	10		20		25		
			6.0	14	8		18		22		
		$\overline{\text{CCLR}}$ (low)	2.0	100	35		150		180		ns
			4.5	20	14		30		36		
			6.0	18	12		25		30		
t_{su}	Set up time	$\overline{\text{CCKEN}}$ low before CLK \uparrow	2.0	80	30		100		120		ns
			4.5	16	10		20		25		
			6.0	14	8		18		22		
		$\overline{\text{CCLR}}$ inactive before CLK \uparrow	2.0	80	30		100		120		ns
			4.5	16	10		20		25		
			6.0	14	8		18		22		
t_h	Hold time	CLK before RCK \uparrow	2.0	100	35		150		180		ns
			4.5	20	14		30		36		
			6.0	18	12		26		30		
		$\overline{\text{CCKEN}}$ low after CLK \uparrow	2.0	3	3		3		3		ns
			4.5	3	0		3		3		
			6.0	3	0		3		3		

AC Characteristics for HC: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER		V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HC590		GD54HC590		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
f_{max}	Maximum Clock Pulse Frequency		2.0	5	18		4		3		MHz
			4.5	20	50		18		16		
			6.0	30	60		25		20		
$t_{\text{PLH}}/$ t_{PHL}	Propagation Delay Time CLK to $\overline{\text{RCO}}$		2.0		50	170		210		250	ns
			4.5		17	30		40		50	
			6.0		16	28		35		45	
t_{PLH}	Propagation Delay Time $\overline{\text{CCLR}}$ to $\overline{\text{RCO}}$		2.0		60	180		220		260	ns
			4.5		25	40		48		55	
			6.0		22	38		46		52	
$t_{\text{PLH}}/$ t_{PHL}	Propagation Delay Time RCK to Q_n		2.0		50	170		210		250	ns
			4.5		17	30		40		50	
			6.0		16	28		35		45	
$t_{\text{PZH}}/$ t_{PZL}	3-state Output Enable Time $\overline{\text{OE}}$ to Q_n		2.0		60	180		220		260	ns
			4.5		25	40		48		55	
			6.0		22	38		46		52	
$t_{\text{PHZ}}/$ t_{PLZ}	3-state Output Disable Time $\overline{\text{OE}}$ to Q_n		2.0		58	180		220		260	ns
			4.5		24	40		48		55	
			6.0		22	38		46		52	
$t_{\text{TLH}}/$ t_{THL}	Output Transition Time		2.0		15	60		75		90	ns
			4.5		6	12		15		18	
			6.0		5	10		13		15	

Timing Requirements for HCT: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER		V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HCT590		GD54HCT590		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_w	Pulse Width	CLK (High or low)	4.5	16	10		20		25		ns
		$\overline{\text{CCLR}}$ (low)	4.5	20	14		30		36		ns
		RCK (High or low)	4.5	20	14		30		36		ns
t_{su}	Set up time	$\overline{\text{CKEN}}$ low before CLK \uparrow	4.5	16	10		20		25		ns
		$\overline{\text{CCLR}}$ inactive before CLK \uparrow	4.5	16	10		20		25		ns
		CLK before RCK \uparrow	4.5	20	14		30		36		ns
t_h	Hold time	$\overline{\text{CKEN}}$ low after CLK \uparrow	4.5	3	0		3		3		ns

AC Characteristics for HCT: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HCT590		GD54HCT590		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
f_{max}	Maximum Clock Pulse Frequency	4.5	18	45		16		15		MHz
$t_{PLH}/$ t_{PHL}	Propagation Delay Time CLK to $\overline{\text{RCO}}$	4.5		19	35		45		52	ns
$t_{PLH}/$ t_{PHL}	Propagation Delay Time $\overline{\text{CCLR}}$ to $\overline{\text{RCO}}$	4.5		26	42		50		58	ns
$t_{PLH}/$ t_{PHL}	Propagation Delay Time RCK to Q_n	4.5		19	35		45		52	ns
$t_{PZH}/$ t_{PZL}	3-state Output Enable Time $\overline{\text{OE}}$ to Q_n	4.5		26	42		50		58	ns
$t_{PHZ}/$ t_{PLZ}	3-state Output Disable Time $\overline{\text{OE}}$ to Q_n	4.5		25	42		50		58	ns
$t_{TLH}/$ t_{THL}	Output Transition Time	4.5		7	12		15		18	ns

AC Waveforms

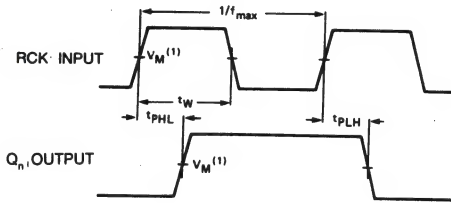


Fig. 2 Waveforms showing the RCK input to Q_n output propagation delays, the RCK pulse width and maximum clock pulse frequency.

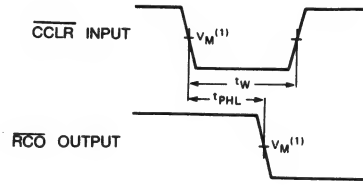


Fig. 3 Waveforms showing the \overline{CCLR} input to \overline{RCO} output propagation delay and the \overline{CCLR} pulse width.

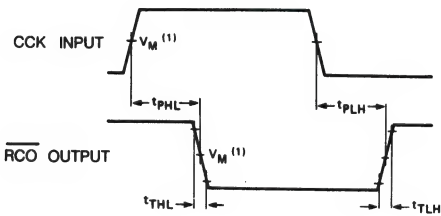


Fig. 4 Waveforms showing the data input (CCK) to output (\overline{RCO}) propagation delays and the output transition times.

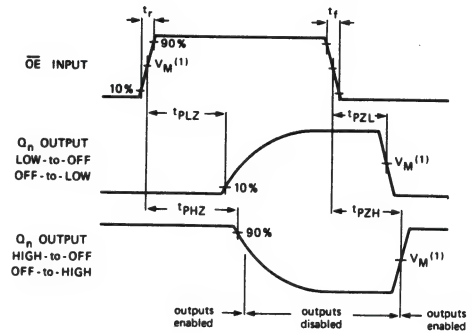


Fig. 5 Waveforms showing the 3-state enable and disable times.

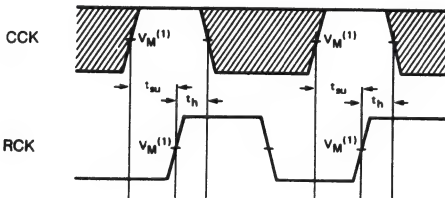
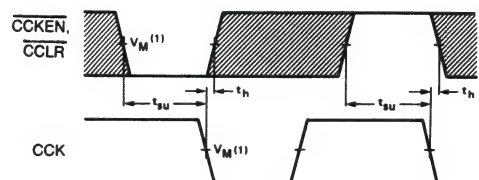


Fig. 6 Waveforms showing hold and set-up times for CCK inputs to RCK input and CCKEN, CCLR inputs to CCK input.



Note to Fig. 6

The shaded areas indicate when the input is permitted to change for predictable output performance.

Note to AC waveforms

- (1) HC : $V_M = 50\%$; $V_I = \text{GND to } V_{CC}$
HCT : $V_M = 1.3V$; $V_I = \text{GND to } 3V$.

GD54/74HC640, GD54/74HCT640

OCTAL INVERTING 3-STATE TRANSCEIVERS

General Description

These devices are identical in pinout to the 54/74LS640. They consist of eight transceivers which are designed for asynchronous two-way communications between data buses. Each device has inverting outputs, and has an active-low output enable which is used to place the I/O ports into high impedance states. The direction control determines the directions of data flow. When it is high, data flow from A to B; when it is low, data flow from B to A. Refer to the other devices for similar functionalities;

The HC/HCT 245 All Noninverting outputs

The HC/HCT 643 4 Inverting &

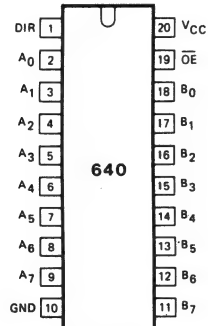
4 Noninverting outputs.

These devices are characterized for operation over wide temperature ranges to meet industry and military specifications.

Features

- Low Power consumption characteristic of CMOS devices
- Output drive capability: 15 LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts
for HCT 4.5 to 5.5 volts
- Low input current: $1\mu\text{A}$ Max.
- Low quiescent current: $80\mu\text{A}$ Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs

Pin Configuration



Suffix-Blank : Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package
Suffix-D : Small Outline Package

Function Table

INPUTS		INPUTS/OUTPUTS	
$\overline{\text{OE}}$	DIR	A _n	B _n
L	L	A = $\overline{\text{B}}$	inputs
L	H	inputs	B = $\overline{\text{A}}$
H	X	Z	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC Supply voltage		-0.5	+7	V
I_{IK}, I_{OK}	DC input or output diode current	for $V_I < -0.5$ or $V_I > V_{CC} + 0.5V$		20	mA
I_O	DC output source or sink current	for $-0.5V < V_O < V_{CC} + 0.5V$		35	mA
I_{CC}	DC V_{CC} or GND current			70	mA
T_{stg}	Storage temperature range		-65	150	°C
P_D	Power dissipation per package	above +70°C: derate linearly with 8mW/K		500	mW
T_L	Lead temperature	At distance 1/16 ± 1/32 in. from case for 60 sec(CERAMIC) 10 sec(PLASTIC)		300 260	°C

Recommended Operating Conditions

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range V_{CC} : GD54/74HC Types GD54/74HCT Types	2 4.5	6 5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A : GD74 Types GD54 Types	-40 -55	+85 +125	°C
Input Rise and Fall times t_r, t_f : GD54/74HC Types at 2V at 4.5V at 6V GD54/74HCT Types at 4.5V		1000 500 400 500	ns

Logic Diagram

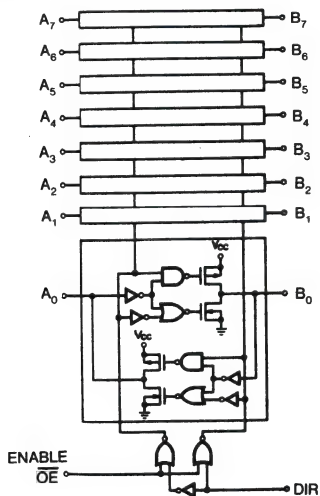


Fig. 1 Logic diagram

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HC640		GD54HC640		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2		1.5 3.15 4.2		V
V _{IL}	LOW level input voltage		2.0 4.5 6.0			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH} or V _{IL}									V
			I _{OH} =−20μA	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0	1.9 4.4 5.9		1.9 4.4 5.9		
			I _{OH} =−6mA I _{OH} =−7.8mA	4.5 6.0	3.98 5.48	4.3 5.2	3.84 5.34		3.7 5.2		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH} or V _{IL}									V
			I _{OL} =20μA	2.0 4.5 6.0		0.1 0.1 0.1	0.1 0.1 0.1		0.1 0.1 0.1		
			I _{OL} =6mA I _{OL} =7.8mA	4.5 6.0	0.17 0.15	0.26 0.26	0.33 0.33		0.4 0.4		
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	6.0			0.1		1.0		1.0	μA
I _{OZ}	Three-State leakage current	V _{IN} =V _{IH} or V _{IL} V _O =V _{CC} or GND	6.0		0.01	0.5		5.0		10.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	6.0			8		80		160	μA

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HCT640		GD54HCT640		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		4.5 to 5.0	2.0			2.0		2.0		V
V _{IL}	LOW level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH} or V _{IL}	I _{OH} =−20μA	4.5	4.4	4.5	4.4		4.4		V
			I _{OH} =−6mA	4.5	3.98	4.3	3.84		3.7		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH} or V _{IL}	I _{OL} =20μA	4.5		0.1		0.1		0.1	V
			I _{OL} =6mA	4.5		0.17		0.33		0.4	
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	5.5			0.1		1.0		1.0	μA
I _{OZ}	Three-State leakage current	V _{IN} =V _{IH} or V _{IL} V _O =V _{CC} or GND	5.5		0.01	0.5		5.0		10.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	5.5			8		80		160	μA

AC Characteristics for HC: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HC640		GD54HC640		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} / t_{PHL}	Propagation Delay Time An to Bn, Bn to An	2.0		30	100		120		140	ns
		4.5		10	20		25		30	
		6.0		9	18		22		26	
t_{PZH} / t_{PZL}	3-state Output Enable Time \overline{OE} , DIR to An \overline{OE} , DIR to Bn	2.0		45	140		180		210	ns
		4.5		18	30		38		45	
		6.0		16	26		32		38	
t_{PLZ} / t_{PHZ}	3-state Output Disable Time \overline{OE} , DIR to An \overline{OE} , DIR to Bn	2.0		45	140		180		210	ns
		4.5		18	30		38		45	
		6.0		16	26		32		38	
t_{TLH} / t_{THL}	Output Transition Time	2.0		15	60		75		90	ns
		4.5		6	12		15		18	
		6.0		5	10		13		15	

AC Characteristics for HCT: $t_r=t_f=6\text{ns}$ $C_L=50\text{pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD54HCT640		GD74HCT640		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} / t_{PHL}	Propagation Delay Time An to Bn, Bn to An	4.5		13	26		28		32	ns
t_{PZH} / t_{PZL}	3-state Output Enable Time \overline{OE} , DIR to An \overline{OE} , DIR to Bn	4.5		19	35		45		52	ns
t_{PLZ} / t_{PHZ}	3-state Output Disable Time \overline{OE} , DIR to An \overline{OE} , DIR to Bn	4.5		19	35		45		52	ns
t_{TLH} / t_{THL}	Output Transition Time	4.5		7	12		15		18	ns

AC Waveforms

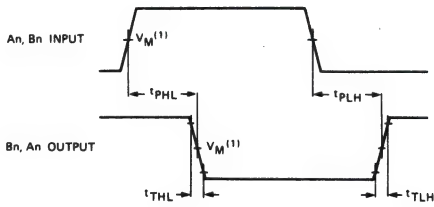


Fig. 2 Waveforms showing the input (A_n , B_n) to output (B_n , A_n) propagation delays and the output transition times

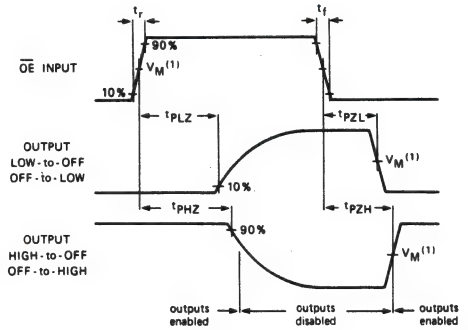


Fig. 3 Waveforms showing the 3-state enable and disable times

Note to AC waveforms

- (1) HC : $V_M = 50\%$; $V_i = \text{GND to } V_{CC}$.
HCT : $V_M = 1.3V$; $V_i = \text{GND to } 3V$.

GD54/74HC643, GD54/74HCT643

OCTAL INVERTING & NONINVERTING 3-STATE TRANSCEIVERS

General Description

These devices are identical in Pinout to the 54/74LS643. They consist of eight transceivers which are designed for Asynchronous two-way communications between Data buses. Each device has 4 inverting and 4 noninverting outputs with Active Low output enable which is used to place the I/O ports into High impedance states.

The direction control determines the directions of Data flow. When it is high, Data flow From A to B; When it is low, Data flow from B to A.

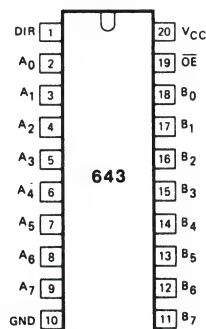
Refer to the other devices for similar functionalities;

The HC/HCT245 All noninverting outputs

The HC/HCT640 All inverting outputs.

These devices are characterized for operation over wide temperature ranges to meet industry and military specifications.

Pin Configuration



Suffix-Blank : Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package
Suffix-D : Small Outline Package

Features

- Low Power consumption characteristic of CMOS devices
- Output drive capability: 15 LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts
for HCT 4.5 to 5.5 volts
- Low input current: $1\mu\text{A}$ Max.
- Low quiescent current: $80\mu\text{A}$ Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs

Function Table

INPUTS		INPUTS/OUTPUTS	
$\overline{\text{OE}}$	DIR	A_n	B_n
L	L	$A=B$	inputs
L	H	inputs	$B=\bar{A}$
H	X	Z	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC Supply voltage		-0.5	+7	V
I_{IK}, I_{OK}	DC input or output diode current	for $V_I < -0.5$ or $V_I > V_{CC} + 0.5V$		[20]	mA
I_O	DC output source or sink current	for $-0.5V < V_O < V_{CC} + 0.5V$		[35]	mA
I_{CC}	DC V_{CC} or GND current			[70]	mA
T_{stg}	Storage temperature range		-65	150	°C
P_D	Power dissipation per package	above +70°C: derate linearly with 8mW/K		500	mW
T_L	Lead temperature	At distance 1/16±1/32 in. from case for 60 sec(CERAMIC) 10 sec(PLASTIC)		300 260	°C

Recommended Operating Conditions

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range V_{CC} : GD54/74HC Types	2	6	V
GD54/74HCT Types	4.5	5.5	
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A : GD74 Types	-40	+85	°C
GD54 Types	-55	+125	
Input Rise and Fall times t_r, t_f : GD54/74HC Types at 2V		1000	ns
at 4.5V		500	
at 6V		400	
GD54/74HCT Types at 4.5V		500	

Logic Diagram

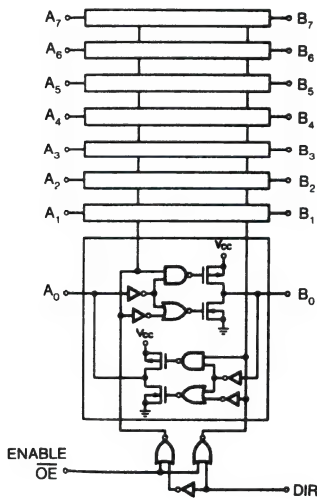


Fig. 1 Logic diagram

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HC643		GD54HC643		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2		1.5 3.15 4.2		V
V _{IL}	LOW level input voltage		2.0 4.5 6.0			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH} or V _{IL}	I _{OH} =-20μA I _{OH} =-6mA I _{OH} =-7.8mA	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0	1.9 4.4 5.9		1.9 4.4 5.9		V
				4.5 6.0	3.98 5.48	4.3 5.2	3.84 5.34		3.7 5.2		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH} or V _{IL}	I _{OL} =20μA I _{OL} =6mA I _{OL} =7.8mA	2.0 4.5 6.0			0.1 0.1 0.1		0.1 0.1 0.1		V
				4.5 6.0		0.17 0.15	0.26 0.26		0.33 0.33		
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	6.0			0.1		1.0		1.0	μA
I _{OZ}	Three-State leakage current	V _{IN} =V _{IH} or V _{IL} V _O =V _{CC} or GND	6.0		0.01	0.5		5.0		10.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	6.0			8		80		160	μA

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HCT643		GD54HCT643		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		4.5 to 5.0	2.0			2.0		2.0		V
V _{IL}	LOW level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH} or V _{IL}	I _{OH} =-20μA I _{OH} =-6mA	4.5 4.5	4.4 3.98	4.5 4.3	4.4 3.84		4.4 3.7		V
V _{OL}	LOW level output voltage	V _{IN} =V _{IH} or V _{IL}	I _{OL} =20μA I _{OL} =6mA	4.5 4.5		0.1 0.17	0.1 0.26		0.1 0.33		V
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	5.5			0.1		1.0		1.0	μA
I _{OZ}	Three-State leakage current	V _{IN} =V _{IH} or V _{IL} V _O =V _{CC} or GND	5.5		0.01	0.5		5.0		10.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	5.5			8		80		160	μA

AC Characteristics for HC: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HC643		GD54HC643		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
$t_{PLH}/$ t_{PHL}	Propagation Delay Time An to Bn; Inverting	2.0 4.5 6.0		300 10 9	100 20 18		120 25 22		140 30 26	ns
$t_{PLH}/$ t_{PHL}	Propagation Delay Time Bn to An; Non-Inverting	2.0 4.5 6.0		34 12 11	110 22 20		130 28 24		160 32 28	ns
$t_{PZH}/$ t_{PZL}	3-state Output Enable Time \overline{OE} , DIR to An; \overline{OE} , DIR to Bn	2.0 4.5 6.0		45 18 16	140 30 26		180 38 32		210 45 38	ns
$t_{PLZ}/$ t_{PHZ}	3-State Output Disable Time \overline{OE} , DIR to An; \overline{OE} , DIR to Bn	2.0 4.5 6.0		45 18 16	140 30 26		180 38 32		210 45 38	ns
$t_{TLH}/$ t_{THL}	Output Transition Time	2.0 4.5 6.0		15 6 5	60 12 10		75 15 13		90 18 15	ns

AC Characteristics for HCT: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HCT643		GD54HCT643		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
$t_{PLH}/$ t_{PHL}	Propagation Delay Time An to Bn; Inverting	4.5		13	26		28		32	ns
$t_{PLH}/$ t_{PHL}	Propagation Delay Time Bn to An; Non-Inverting	4.5		15	28		32		38	ns
$t_{PZH}/$ t_{PZL}	3-state Output Enable Time \overline{OE} , DIR to An; \overline{OE} , DIR to Bn	4.5		19	35		45		52	ns
$t_{PLZ}/$ t_{PHZ}	3-State Output Disable Time \overline{OE} , DIR to An; \overline{OE} , DIR to Bn	4.5		19	35		45		52	ns
$t_{TLH}/$ t_{THL}	Output Transition Time	4.5		7	12		15		18	ns

AC Waveforms

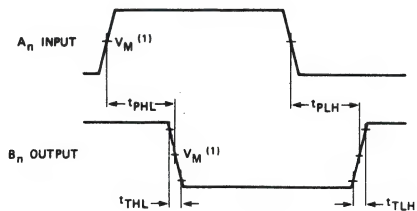


Fig. 2 Waveforms showing the input (An) to output (Bn) propagation delays and the output transition times.

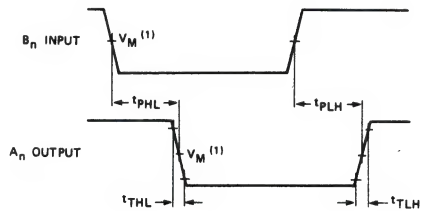


Fig. 3 Waveforms showing the input (Bn) to output (An) propagation delays and the output transition times.

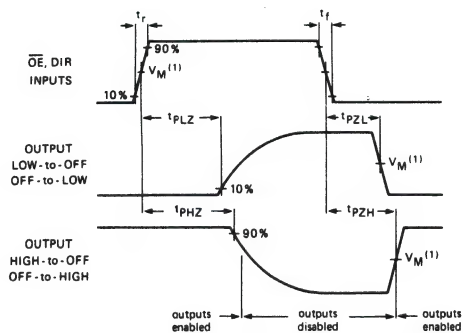


Fig. 4 Waveforms showing the 3-state enable and disable times for OE and DIR inputs.

Note to AC waveforms

(1) HC : $V_M = 50\%$; $V_I = \text{GND to } V_{CC}$.
HCT : $V_M = 1.3V$; $V_I = \text{GND to } 3V$.

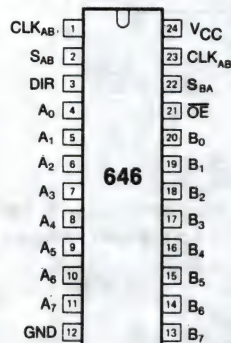
GD54/74HC646, GD54/74HCT646

OCTAL 3-STATE NONINVERTING TRANSCEIVERS AND D-TYPE FLIP-FLOPS

General Description

These devices are identical in pinout to the 54/74LS646. They are bus transceivers with D-type flip-flops designed for high speed multiplexed transmission of data. Depending upon the states of the data source selection inputs, data may be routed to the outputs either from the flip-flops or directly from the inputs. The output enable and the direction pins control the transceiver function. Only one of the two buses, A or B, may be enabled as outputs at any time. However, when either or both of the outputs are in the high impedance state, the pins may be used as inputs to the D-type flip-flops for storage of data. The HC/HCT 648 have similar function with inverting outputs. These devices are characterized for operation over wide temperature ranges to meet industry and military specifications.

Pin Configuration



Suffix-Blank : Plastic Dual In Line Package
 Suffix-J : Ceramic Dual In Line Package
 Suffix-D : Small Outline Package

Features

- Low Power consumption characteristic of CMOS devices
- Output drive capability: 15 LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts
for HCT 4.5 to 5.5 volts
- Low input current: 1 μ A Max.
- Low quiescent current: 80 μ A Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs

Function Table

INPUTS						DATA I/O*		FUNCTION
OE	DIR	CLK _{AB}	CLK _{BA}	S _{AB}	S _{BA}	A ₀ to A ₇	B ₀ to B ₇	
H	X	H or L	H or L	X	X	input	input	isolation
H	X	†	†	X	X			store A and B data
L	L	X	X	X	L	output	input	real-time B data to A bus
L	L	X	X	X	H			stored B data to A bus
L	H	X	X	L	X	input	output	real-time A data to B bus
L	H	H or L	X	H	X			stored A data to B bus

* The data output functions may be enabled or disabled by various signals at the OE and DIR inputs. Data input functions are always enabled, i.e., data at the bus inputs will be stored on every LOW-to-HIGH transition on the clock inputs.

H = HIGH voltage level

L = LOW voltage level

X = don't care

† = LOW-to-HIGH level transition

Logic Diagram

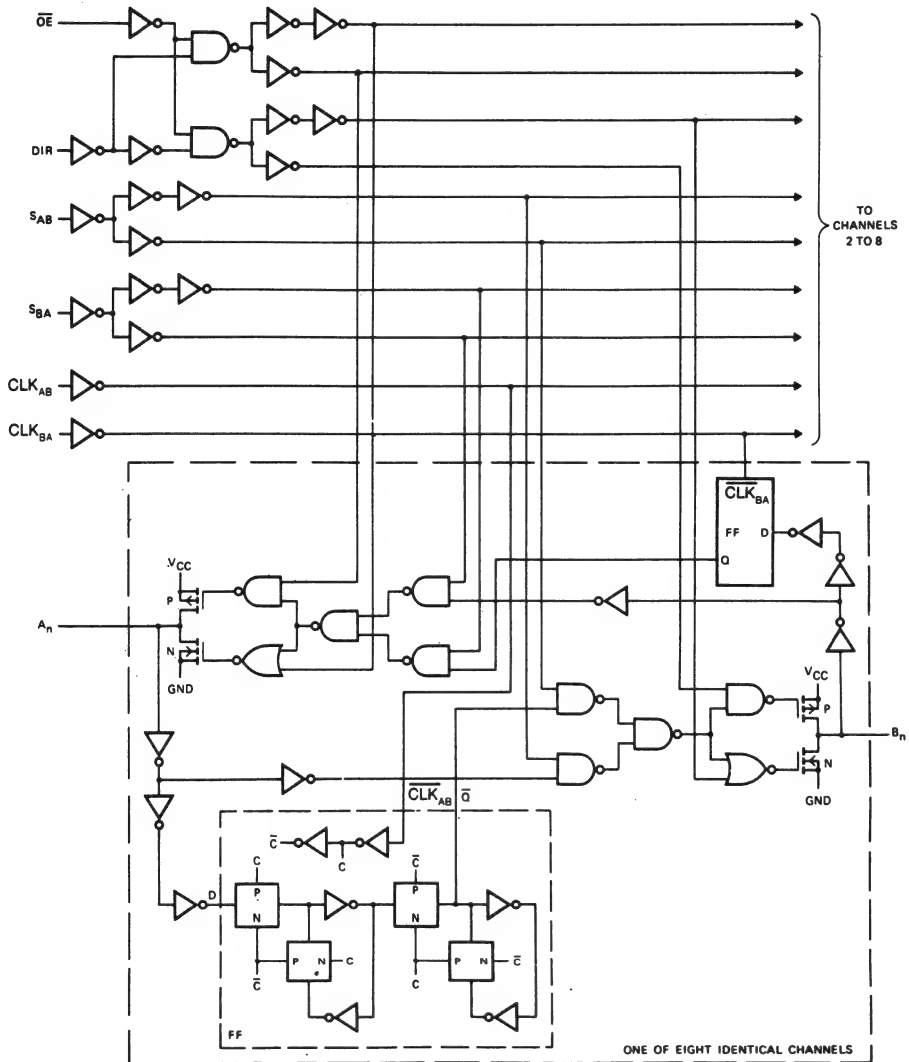


Fig. 1 Logic Diagram

Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC Supply voltage		-0.5	+7	V
I_{IK}, I_{OK}	DC input or output diode current	for $V_I < -0.5$ or $V_I > V_{CC} + 0.5V$		20	mA
I_O	DC output source or sink current	for $-0.5V < V_O < V_{CC} + 0.5V$		35	mA
I_{CC}	DC V_{CC} or GND current			70	mA
T_{stg}	Storage temperature range		-65	150	°C
P_D	Power dissipation per package	above +70°C: derate linearly with 8mW/K		500	mW
T_L	Lead temperature	At distance 1/16 ± 1/32 in. from case for 60 sec(CERAMIC) 10 sec(PLASTIC)		300 260	°C

Recommended Operating Conditions

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range V_{CC} : GD54/74HC Types GD54/74HCT Types	2 4.5	6 5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A : GD74 Types GD54 Types	-40 -55	+85 +125	°C
Input Rise and Fall times t_r, t_f : GD54/74HC Types at 2V at 4.5V at 6V GD54/74HCT Types at 4.5V		1000 500 400 500	ns

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HCT646		GD54HCT646		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2		1.5 3.15 4.2		V
V _{IL}	LOW level input voltage		2.0 4.5 6.0			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH} or V _{IL}	I _{OH} =-20μA	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0	1.9 4.4 5.9		1.9 4.4 5.9		V
			I _{OH} =-6mA	4.5 6.0	3.98 5.48	4.3 5.2	3.84 5.34		3.7 5.2		
			I _{OH} =-7.8mA								
V _{OL}	LOW level output voltage	V _{IN} =V _{IH} or V _{IL}	I _{OL} =20μA	2.0 4.5 6.0			0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1		V
			I _{OL} =6mA	4.5 6.0		0.17 0.15	0.26 0.26	0.33 0.33		0.4 0.4	
			I _{OL} =7.8mA								
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	6.0			0.1		1.0		1.0	μA
I _{OZ}	Three-State leakage current	V _{IN} =V _{IH} or V _{IL} V _O =V _{CC} or GND	6.0		0.01	0.5		5.0		10.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	6.0			8		80		160	μA

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HCT646		GD54HCT646		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		4.5 to 5.0	2.0			2.0		2.0		V
V _{IL}	LOW level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH} or V _{IL}	I _{OH} =-20μA	4.5	4.4	4.5	4.4		4.4		V
			I _{OH} =-6mA	4.5	3.98	4.3	3.84		3.7		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH} or V _{IL}	I _{OL} =20μA	4.5		0.1	0.1		0.1		V
			I _{OL} =6mA	4.5		0.17	0.26	0.33		0.4	
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	5.5			0.1		1.0		1.0	μA
I _{OZ}	Three-State leakage current	V _{IN} =V _{IH} or V _{IL} V _O =V _{CC} or GND	5.5		0.01	0.5		5.0		10.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	5.5			8		80		160	μA

Timing Requirements for HC: $t_r = t_f = 6\text{ns}$ $C_L = 50\text{pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A = 25^\circ\text{C}$			GD74HC646		GD54HC646		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_w	Pulse width	CLK_{AB}, CLK_{BA}	2.0 4.5 6.0	80 16 14	30 10 8		100 20 18		120 25 22	ns
t_{su}	Setup time	An, Bn to CLK_{AB}, CLK_{BA}	2.0 4.5 6.0	60 12 10	30 10 8		100 20 18		120 25 22	ns
t_h	Hold time	An, Bn to CLK_{AB}, CLK_{BA}	2.0 4.5 6.0	3 3 3	0 0 0		3 3 3		3 3 3	ns

AC Characteristics for HC: $t_r = t_f = 6\text{ns}$ $C_L = 50\text{ pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A = 25^\circ\text{C}$			GD74HC648		GD54HC648		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
f_{max}	Maximum clock pulse frequency	2.0 4.5 6.0	6 30 35	20 65 75		5 25 30		4 20 25		ns
t_{PLH}/t_{PHL}	Propagation Delay Time An, Bn to Bn, An	2.0 4.5 6.0		45 15 14	140 30 26		180 36 33		210 40 38	ns
t_{PLH}/t_{PHL}	Propagation Delay Time CLK_{AB}, CLK_{BA} to Bn, An	2.0 4.5 6.0		40 12 10	140 25 24		180 35 32		210 40 38	ns
t_{PLH}/t_{PHL}	Propagation Delay Time S_{AB}, S_{BA} to Bn, An	2.0 4.5 6.0		50 16 15	150 35 22		190 50 45		250 60 55	ns
t_{PZH}/t_{PZL}	3-state Output Enable Time \overline{OE} to An, Bn	2.0 4.5 6.0		60 18 16	170 35 30		200 40 38		240 50 45	ns
t_{PLZ}/t_{PHZ}	3-state Output Disable Time \overline{OE} to An, Bn	2.0 4.5 6.0		60 18 16	170 35 30		200 40 38		240 50 45	ns
t_{PZH}/t_{PZL}	3-state Output Enable Time DIR to An, Bn	2.0 4.5 6.0		60 18 16	170 35 30		200 40 38		240 50 45	ns
t_{PLZ}/t_{PHZ}	3-state Output Disable Time DIR to An, Bn	2.0 4.5 6.0		60 18 16	170 35 30		200 40 38		240 50 45	ns
t_{TLH}/t_{THL}	Output Transition Time	2.0 4.5 6.0		15 6 5	60 12 10		75 15 13		90 18 15	ns

Timing Requirements for HCT: $t_r=t_f=6\text{ns}$ $C_L=50\text{pF}$

SYMBOL	PARAMETER		V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HCT646		GD54HCT646		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_w	Pulse width	$\text{CLK}_{AB}, \text{CLK}_{BA}$	4.5	16	10		20		25		ns
t_{su}	Setup time	An, Bn to $\text{CLK}_{AB}, \text{CLK}_{BA}$	4.5	12	10		20		25		ns
t_h	Hold time	An, Bn to $\text{CLK}_{AB}, \text{CLK}_{BA}$	4.5	3	0		3		3		ns

AC Characteristics for HCT: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER		V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HCT646		GD54HCT646		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
f_{max}	Maximum Clock Pulse Frequency		4.5	27	54		22		18		ns
t_{PLH}/t_{PHL}	Propagation Delay Time An Bn to Bn, An		4.5		16	30		36		40	ns
t_{PLH}/t_{PHL}	Propagation Delay Time $\text{CLK}_{AB}, \text{CLK}_{BA}$ to Bn, An		4.5		14	28		35		40	ns
t_{PLH}/t_{PHL}	Propagation Delay Time S_{AB}, S_{BA} to Bn An,		4.5		18	36		50		60	ns
t_{PZH}/t_{PZL}	3-state Output Enable Time \overline{OE} to An, Bn		4.5		19	38		42		52	ns
t_{PLZ}/t_{PHZ}	3-state Output Disable Time \overline{OE} to An, Bn		4.5		19	38		42		52	ns
t_{PZH}/t_{PZL}	3-state Output Enable Time DIR to An, Bn		4.5		19	38		42		52	ns
t_{PLZ}/t_{PHZ}	3-state Output Disable Time DIR to An, Bn		4.5		19	38		42		52	ns
t_{TLH}/t_{THL}	Output Transition Time		4.5		6	12		15		18	ns

AC Waveforms

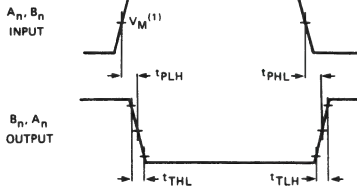


Fig. 2 Waveforms showing the input A_n, B_n to output B_n, A_n propagation delays and the output transition times.

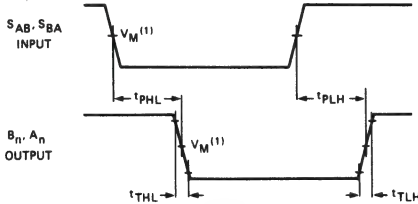


Fig. 4 Waveforms showing the input S_{AB}, S_{BA} to output B_n, A_n propagation delays and output transition times.

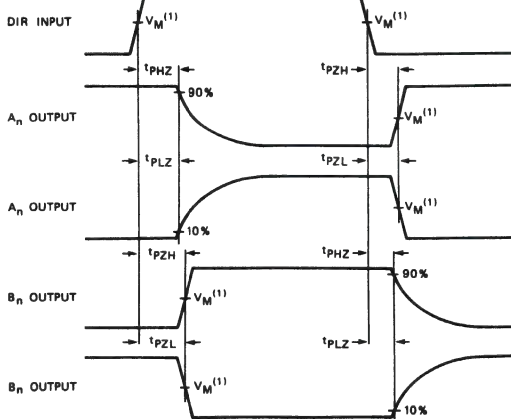


Fig. 6 Waveforms showing the input DIR to output A_n, B_n 3-state enable and disable times.

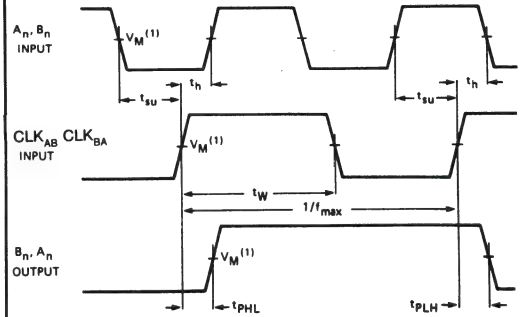


Fig. 3 Waveforms showing the A_n, B_n to CLK_{AB}, CLK_{BA} set-up and hold times, clock CLK_{AB}, CLK_{BA} pulse width, maximum clock pulse frequency and the CLK_{AB}, CLK_{BA} to output B_n, A_n propagation delays.

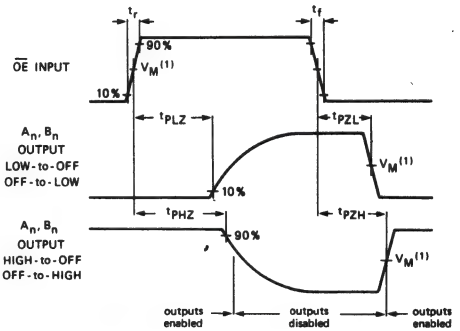


Fig. 5 Waveforms showing the input \overline{OE} to output A_n, B_n 3-state enable and disable times.

Note to AC waveforms

- (1) HC : $V_M=50\%$; $V_I=GND$ to V_{CC} .
HCT : $V_M=1.3V$; $V_I=GND$ to $3V$.

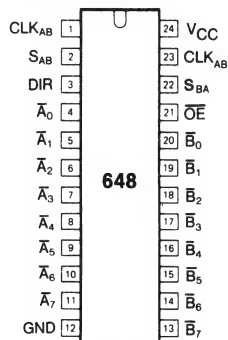
GD54/74HC648, GD54/74HCT648

OCTAL 3-STATE INVERTING TRANSCEIVERS AND D-TYPE FLIP-FLOPS

General Description

These devices are identical in pinout to the 54/74LS648. they are bus transceivers with D-type flip-flops designed for high speed multiplexed transmission of data. Depending upon the states of the data source selection inputs, data may be routed to the outputs either from the flip-flops or directly from the inputs. The output enable and the direction pins control the transceiver function. Only one of the two buses, A or B, may be enabled as outputs at any time. However, when either or both of the outputs are in the high impedance state, the pins may be used as inputs to the D-type flip-flops for storage of data. The HC/HCT 646 have similar function with noninverting outputs. These devices are characterized for operation over wide temperature ranges to meet industry and military specifications.

Pin Configuration



Suffix-Blank : Plastic Dual In Line Package
 Suffix-J : Ceramic Dual In Line Package
 Suffix-D : Small Outline Package

Features

- Low Power consumption characteristic of CMOS devices
- Output drive capability: 15 LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts
for HCT 4.5 to 5.5 volts
- Low input current: 1μA Max.
- Low quiescent current: 80μA Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs

Function Table

INPUTS						DATA I/O*		FUNCTION
OE	DIR	CLK _{AB}	CLK _{BA}	S _{AB}	S _{BA}	A ₀ to A ₇	B ₀ to B ₇	
H	X	H or L	H or L	X	X	input	input	isolation store A and B data
H	X	†	†	X	X			
L	L	X	X	X	L	output	input	real-time B data to A bus stored B data to A bus
L	L	X	X	X	H			
L	H	X	X	L	X	input	output	real-time A data B bus stored A data to B bus
L	H	H or L	X	H	X			

* The data output functions may be enabled or disabled by various signals at the OE and DIR inputs. Data input functions are always enabled. i.e., data at the bus inputs will be stored on every LOW-to-HIGH transition on the clock inputs.

H = HIGH voltage level

L = LOW voltage level

X = don't care

† = LOW-to-HIGH level transition

Logic Diagram

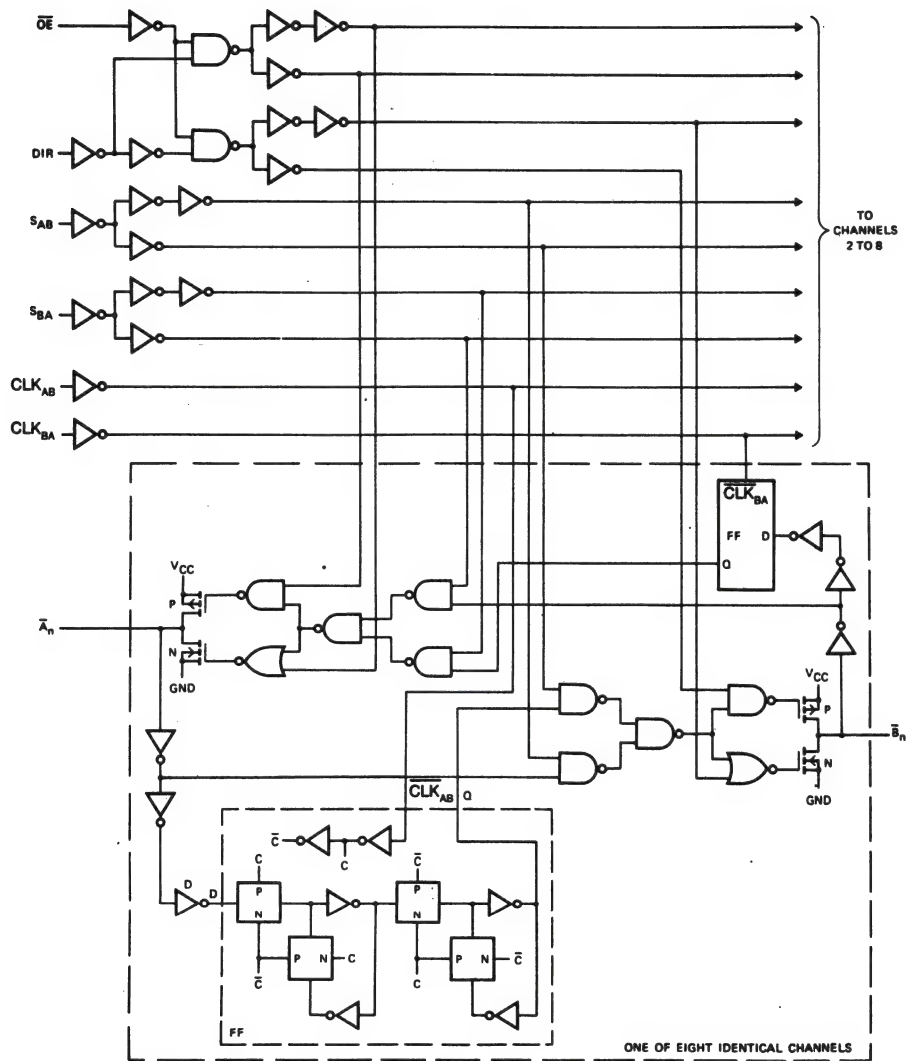


Fig. 1. Logic Diagram

Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC Supply voltage		-0.5	+7	V
I_{IK}, I_{OK}	DC input or output diode current	for $V_I < -0.5$ or $V_I > V_{CC} + 0.5V$		20	mA
I_O	DC output source or sink current	for $-0.5V < V_O < V_{CC} + 0.5V$		35	mA
I_{CC}	DC V_{CC} or GND current			70	mA
T_{stg}	Storage temperature range		-65	150	°C
P_D	Power dissipation per package	above +70°C: derate linearly with 8mW/K		500	mW
T_L	Lead temperature	At distance $1/16 \pm 1/32$ in. from case for 60 sec(CERAMIC) 10 sec(PLASTIC)		300 260	°C

Recommended Operating Conditions

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range V_{CC} : GD54/74HC Types GD54/74HCT Types	2 4.5	6 5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A : GD74 Types GD54 Types	-40 -55	+85 +125	°C
Input Rise and Fall times t_r, t_f : GD54/74HC Types at 2V at 4.5V at 6V GD54/74HCT Types at 4.5V		1000 500 400 500	ns

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HCT648		GD54HCT648		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2		1.5 3.15 4.2		V
V _{IL}	LOW level input voltage		2.0 4.5 6.0			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH} or V _{IL}	I _{OH} =-20μA	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0	1.9 4.4 5.9		1.9 4.4 5.9		V
				I _{OH} =-6mA I _{OH} =-7.8mA	4.5 6.0	3.98 5.48	4.3 5.2		3.84 5.34		
			I _{OL} =20μA	2.0 4.5 6.0			0.1 0.1 0.1	0.1 0.1 0.1		0.1 0.1 0.1	
				I _{OL} =6mA I _{OL} =7.8mA	4.5 6.0	0.17 0.15	0.26 0.26	0.33 0.33		0.4 0.4	
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	6.0			0.1		1.0		1.0	μA
I _{OZ}	Three-State leakage current	V _{IN} =V _{IH} or V _{IL} V _O =V _{CC} or GND	6.0		0.01	0.5		5.0		10.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	6.0			8		80		160	μA

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HCT648		GD54HCT648		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		4.5 to 5.0	2.0			2.0		2.0		V
V _{IL}	LOW level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH} or V _{IL}	I _{OH} =-20μA	4.5	4.4	4.5	4.4		4.4		V
			I _{OH} =-6mA	4.5	3.98	4.3	3.84		3.7		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH} or V _{IL}	I _{OL} =20μA	4.5			0.1	0.1		0.1	V
			I _{OL} =6mA	4.5		0.17	0.26	0.33		0.4	
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	5.5			0.1		1.0		1.0	μA
I _{OZ}	Three-State leakage current	V _{IN} =V _{IH} or V _{IL} V _O =V _{CC} or GND	5.5		0.01	0.5		5.0		10.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	5.5			8		80		160	μA

Timing Requirements for HC: $t_r=t_f=6\text{ns}$ $C_L=50\text{pF}$

SYMBOL	PARAMETER		V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HC648		GD54HC648		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_w	Pulse with	$\text{CLK}_{AB}, \text{CLK}_{BA}$	2.0	80	30		100		120		ns
			4.5	16	10		20		25		
			6.0	14	8		18		22		
t_{su}	Setup time	\bar{A}_n, \bar{B}_n to $\text{CLK}_{AB}, \text{CLK}_{BA}$	2.0	60	30		100		120		ns
			4.5	12	10		20		25		
			6.0	10	8		18		22		
t_h	Hold time	\bar{A}_n, \bar{B}_n to $\text{CLK}_{AB}, \text{CLK}_{BA}$	2.0	3	0		3		3		ns
			4.5	3	0		3		3		
			6.0	3	0		3		3		

AC Characteristics for HC, $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER		V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HC648		GD54HC648		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
f_{max}	Maximum Clock Pulse Frequency		2.0	6	20		5		4		MHz
			4.5	30	65		25		20		
			6.0	35	75		30		25		
$t_{PLH}/$ t_{PHL}	Propagation Dealy Time \bar{A}_n, \bar{B}_n to \bar{B}_n, \bar{A}_n		2.0		45	140		180		210	ns
			4.5		15	30		36		40	
			6.0		14	26		33		38	
t_{PLH} t_{PHL}	Propagation Delay Time $\text{CLK}_{AB}, \text{CLK}_{BA}$ to \bar{B}_n, \bar{A}_n		2.0		40	140		180		210	ns
			4.5		12	25		35		40	
			6.0		10	24		32		38	
$t_{PLH}/$ t_{PHL}	Propagation Delay Time S_{AB}, S_{BA} to \bar{B}_n, \bar{A}_n		2.0		50	150		190		250	ns
			4.5		16	35		50		60	
			6.0		15	22		45		55	
$t_{PZH}/$ t_{PZL}	3-state Output Enable Time \bar{OE} to \bar{A}_n, \bar{B}_n		2.0		60	170		200		240	ns
			4.5		18	35		40		50	
			6.0		16	30		38		45	
$t_{PLZ}/$ t_{PHZ}	3-state Output Disable Time \bar{OE} to \bar{A}_n, \bar{B}_n		2.0		60	170		200		240	ns
			4.5		18	35		40		50	
			6.0		16	30		38		45	
$t_{PZH}/$ t_{PZL}	3-state Output Enable Time DIR to \bar{A}_n, \bar{B}_n ,		2.0		60	170		200		240	ns
			4.5		18	35		40		50	
			6.0		16	30		38		45	
$t_{PLZ}/$ t_{PHZ}	3-state Output Disable Time DIR to \bar{A}_n, \bar{B}_n		2.0		60	170		200		240	ns
			4.5		18	35		40		50	
			6.0		16	30		38		45	
$t_{TLH}/$ t_{THL}	Output Transition Time		2.0		15	60		75		90	ns
			4.5		6	12		15		18	
			6.0		5	10		13		15	

Timing Requirements for HCT: $t_r=t_f=6\text{ns}$ $C_L=50\text{pF}$

SYMBOL	PARAMETER		V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HCT648		GD54HCT648		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_w	Pulse width	$\text{CLK}_{AB}, \text{CLK}_{BA}$	4.5	16	10		20		25		ns
t_{su}	Setup time	\bar{A}_n, \bar{B}_n to $\text{CLK}_{AB}, \text{CLK}_{BA}$	4.5	12	10		20		25		ns
t_h	Hold time	\bar{A}_n, \bar{B}_n to $\text{CLK}_{AB}, \text{CLK}_{BA}$	4.5	3	0		3		3		ns

AC Characteristics for HCT, $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HCT648		GD54HCT648		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
f_{max}	Maximum clock pulse frequency	4.5	27	54		22		18		MHz
t_{PLH}/t_{PHL}	Propagation Delay Time \bar{A}_n, \bar{B}_n to \bar{B}_n, \bar{A}_n	4.5		16	30		36		40	ns
t_{PLH}/t_{PHL}	Propagation Delay Time $\text{CLK}_{AB}, \text{CLK}_{BA}$ to \bar{B}_n, \bar{A}_n	4.5		14	28		35		40	ns
t_{PLH}/t_{PHL}	Propagation Delay Time S_{AB}, S_{BA} to \bar{B}_n, \bar{A}_n	4.5		18	36		50		60	ns
t_{PZH}/t_{PZL}	3-state Output Enable Time \overline{OE} to \bar{A}_n, \bar{B}_n	4.5		19	38		42		52	ns
t_{PLZ}/t_{PHZ}	3-state Output Disable Time \overline{OE} to \bar{A}_n, \bar{B}_n	4.5		19	38		42		52	ns
t_{PZH}/t_{PZL}	3-state Output Enable Time DIR to \bar{A}_n, \bar{B}_n	4.5		19	38		42		52	ns
t_{PLZ}/t_{PHZ}	3-state Output Disable Time DIR to \bar{A}_n, \bar{B}_n	4.5		19	38		42		52	ns
t_{TLH}/t_{THL}	Output Transition Time	4.5		6	12		15		18	ns

AC Waveforms

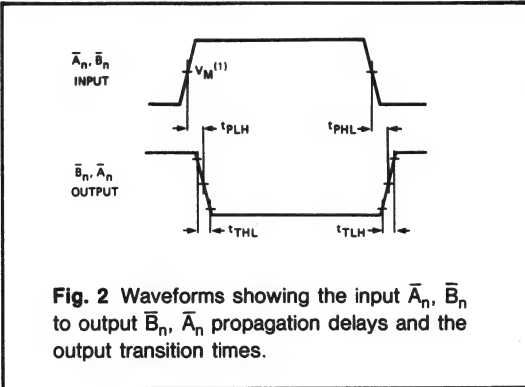


Fig. 2 Waveforms showing the input \bar{A}_n, \bar{B}_n to output \bar{B}_n, \bar{A}_n propagation delays and the output transition times.

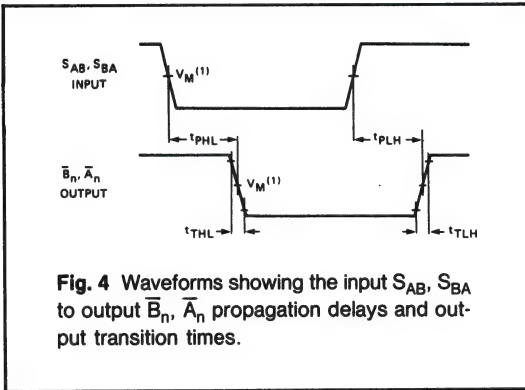


Fig. 4 Waveforms showing the input S_{AB}, S_{BA} to output \bar{B}_n, \bar{A}_n propagation delays and output transition times.

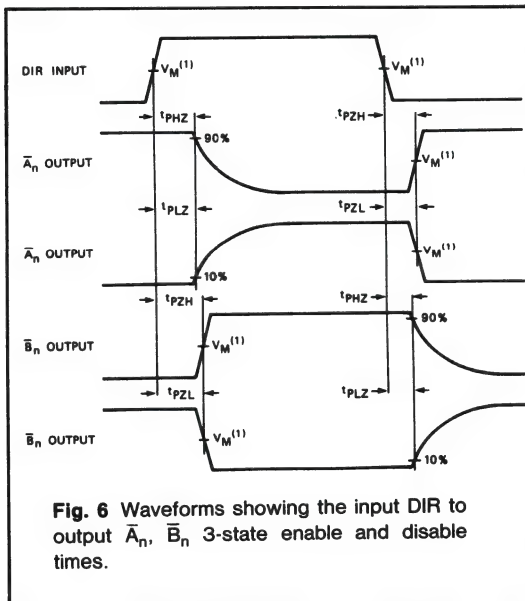


Fig. 6 Waveforms showing the input DIR to output \bar{A}_n, \bar{B}_n 3-state enable and disable times.

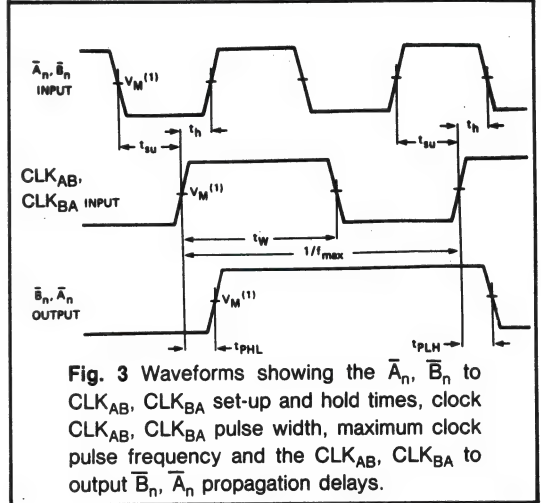


Fig. 3 Waveforms showing the \bar{A}_n, \bar{B}_n to CLK_{AB}, CLK_{BA} set-up and hold times, clock CLK_{AB}, CLK_{BA} pulse width, maximum clock pulse frequency and the CLK_{AB}, CLK_{BA} to output \bar{B}_n, \bar{A}_n propagation delays.

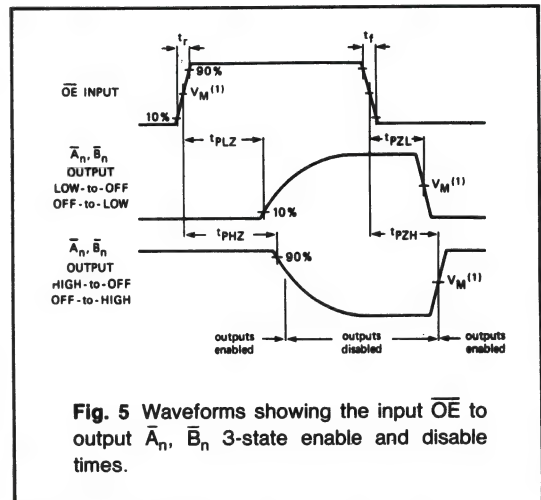


Fig. 5 Waveforms showing the input \overline{OE} to output \bar{A}_n, \bar{B}_n 3-state enable and disable times.

Note to AC waveforms

- (1) HC : $V_M = 50\%$; $V_i = GND$ to V_{CC} .
- HCT : $V_M = 1.3V$; $V_i = GND$ to $3V$.

GD54/74HC670, GD54/74HCT670

4-BY-4 REGISTER FILE WITH 3-STATE OUTPUTS

General Description

These devices are identical in pinout to the 54/74LS670. This register file is organized as 4 words of 4 bits each and separate on-chip decoding is provided for addressing the four word locations to either write-in or retrieve data. This permits simultaneous writing into one location and reading from another word location. The individual address lines permit direct acquisition of data stored in any four of the latches. This circuit can be used as:

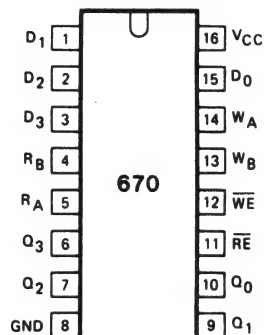
Scratch-pad Memory

Buffer storage between processors

Bit storage in fast multiplication designs

These devices are characterized for operation over wide temperature ranges to meet industry and military specifications.

Pin Configuration



Suffix-Blank : Plastic Dual In Line Package
 Suffix-J : Ceramic Dual In Line Package
 Suffix-D : Small Outline Package

Features

- Low Power consumption characteristic of CMOS devices
- Output drive capability: 15 LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts
for HCT 4.5 to 5.5 volts
- Low input current: 1μA Max.
- Low quiescent current: 80μA Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs

Function Table

WRITE MODE SELECT TABLE

OPERATING MODE	INPUTS		INTERNAL LATCHES★
	WE	D _n	
write data	L	L	L
	L	H	H
data latched	H	X	no change

★ The write address (W_A and W_B) to the "internal latches" must be stable while WE is LOW for conventional operation.

READ MODE SELECT TABLE

OPERATING MODE	INPUTS		OUTPUT
	RE	INTERNAL LATCHES★★	
read	L	L	L
	L	H	H
disabled	H	X	Z

★★ The selection of the "internal latches" by read address (R_A and R_B) are not constrained by WE or RE operation.

Logic Diagram

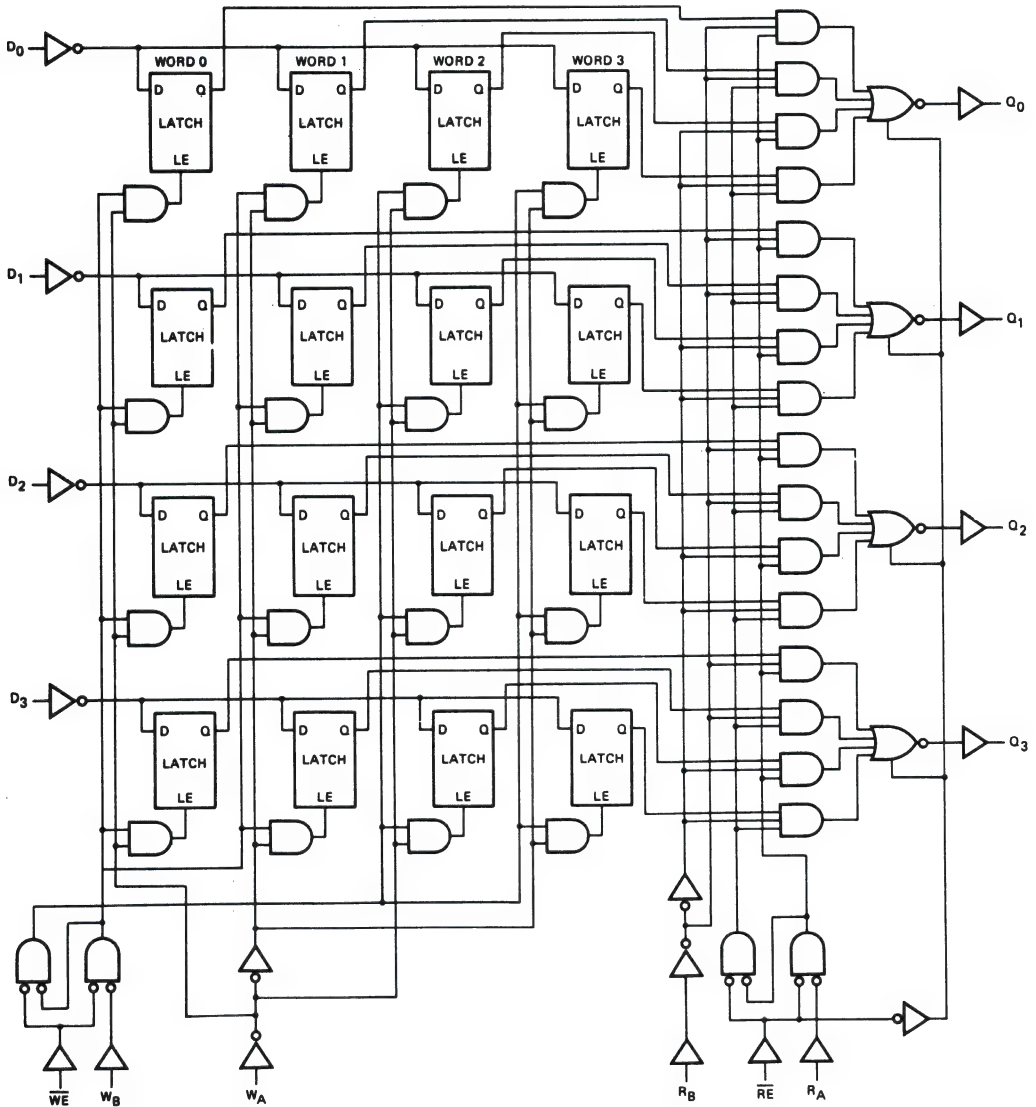


Fig. 1 Logic diagram

Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC Supply voltage		-0.5	+7	V
I_{IK}, I_{OK}	DC input or output diode current	for $V_I < -0.5$ or $V_I > V_{CC} + 0.5V$		20	mA
I_O	DC output source or sink current	for $-0.5V < V_O < V_{CC} + 0.5V$		25	mA
I_{CC}	DC V_{CC} or GND current			50	mA
T_{stg}	Storage temperature range		-65	150	°C
P_D	Power dissipation per package	above +70°C: derate linearly with 8mW/K		500	mW
T_L	Lead temperature	At distance $1/16 \pm 1/32$ in. from case for 60 sec(CERAMIC) 10 sec(PLASTIC)		300 260	°C

Recommended Operating Conditions

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range V_{CC} : GD54/74HC Types GD54/74HCT Types	2 4.5	6 5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A : GD74 Types GD54 Types	-40 -55	+85 +125	°C
Input Rise and Fall times t_r, t_f : GD54/74HC Types at 2V at 4.5V at 6V GD54/74HCT Types at 4.5 V		1000 500 400 500	ns

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HC670		GD54HC670		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2		1.5 3.15 4.2		V
V _{IL}	LOW level input voltage		2.0 4.5 6.0			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH}	I _{OH} =-20μA	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0	1.9 4.4 5.9		1.9 4.4 5.9		V
		or V _{IL}	I _{OH} =-4mA I _{OH} =-5.2mA	4.5 6.0	3.98 5.48	4.3 5.2	3.84 5.34		3.7 5.2		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH}	I _{OL} =20μA	2.0 4.5 6.0			0.1 0.1 0.1		0.1 0.1 0.1		V
		or V _{IL}	I _{OL} =4mA I _{OL} =5.2mA	4.5 6.0		0.17 0.15	0.26 0.26		0.33 0.33		
									0.4 0.4		
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	6.0			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	6.0			8		80		160	μA

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HCT670		GD54HCT670		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		4.5 to 5.5	2.0			2.0		2.0		V
V _{IL}	LOW level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH}	I _{OH} =-20μA	4.5	4.4	4.5	4.4		4.4		V
		or V _{IL}	I _{OH} =-4mA	4.5	3.98	4.3	3.84		3.7		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH}	I _{OL} =20μA	4.5			0.1		0.1		V
		or V _{IL}	I _{OL} =4mA	4.5		0.17	0.26		0.33		
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	5.5			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	5.5			8		80		160	μA

Timing Requirements for HC: $t_r = t_f = 6\text{ns}$ $C_L = 50\text{ pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A = 25^\circ\text{C}$			GD74HC670		GD54HC670		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_w	Pulse width	RE low	2.0	70		115		135		ns
			4.5	18		23		27		
			6.0	15		20		23		
		\overline{WE} low	2.0	90		115		135		ns
			4.5	18		23		27		
			6.0	15		20		23		
t_{su}	Setup time	Dn before $\overline{WE} \uparrow$	2.0	60		75		90		ns
			4.5	12		15		18		
			6.0	10		13		15		
		W_A, W_B before $\overline{WE} \downarrow$	2.0	60		75		90		ns
			4.5	12		15		18		
			6.0	10		13		15		
t_h	Hold time	Dn after $\overline{WE} \uparrow$	2.0	5		5		5		ns
			4.5	5		5		5		
			6.0	5		5		5		
		W_A, W_B after $\overline{WE} \uparrow$	2.0	5		5		5		ns
			4.5	5		5		5		
			6.0	5		5		5		
t_{latch}	Latch time	\overline{WE} to $R_A, R_B \uparrow$	2.0	225		230		340		ns
			4.5	45		56		68		
			6.0	38		48		58		

AC Characteristics for HC: $t_r = t_f = 6\text{ns}$ $C_L = 50\text{ pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A = 25^\circ\text{C}$			GD74HC670		GD54HC670		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
$t_{PLH}/$ t_{PHL}	Propagation Delay Time R_A, R_B to Qn	2.0			225		280		340	ns
		4.5			45		56		68	
		6.0			38		48		58	
$t_{PLH}/$ t_{PHL}	Propagation Delay Time \overline{WE} to Qn	2.0			250		315		375	ns
		4.5			50		63		75	
		6.0			43		54		64	
$t_{PLH}/$ t_{PHL}	Propagation Delay Time Dn to Qn	2.0			250		315		375	ns
		4.5			50		63		75	
		6.0			43		54		64	
$t_{PZH}/$ t_{PZL}	3-state Output Enable Time \overline{RE} to Qn	2.0			175		220		265	ns
		4.5			35		44		53	
		6.0			30		37		45	
$t_{PLZ}/$ t_{PHZ}	3-state Output Disable Time \overline{RE} to Qn	2.0			175		220		265	ns
		4.5			35		44		53	
		6.0			30		37		45	
$t_{TLH}/$ t_{THL}	Output Transition Time	2.0		19	75		95		110	ns
		4.5		7	15		19		22	
		6.0		6	13		16		19	

Timing Requirements for HCT: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER		V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HCT670		GD54HCT670		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_w	Pulse width	\overline{RE} low	4.5	25			31		38		ns
		\overline{WE} low	4.5	25			31		38		ns
t_{su}	Setup time	Dn before $\overline{WE} \uparrow$	4.5	12			15		18		ns
		W_A, W_B before $\overline{WE} \downarrow$	4.5	18			23		27		ns
t_h	Hold time	Dn after $\overline{WE} \uparrow$	4.5	5			5		5		ns
		W_A, W_B after $\overline{WE} \uparrow$	4.5	5			5		5		ns
t_{latch}	Latch time	\overline{WE} to $R_A, R_B \uparrow$	4.5	50			63		75		Mhz

AC Characteristics for HCT: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HCT670		GD54HCT670		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
$t_{PLH}/$ t_{PHL}	Propagation Delay Time R_A, R_B to Qn	4.5			50		63		75	ns
$t_{PLH}/$ t_{PHL}	Propagation Delay Time \overline{WE} to Qn	4.5			53		66		80	ns
$t_{PLH}/$ t_{PHL}	Propagation Delay Time Dn to Qn	4.5			50		63		75	ns
$t_{PZH}/$ t_{PZL}	3-state Output Enable Time \overline{RE} to Qn	4.5			40		50		60	ns
$t_{PLZ}/$ t_{PHZ}	3-state Output Disable Time \overline{RE} to Qn	4.5			35		44		53	ns
$t_{TLH}/$ t_{THL}	Output Transition Time	4.5		7	15		19		22	ns

AC Waveforms

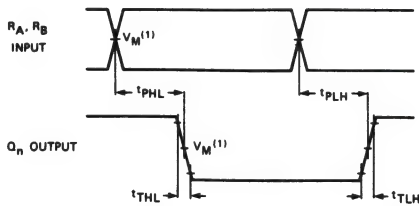


Fig. 2 Waveforms showing the read address input (R_A, R_B) to output (Q_n) propagation delays and output transition times.

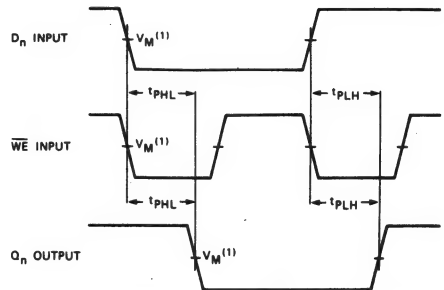
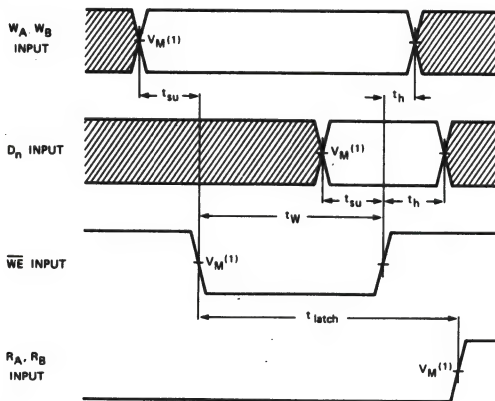


Fig. 3 Waveforms showing the write enable input (\overline{WE}) and data input (D_n) to output (Q_n) propagation delays, and the write enable pulse width.



Note to Fig. 4

The shaded areas indicate when the input is permitted to change for predictable output performance.

The time allowed for the internal output of the latch to assume the state of the new data (t_{latch}) is important only when attempting to read from a location immediately after that location has received new data. This parameter is measured from the falling edge of \overline{WE} to the rising edge of R_A or R_B . \overline{RE} must be LOW.

Fig. 4 Waveforms showing the write address input (W_A, W_B) and data input (D_n) to write enable (\overline{WE}) set-up, hold and latch times.

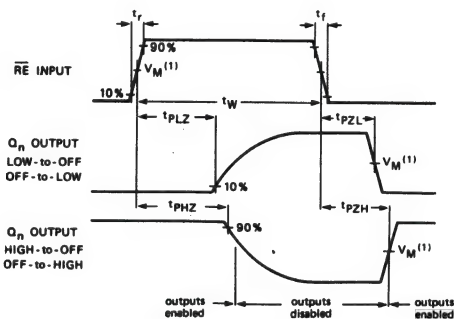


Fig. 5 Waveforms showing the read enable (\overline{RE}) to output (Q_n) enable and disable times, and read enable pulse width.

Note to AC waveforms

- (1) HC : $V_M = 50\%$; $V_i = \text{GND}$ to V_{CC} .
- HCT : $V_M = 1.3V$; $V_i = \text{GND}$ to $3V$.

GD54/74HC688, GD54/74HCT688

MAGNITUDE COMPARATOR/EQUALITY DETECTOR

General Description

These devices are identical in pinout to the 54/74LS688. This circuit compares two 8-bit binary of BCD words and indicates whether or not they are equal. The comparator output indicates equality when it is low. A single active low enable is provided to facilitate cascading of several packages and enable comparison of words greater than 8 bits. This device is useful in memory block decoding applications, where memory block enable signals must be generated from computer address information. These devices are characterized for operation over wide temperature ranges to meet industry and military specifications.

Features

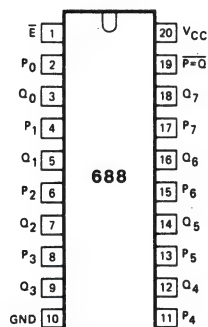
- Low Power consumption characteristic of CMOS devices
- Output drive capability: 10 LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts
for HCT 4.5 to 5.5 volts
- Low input current: 1 μ A Max.
- Low quiescent current: 80 μ A Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs

Function Table

INPUTS		OUTPUT
DATA P_n, Q_n	ENABLE \overline{E}	$\overline{P=Q}$
$P=Q$	L	L
X	H	H
$P>Q$	L	H
$P<Q$	L	H

H = HIGH voltage level
L = LOW voltage level
X = don't care

Pin Configuration



Suffix-Blank : Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package
Suffix-D : Small Outline Package

Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC Supply voltage		-0.5	+7	V
I_{IK}, I_{OK}	DC input or output diode current	for $V_I < -0.5$ or $V_I > V_{CC} + 0.5V$		20	mA
I_O	DC output source or sink current	for $-0.5V < V_O < V_{CC} + 0.5V$		25	mA
I_{CC}	DC V_{CC} or GND current			50	mA
T_{stg}	Storage temperature range		-65	150	°C
P_D	Power dissipation per package	above +70°C: derate linearly with 8mW/K		500	mW
T_L	Lead temperature	At distance 1/16 ± 1/32 in. from case for 60 sec(CERAMIC) 10 sec(PLASTIC)		300 260	°C

Recommended Operating Conditions

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range V_{CC} : GD54/74HC Types GD54/74HCT Types	2 4.5	6 5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A : GD74 Types GD54 Types	-40 -55	+85 +125	°C
Input Rise and Fall times t_r, t_f : GD54/74HC Types at 2V at 4.5V at 6V GD54/74HCT Types at 4.5V		1000 500 400 500	ns

Logic Diagram

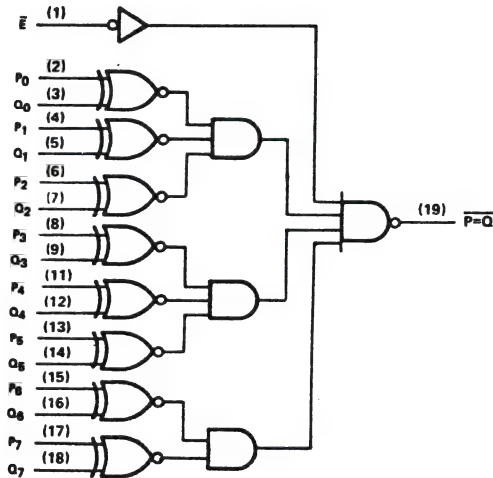


Fig. 1 Logic diagram

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HC688		GD54HC688		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2		1.5 3.15 4.2		V
V _{IL}	LOW level input voltage		2.0 4.5 6.0			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH}	I _{OH} =-20μA	2.0	1.9	2.0			1.9		V
				4.5	4.4	4.5			4.4		
		or V _{IL}	I _{OH} =-4mA I _{OH} =-5.2mA	6.0	5.9	6.0			5.9		
				4.5	3.98	4.3			3.84		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH}	I _{OL} =20μA	2.0			0.1	0.1		0.1	V
				4.5			0.1	0.1		0.1	
		or V _{IL}	I _{OL} =4mA I _{OL} =5.2mA	6.0			0.1	0.1		0.1	
				4.5		0.17	0.26	0.33		0.4	
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	6.0			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	6.0			8		80		160	μA

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HCT688		GD54HCT688		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		4.5 to 5.5	2.0			2.0		2.0		V
V _{IL}	LOW level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH}	I _{OH} =-20μA	4.5	4.4	4.5			4.4		V
				4.5	3.98	4.3			3.84		
		or V _{IL}	I _{OH} =-4mA	4.5	3.98	4.3			3.84		
				4.5					3.7		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH}	I _{OL} =20μA	4.5			0.1	0.1		0.1	V
				4.5							
		or V _{IL}	I _{OL} =4mA	4.5		0.17	0.26	0.33		0.4	
				4.5							
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	5.5			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	5.5			8		80		160	μA

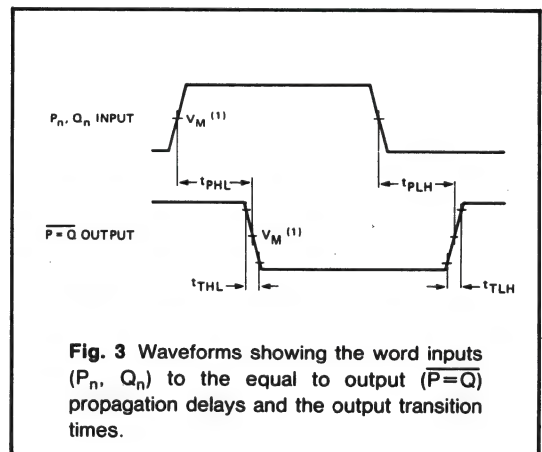
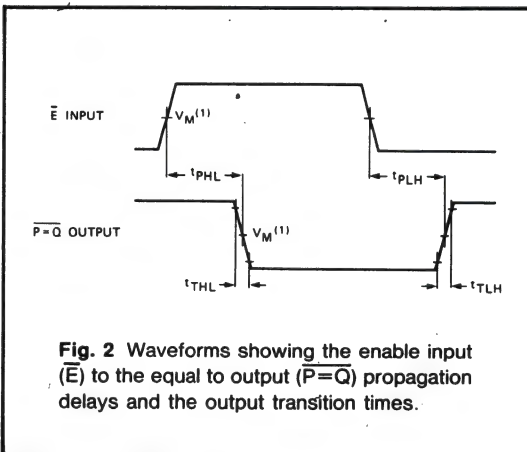
AC Characteristics for HC: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER	V_{CC}	$T_A=25^\circ\text{C}$			GD74HC688		GD54HC688		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} / t_{PHL}	Propagation Delay Time P_n, Q_n to $\overline{P=Q}$	2.0 4.5 6.0		45 16 15	160 34 29		210 40 36		250 50 44	ns
t_{PLH} / t_{PHL}	Propagation Delay Time \overline{E} to $\overline{P=Q}$	2.0 4.5 6.0		30 10 8	120 24 20		140 30 26		180 56 32	ns
t_{TLH} / t_{THL}	Output Transition Time	2.0 4.5 6.0		25 8 7	70 15 13		85 18 16		120 22 19	ns

AC Characteristics for HCT: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER	V_{CC}	$T_A=25^\circ\text{C}$			GD74HCT688		GD54HCT688		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} / t_{PHL}	Propagation Delay Time P_n, Q_n to $\overline{P=Q}$	4.5		18	36		42		50	ns
t_{PLH} / t_{PHL}	Propagation Delay Time \overline{E} to $\overline{P=Q}$	4.5		12	24		32		38	ns
t_{TLH} / t_{THL}	Output Transition Time	4.5		8	15		18		22	ns

AC Waveforms



Note to AC waveforms

(1) HC : $V_M=50\%$; $V_I=GND$ to V_{CC} .

HCT : $V_M=1.3V$; $V_I=GND$ to $3V$.



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QUALITY ASSURANCE MANUAL

1. INTRODUCTION

2. QUALITY ASSURANCE SYSTEM

- 2.1 Quality Assurance at the Development State
- 2.2 Quality Assurance at the Mass Production State
 - 2.2.1 Control of Material Purchasing
 - 2.2.2 Control of The Manufacturing Process
 - 2.2.3 Environment Control
 - 2.2.4 Control of Production and Instrument

3. RELIABILITY TEST

- 3.1 Principle of Reliability
- 3.2 Reliability Test Items and Conditions

4. SUMMARY

5. HANDLING AND STORAGE INSTRUCTION

1. INTRODUCTION

In recent years, advances in integrated circuit have been rapid with increasing density and speed accompanied by decreasing cost. To meet these advances, there are three basic ingredients in the manufacture of reliable integrated circuits.

First, The device must be designed with the user's applications and reliability requirements in mind. Secondly, The device must be manufactured with the optimum technology for the application.

Thirdly, Controls must be established to assure maintenance of the quality/reliability levels.

Goldstar Semiconductor has a Quality Assurance System and conducts extensive reliability testing to supply its customer's needs.

This report presents Quality Assurance System and Reliability test results of Goldstar Semiconductor Company Products.

2. QUALITY ASSURANCE SYSTEM

To ensure that customers are satisfied with the products that are supplied, quality assurance programs are used at both the design and manufacturing phases, focusing on the following points:

- (1) In the development stage, reliability is designed into products. A thorough evaluation of reliability is performed to ascertain whether the design will lead to the desired quality and reliability.
- (2) Efforts are made at the manufacturing stage of quality control to assure that quality and reliability are built into products. Intermediate, final, and quality assurance inspection are used to verify that the desired quality and reliability have been achieved.
- (3) Information with regard to quality is fed back in a timely manner so that the required corrective action can be taken by quality assurance personnel.

2.1 Quality Assurance at the Development Stage

It is not an exaggeration to say that the fundamental quality and reliability of a discrete semiconductor device or an integrated circuit is determined at the design stage. Thus, to eliminate design problems and provide design improvements while attaining the desired quality and reliability, design reviews are performed on prototypes assure product quality. Particularly in the case of integrated circuits, bread-board models of the circuit using standard components can be an effective means of evaluating the required characteristic and quality. In addition CAD technology may be used to aid in the design of circuits and devices based on design standards.

Between the development stage, and mass production, there are two steps of prototype and pre-production (trial mass production).

At the prototype development stage, new theories, technologies and concepts are used by the development department to design and produce a new product. To determine whether the desired goals for characteristics, ratings, and reliability have been met, primary type test is performed at this stage. Based on these results, thorough investigations are made by both the engineering and quality assurance departments. Should product deficiencies arise, inspections and failure analysis are performed to enable improvements of the development prototype.

At the pre-production stage, the production department produces sufficient products having quality equal to or superior to the prototype. At this stage, secondary type test is used to verify quality. The required product specifications, operation instructions, drawings, etc., are produced at this stage in addition to the required manufacturing facilities.

2.2 Quality Assurance at the Mass Production Stage

At the mass production stage, the production department takes over production of product based on production planning. To maintain equal or better quality than that obtained in previous stages, careful control of materials purchasing, production processing, environment and facilities is performed. In addition, in process inspections and final inspections provide the required information with regard to partially completed and completed devices to assure overall quality.

2.2.1 Control of Materials Purchasing

While the responsibility for quality of individual materials purchased from vendors based on drawings and purchase specifications is the responsibility of the vendor, the corporation provides data from incoming inspection of sampled products as a means of monitoring quality and assuring materials quality.

Selection of vendors is made after an investigation of quality control, management, facilities and production capacity of the vendor, placing heavy emphasis on quality. Next, a meeting is held with the vendor concerning the purchase specifications, and prototypes or sample evaluations are used to verify quality at the beginning of a purchase cycle or after a change in manufacturing method or specifications.

2.2.2 Control of the Manufacturing Process

To prototype products of high quality in an economic manner, quality must be built-in at the manufacturing stage. To do this, work is carried out in accordance with operation instructions and check sheets are used to control those aspects of manufacturing that could affect quality. For example, such information as the purity of water, atmosphere, furnace temperature and gas flow are recorded. In addition, because of their great influence on diffusion, diffusion depth and surface density are recorded and used as control data for process conditions. Also, operations such as wire bonding which are affected by differences of individuals have been fully automated to contribute to product uniformity.

In-process inspections and final inspections are performed to evaluate product quality including outward appearance, dimensions, structure, as well as mechanical and electrical characteristics. The data obtained by such inspections is fed back to earlier processes to maintain and improve product quality as well as reduce variations in these areas.

Wafer processing and assembly inspections are part of the in-process inspection program, each contributing to the concept of building in quality at the manufacturing stage by providing self checks and the inspections performed by the quality control department. A final inspection of all products is performed to verify electrical characteristics as well as outward appearance of products. In addition, to improve product quality uniformity, debugging is used as a means of eliminating products which do not meet quality specifications. Again, data from these inspections are useful in quality control.

Products which have passed final inspection are then subjected to quality assurance inspections. This is a form of overall inspection from the standpoint of the end user and is used to accept or reject products on a lot basis, including tests of outward appearance, electrical characteristics, thermal and mechanical environment, and endurance. As an additional control test, samples are made periodically for evaluation of reliability. These tests include those of electrical characteristics, thermal and mechanical environment, and endurance for long periods of operation. The information on quality obtained by such quality assurance inspections is fed back in a timely fashion to the related departments, enabling the maintenance and improvement of quality as well as providing a means of predicting product quality in the market place.


QUALITY ASSURANCE MANUAL

STANDARD ASS'Y FLOW CHART OF GSS

FLOW CHART	PROCESS TITLE	QC POINT
	Wafer	
	Foil Mount	
	Wafer Sawing	
	Q.C Monitor * DI Water * Visual	RESISTIVITY VISUAL
	Die Bond	
	Q.C Monitor * Visual * Die Shear	APPEARANCE STRENGTH
	Wire Bond	
	Q.C Monitor * Visual * Bond pull * Crater	APPEARANCE APPEARANCE, STRENGTH CRATER
	3rd Optical Insp.	
	Q.C 3/O gate * Visual	APPEARANCE
	Molding	SPRIAL FLOW
	Q.C Monitor * Visual * X-Ray Monitor	APPEARANCE X-RAY INSP.
	Deflash/Trim/Form	
	Q.C Monitor * Visual/Dimension	APPEARANCE/DIMENSION

QUALITY ASSURANCE MANUAL

FLOW CHART	PROCESS TITLE	QC POINT
<pre> graph TD Start(()) --- A(()) A --- B[] B --- C{ } C --- D[] D --- E(()) E --- F[] F --- G[] G --- H(()) H --- I[] I --- J{ } J --- K[] K --- End(()) </pre>	Solder-Dipping	
	Q.C Monitor * Temp of S/Bath * Sn in Solder * Solderability	TEMPERATURE. % OF Sn APPEARANCE
	4th Optical Insp	
	4th O/Gate * Visual	APPEARANCE
	Temp. cycle (Option)	
	Mark & Cure	
	Final Visual/Mech.	
	Initial Class	
	Burn-In (Option)	
	Final Test	
	Q.C Final Gate * Visual * Electrical	APPEARANCE ELECTRICAL PARAMETERS * D.C & SPEED * FUNCTION
	RELIABILITY TEST * LIFE TEST LTPD: 5% * 85/85 TEST LTPD: 10% * PRESSURE POT LTPD: 10% * THERMAL SERIES LTPD: 10% * LEAD INTEGRITY LTPD: 20% * PHYSICAL DIMENSION LTPD: 15%	ENVIRONMENTAL TEST MECHANICAL TEST AND ENDURANCE TEST

FLOW CHART	PROCESS TITLE	QC POINT
	<p>* RESISTANCE TO SOLVENTS LTPD: 15%</p> <p>* SOLDERABILITY LTPD: 10%</p> <p>Packing</p> <p>Q.C Pack Gate</p> <p>Ship</p> <p>* ESD MONITOR (ALL PROCESS)</p>	

2.2.3 Environmental Control

In the semiconductor industry, the environment plays a large role in influencing product quality and reliability. Control levels for dust, humidity, and temperature are set and rigidly maintained. The gases or water used in the production plant are carefully controlled to ensure high level of purity.

The control of dust is particularly important in reducing manufacturing defects and improving quality and reliability. For this reason the Corporation places heavy emphasis in this area, providing strict controls of working conditions and periodic checks to verify that these are being maintained.

2.2.4 Control of Production Equipment and Instrumentation.

The semiconductor industry is an equipment intensive industry having adopted a large variety of automatic equipment and high performance facilities to provide uniform high quality. The control of such equipment and instrumentation is extremely important in the manufacture of devices. For this reason, to eliminate loss of accuracy and equipment failures, periodic preventive maintenance and inspections are performed.

3. RELIABILITY TEST

3.1 Principle of Reliability

The fundamental principles of reliability engineering predict that the failure rate of any group of devices as a function of time will follow a curve similar to Figure 1. The curve is divided into three regions: Infant Mortality, Random Failures and Wearout Failures. These regions describe the principal classes of failure mechanisms encountered in that portion of the life of a device.

Infant Mortality represents the early life failures of a device. Failures in this region are usually associated with one or more manufacturing defects. After some period of time the failure rate reaches a low value or the Random failure portion of the curve that represents the useful portion of device life. Infant Mortal

failures are eliminated prior to customer shipment by high voltage cell stress, HTRB and reliability screen testing. (Baking, Temp Cycle, Burn-IN)

Wearout failures occur at the end of the device's useful life and are characterized by rapidly rising failure rate with time. This does not occur before hundreds of years for integrated circuits.

Associated with each portion of the curve are specific failure mechanisms. These failure mechanisms have been extensively discussed in the literature.

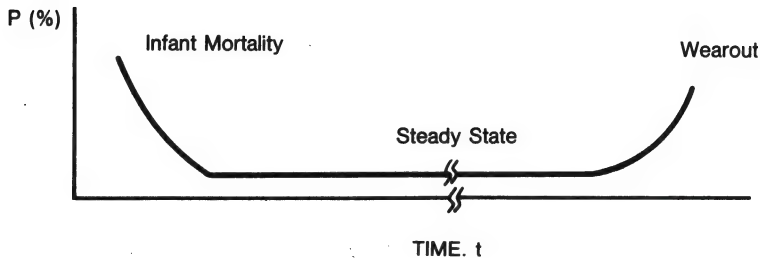


Figure 1. Reliability Life (Bath-tub) Curve

3.2 Reliability Test Items and Conditions

I. Group A: ELECTRICAL TEST

TEST ITEMS.	METHOD.	MIL-STD-883C	GOLDSTAR SEMI.
1. STATIC TEST (AT 25°C)		LTPD 2 : S/S = 266 C = 26	
2. STATIC TEST (AT MAX. OP. TEMP.)		LTPD 3 : S/S = 176 C = 2	AQL = 0.04% S/S = 315 C = 0
3. STATIC TEST (AT MIN. OP. TEMP.)		LTPD 5 : S/S = 105 C = 2	
4. DYNAMIC TEST (AT 25°C)		LTPD 2 : S/S = 266 C = 2	
5. DYNAMIC TEST (AT MAX. OP. TEMP.)		LTPD 3 : S/S = 176 C = 2	
6. DYNAMIC TEST (AT MIN. OP. TEMP.)		LTPD 5 : S/S = 105 C = 2	
7. FUNC. TEST (AT 25°C)		LTPD 2 : S/S = 266 C = 2	
8. FUNC. TEST (AT MAX. MIN OP. TEMP.)		LTPD 5 : S/S = 105 C = 2	
9. SWITCHING (AT 25°C)		LTPD 2 : S/S = 266 C = 2	
10. SWITCHING (AT MAX. OP. TEMP.)		LTPD 3 : S/S = 176 C = 2	
11. SWITCHING (AT MIN. OP. TEMP.)		LTPD 5 : S/S = 105 C = 2	

QUALITY ASSURANCE MANUAL

II. Group B : Per Lot

TEST ITEMS.	METHOD.	MIL-STD-883C	GOLDSTAR SEMI.
Sub 1 PHYSICAL DIMENSION	2016	n = 2 : c = 0	n = 2 : c = 0
Sub 2 RESISTANCE TO SOLVENTS	2015	n = 4 : c = 0	LTPD 15% S/S = 15 C = 0
Sub 3 SOLDERABILITY TEST	2022 2003	LTPD 15% S/S = 15 C = 0	LTPD 10% S/S = 22 C = 0
Sub 4 INTERNAL VISUAL & MECHANICAL	2014	n = 1 : c = 0	n = 1 : c = 0
Sub 5 BOND STRENGTH	2011	LTPD 15% S/S = 15 C = 0	LTPD 15% S/S = 15 C = 0
Sub 6 INTERNAL WATER VAPOR CONTENT	1018	n = 3 : c = 0 or n = 5 : c = 1	NOT BEING
Sub 7 SEAL			
FINE LEAK	1014	LTPD 5% S/S = 45	LTPD 5% S/S = 45
GROSS LEAK		C = 0	C = 0
Sub 8			
A) ELECTRICAL PARAMETERS	Gr A	n = 15 : c = 0	LTPD 10% S/S = 22
B) E. S. D CLASSIFICATION	3015		C = 0
C) ELECTRICAL PARAMETERS	Gr A		

III. Group C : PERIODIC : DIE-RELATED TESTS

TEST ITEMS.	METHOD.	MIL-STD-883C	GOLDSTAR SEMI.
Sub 1			
A) STEADY STATE LIFE TEST	1005	AT 125°C : 1000 HRS	AT 125°C : 1000 HRS
B) END POINT ELECTRICAL.		LTPD 5% S/S = 77 C = 1	LTPD 5% S/S = 77 C = 1
Sub 2			
A) TEMPERATURE CYCLE	1010	TEST COND. C LTPD 15% S/S = 25, C = 1	TEST COND. C : 100 CYCLE LTPD 15% S/S = 25, C = 1
B) CONSTANT ACCELERATION	2001	TEST COND. E Y1 ORIENTATION ONLY	TEST COND. E Y1 ORIENTATION ONLY
C) SEAL	1014		
FINE LEAK		TEST COND. B	TEST COND. B
GROSS LEAK		TEST COND. C	TEST COND. C
D) VISUAL EXAMINATION	1010		
	1011		
E) END POINT ELECTRICAL.			

QUALITY ASSURANCE MANUAL

IV. Group D : PACKAGE RELATED TESTS

TEST ITEMS.	METHOD.	MIL-STD-883C	GOLDSTAR SEMI.
Sub 1 PHYSICAL DIMENSION	2016	LTPD 15% S/S = 15 C = 0	LTPD 15% S/S = 15 C = 0
Sub 2 A) LEAD INTERGRITY	2004	LTPD 15% S/S = 15 C = 0	LTPD 15% S/S = 15 C = 0
B) SEAL FINE LEAK GROSS LEAK	1014	TEST COND. B TEST COND. C	TEST COND. B TEST COND. C
Sub 3 A) THERMAL SHOCK	1011	COND. B : 15 CYCLES LTPD 15% S/S = 15 C = 0	NOT BEING
B) TEMPERATURE CYCLE	1010	TEST COND. C : 100 CYCLE	TEST COND. C : 100 CYCLE
C) MOISTURE RESISTANCE	1004		
D) SEAL FINE LEAK GROSS LEAK	1004	TEST COND. B TEST COND. C	TEST COND. B TEST COND. C
E) VISUAL EXAMINATION	1010 & 1004		
F) END POINT ELECTRICAL.			
Sub 4 A) MECHANICAL SHOCK	2002	LTPD 15% S/S = 15 COND. B C = 0	LTPD 15% S/S = 15 COND B C = 0
B) VIBRATION, VARIABLE FREQUENCY	2007	TEST COND. A	TEST COND. A
C) CONSTANT ACCELERATION	2001	TEST COND. E Y1 ORIENTATION ONLY	TEST COND. E Y1 ORIENTATION ONLY
D) SEAL FINE LEAK GROSS LEAK	1014	TEST COND. B TEST COND. C	TEST COND. B TEST COND. C
E) VISUAL EXAMINATION	1010 & 1011		
F) END POINT ELECTRICAL.			
Sub 5 A) SALT ATMOSPHERE	1009	LTPD 15% S/S = 15 COND A C = 0	NOT BEING
B) VISUAL EXAMINATION	1009		
C) END POINT ELECTRICAL.			
Sub 6 INTERNAL WATER VAPOR CONTENT (5000 PPM)	1018	n = 3 : c = 0 or n = 5 : c = 1	NOT BEING
Sub 7 ADHESION OF LEAD FINISH	2025	LTPD 15% S/S = 15 C = 0	LTPD 15% S/S = 15 C = 0
Sub 8 LID TORQUE	2024	n = 5 : c = 0	n = 5 : c = 0

QUALITY ASSURANCE MANUAL

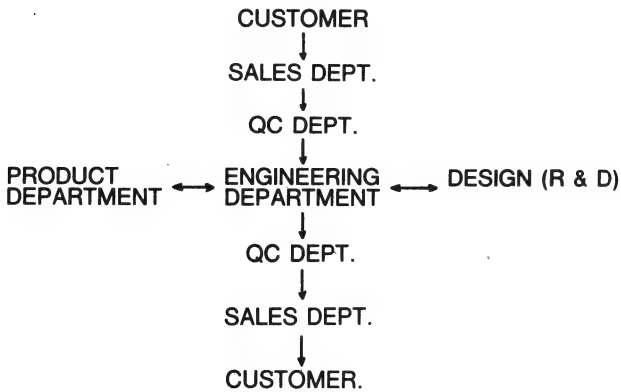
V. Group E : RADIATION HARDNESS ASSURANCE TESTS

TEST ITEMS.	METHOD.	MIL-STD-883C	GOLDSTAR SEMI.
Sub 1 NEUTRON IRRADIATION A) QUALIFICATION B) QCI	1017	at 25°C n = 15 : c = 0 n = 11 : c = 0	NOT BEING
Sub 2 STEADY-STATE TOTAL DOSE IRRADIATION A) QUALIFICATION B) QCI	1019	at 25°C n = 15 : c = 0 n = 11 : c = 0	NOT BEING

QUALITY ASSURANCE MANUAL

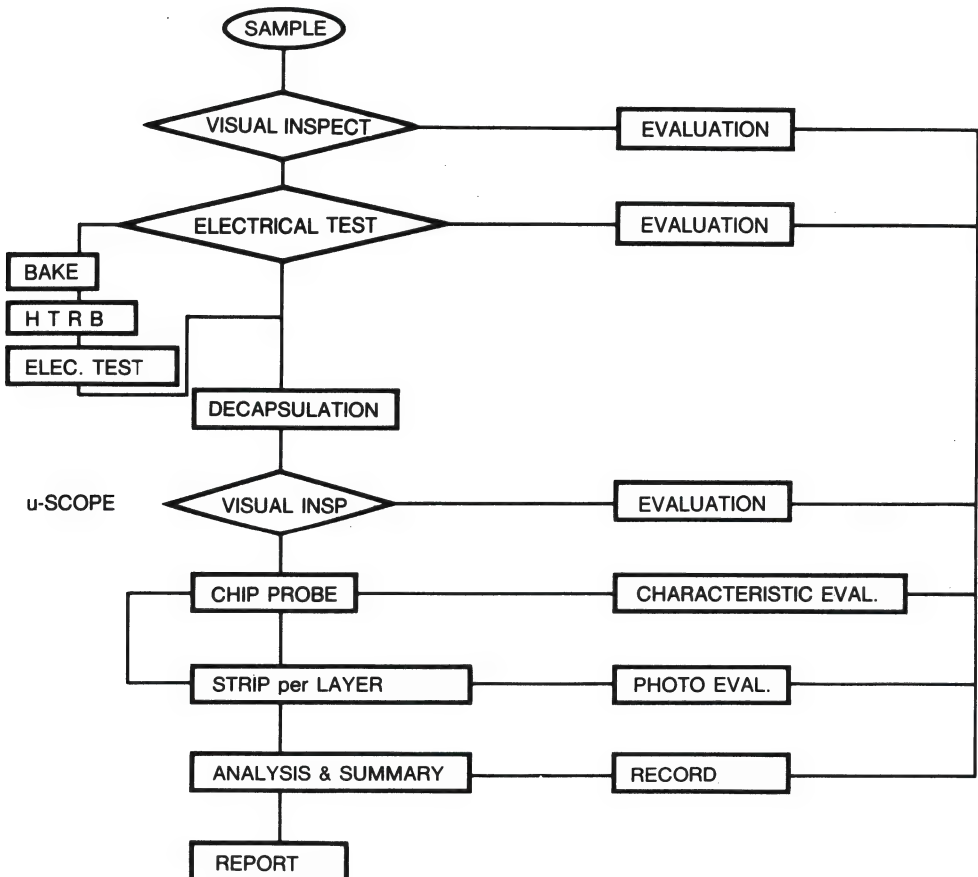
FMA FLOW CHART

PROCEDURE OF FAILURE ANALYSIS



- CLAIM, COMPLAINT
- IF REQUIRED, SEND DEVICE FAILED TO QC DEPT.
- * FAILURE ANALYSIS
- DETAILED INVESTIGATION.
- CORRECTIVE ACTION
- PREVENTION OF REOCCURENCE
- REPORT THE RESULT
- ANSWER TO THE CLAIM.

* FAILURE ANALYSIS



RELIABILITY TEST ITEMS of GOLDSTAR SEMICONDUCTOR

PLASTIC-DIP ONLY

ITEM	TEST ITEM	TEST CONDITION	QUALITY APPROVAL				QUALITY CONFORMANCE			
			TEST FREQ	S/S	LTPD	# of ACC.	TEST FREQ	S/S	LTPD	# of ACC.
1	Visual Inspection	Outgoing Visual Specification		—	—	—	Every Lot		ACL 0.065%	0
2	Electrical Test (DC/AC)	Outgoing Test Specification		—	—	—	Every Lot		ACL 0.04%	0
3	Dimension	Lead Thickness	Every Lot	5	—	0	Every Lot	1	—	0
4	Dimension	All Dimension	Every Week	5	—	0	Every Week	1	—	0
5	Packaging Inspection	Outgoing Packaging Specification		—	—	—	Every Lot	All	—	0
6	High Temperature Operating Life Test	Ta=125 C, t=1000 HRS Vcc=5V	Every 3 Month	77	5	1	Every Week	38	10	1
7	High Temperature Storage Test	Ta=150 C, t=1000 HRS	Every 3 Month	38	10	1		—	—	—
8	Biased Humidity Test	Ta=85 C 35% RH Vcc=5V, t=1000	Every 3 Month	38	10	1	Every Week	38	10	1
9	Pressure Pot	Ta=121 C, 30 PSIG 100% RH, 100 HRS	Every 3 Month	38	10	1	Every Week	25	15	0
10	Temperature Cycle Test	-65 C 25 C 150 C 10 Min, 5 Min, 10 Min 200 Cycle	Every 3 Month	38	10	1	Every Week	22	10	0
11	Lead Integrity	3 X, 90 Arcs 5 Units	Every 3 Month	15	15	0		—	—	—
12	Solderability	Solder Temp 240 5°C, Steam Aging 1 HRS Flux 6Sec, Solder 5Sec	2 Times / Weeks	22	10	0	2 Times / Weeks	22	10	0
13	Resistance to Solvents		Every Lot	15	15	0	Every Lot	15	15	0
14	Electro Static Discharge	MIC-STD-883C METHOD 3015	Every Lot	22	10	0	Every Lot	15	15	0

4. SUMMARY

This report has presented quality assurance system and reliability test on GoldStar Semiconductor devices. According to the reliability test results and actual experimental data of operating life test, it is concluded that GoldStar devices are high quality devices and the incoming failure rate is expected to be less than 0.04%.

5. HANDLING AND STORAGE INSTRUCTION

5.1 HANDLING PRECAUTIONS

For all devices, the following practices should be observed for protection against high electrical static discharges.

5.1.1 Device leads should be in contact with a conductive material except when being tested or in actual operation.

5.1.2 Conductive parts tools, fixtures, soldering irons and handling equipment should be grounded to handle the devices.

5.1.3 Devices should not be inserted into or removed from test stations unless the power is off.

5.1.4 Neither should signals be applied to the input while the device power supply is in an off condition.

5.1.5 Operators should use grounded wrist straps and work conductive surfaces should be also grounded.

5.2 STORAGING PRECAUTIONS.

There are several basic requirements in case of long term storage for semiconductor devices.

5.2.1 Store the devices in a covered or sealed antistatic container.

5.2.2 Store the devices in an environment of no more than 60% relative humidity.

5.2.3 Store the devices in a inert atmosphere not exceeding $+125^{\circ}\text{C}$ or no more than -55°C .

5.2.4 Physical force is not permitted on any leads or plastic body when the devices are stored for prevention damage of device.



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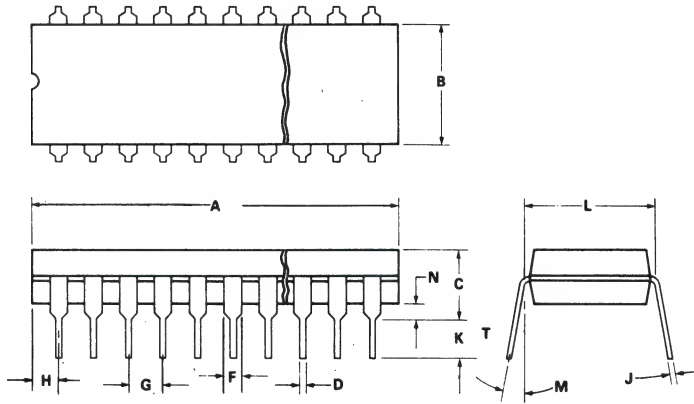
ORDERING INFORMATION

Marking Code Formats of GS CMOS Logic are Shown as following Example:

Ex: GD 74 HC 373 A D
(1) (2) (3) (4) (5) (6)

- (1) GD, Prefix of GS Digital IC
- (2) Operating Temperature Range
74; -40°C to $+85^{\circ}\text{C}$
54; -55°C to $+125^{\circ}\text{C}$
- (3) Classification of CMOS Logic
HC : CMOS input switching levels, supply voltage range 2 to 6V and fully buffered
HCT : TTL input switching levels, supply voltage range 4.5 to 5.5V and fully buffered.
HCU : CMOS input switching levels, supply voltage range 2 to 6V and unbuffered (single-stage devices)
- (4) Consecutive Number to Indicate the Each Type
- (5) Alphabet: Series Improved.
- (6) Package Type
Blank: Plastic Dual In Line Package
J : Cermic Dual In Line Package
D : Small Outline Package.

PLASTIC DIP



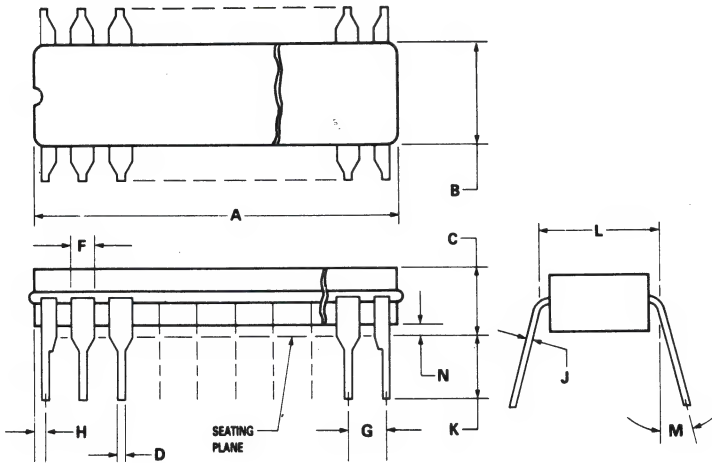
(INCHES)

SYMBOL	14 PIN		16 PIN		20 PIN		24 PIN	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	0.743	0.778	0.743	0.780	1.013	1.040	1.243	1.270
B	0.245	0.255	0.245	0.255	0.263	0.273	0.535	0.545
C	0.145	0.200	0.145	0.200	0.145	0.200	0.170	0.210
D	0.015	0.021	0.015	0.021	0.015	0.021	0.015	0.021
F	TYP 0.065		TYP 0.065		TYP 0.065		TYP 0.065	
G	0.09	0.11	0.09	0.11	0.09	0.11	0.09	0.11
H	—	0.075	0.015	0.045	0.055	0.065	0.06	0.09
J	0.009	0.015	0.009	0.015	0.009	0.015	0.009	0.015
K	0.125	0.140	0.125	0.140	0.125	0.140	0.125	0.140
L	0.300	0.320	0.300	0.320	0.300	0.320	0.6	0.62
M	0°	10°	0°	10°	0°	10°	0°	10°
N	0.02	—	0.02	—	0.02	—	0.015	—

(MILLIMETERS)

SYMBOL	14 PIN		16 PIN		20 PIN		24 PIN	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	18.87	19.56	18.87	19.81	25.73	26.42	31.57	32.26
B	6.223	6.477	6.223	6.477	6.477	6.731	13.589	13.843
C	3.683	5.080	3.683	5.080	3.683	5.080	4.318	5.234
D	0.387	0.527	0.387	0.527	0.387	0.527	0.387	0.527
F	TYP 1.524		TYP 1.524		TYP 1.524		TYP 1.524	
G	2.286	2.794	2.286	2.794	2.286	2.794	2.286	2.794
H	—	1.905	0.381	1.143	1.397	1.651	1.524	2.286
J	0.229	0.381	0.229	0.381	0.229	0.381	0.229	0.381
K	3.175	3.554	3.175	3.554	3.175	3.554	3.175	3.554
L	7.620	8.128	7.620	8.128	7.620	8.128	15.24	15.75
M	0°	10°	0°	10°	0°	10°	0°	10°
N	5.08	—	5.08	—	5.08	—	3.81	—

CERAMIC DIP



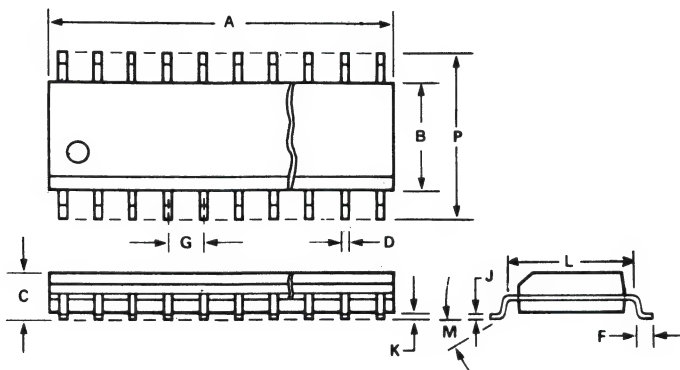
(INCHES)

SYMBOL	14 PIN		16 PIN		20 PIN		24 PIN	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	—	0.785	—	0.785	—	0.985	—	1.290
B	0.22	0.31	0.22	0.31	0.22	0.31	0.514	0.526
C	—	0.18	—	0.18	—	0.18	—	0.18
D	0.015	0.021	0.015	0.021	0.015	0.021	0.015	0.021
F	0.055	0.065	0.055	0.065	0.050	0.060	0.055	0.065
G	0.09	0.11	0.09	0.11	0.09	0.11	0.09	0.11
H	—	0.098	—	0.08	—	0.08	—	0.098
J	0.008	0.012	0.008	0.012	0.008	0.012	0.008	0.012
K	0.125	0.20	0.125	0.20	0.125	0.20	0.125	0.20
L	0.29	0.32	0.29	0.32	0.29	0.32	0.59	0.62
M	0°	10°	0°	10°	0°	10°	0°	10°
N	0.02	0.06	0.02	0.06	0.02	0.07	0.02	0.06

(MILLIMETERS)

SYMBOL	14 PIN		16 PIN		20 PIN		24 PIN	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	—	19.939	—	19.939	—	25.019	—	32.766
B	5.588	7.784	5.588	7.784	5.588	7.784	13.06	13.36
C	—	4.572	—	4.572	—	4.572	—	4.572
D	0.387	0.527	0.387	0.527	0.387	0.527	0.387	0.527
F	1.397	1.651	1.397	1.651	1.27	1.524	1.397	1.651
G	2.286	2.794	2.286	2.794	2.286	2.794	2.286	2.794
H	—	2.489	—	2.032	—	2.489	—	2.489
J	0.203	0.305	0.203	0.305	0.203	0.305	0.203	0.305
K	3.175	5.080	3.175	5.080	3.175	5.080	3.175	5.080
L	7.366	8.128	7.366	8.128	7.366	8.128	14.986	15.748
M	0°	10°	0°	10°	0°	10°	0°	10°
N	0.051	0.152	0.051	0.152	0.051	0.178	0.051	0.152

SOIC



(INCHES)

SYMBOL	14 PIN		16 PIN		20 PIN		24 PIN	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	0.337	0.344	0.386	0.394	0.496	0.510	0.598	0.614
B	0.15	0.157	0.15	0.157	0.291	0.299	0.291	0.299
C	0.053	0.069	0.053	0.069	0.093	0.104	0.093	0.104
D	0.014	0.019	0.014	0.019	0.014	0.019	0.014	0.019
F	0.027	0.035	0.027	0.035	0.027	0.035	0.034	0.042
G	0.050 BSC		0.050 BSC		0.050 BSC		0.050 BSC	
J	0.007	0.010	0.007	0.010	0.009	0.013	0.009	0.013
K	0.004	0.008	0.004	0.008	0.004	0.008	0.004	0.008
L	0.189	0.205	0.189	0.205	0.368	0.375	0.368	0.375
P	0.228	0.244	0.228	0.244	0.404	0.419	0.404	0.419
M	0°	8°	0°	8°	0°	8°	0°	8°

(MILLIMETERS)

SYMBOL	14 PIN		16 PIN		20 PIN		24 PIN	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	8.55	8.75	9.80	10.10	12.60	13.00	15.20	15.60
B	3.80	4.00	3.80	4.00	7.40	7.60	7.40	7.60
C	1.35	1.75	1.35	1.75	2.35	2.65	2.35	2.65
D	0.35	0.49	0.35	0.49	0.35	0.49	0.35	0.49
F	0.69	0.89	0.69	0.89	0.86	1.07	0.86	1.09
G	1.27 BSC		1.27 BSC		1.27 BSC		1.27 BSC	
J	0.19	0.25	0.19	0.25	0.23	0.32	0.23	0.32
K	0.10	0.20	0.10	0.20	0.10	0.20	0.10	0.20
L	4.82	5.21	4.82	5.21	9.34	9.53	9.34	9.53
P	5.80	6.20	5.80	6.20	10.26	10.65	10.26	10.65
M	0°	8°	0°	8°	0°	8°	0°	8°



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